EMC Control with PCB Design for Working Engineers

April 2010

IBM

Dr. Bruce Archambeault
IBM Distinguished Engineer and IEEE Fellow
barch@us.ibm.com

About the Presenter

- **Dr. Bruce Archambeault**

- Dr. Bruce Archambeault received his B.S.E.E degree from the University of New Hampshire in 1977 and his M.S.E.E degree from Northeastern University in 1981. He received his Ph. D. from the University of New Hampshire in 1997. His doctoral research was in the area of computational electromagnetics applied to real-world EMC problems. In 1981 he joined Digital Equipment Corporation and through 1994 he had assignments ranging from EMC/TEMPEST product design and testing to developing computational electromagnetic EMC-related software tools. In 1994 he joined SETH Corporation where he continued to develop computational electromagnetic EMC-related software tools and used them as a consulting engineer in a variety of different industries. In 1997 he joined IBM in Raleigh, N.C. where he is the EMC Distinguished Engineer, responsible for EMC tool development and use on a variety of products. During his career in the U.S. Air Force he was responsible for in-house communications security and TEMPEST/EMC related research and development projects.

- Dr. Archambeault has authored or co-authored a number of papers in computational electromagnetics, mostly applied to real-world EMC applications. He is a past Board of Directors member of the IEEE EMC Society and Applied Computational Electromagnetics Society (ACES). He is the author of the book "PCB Design for Real-World EMI Control" and the lead author of the book titled "EMI/EMC Computational Modeling Handbook".

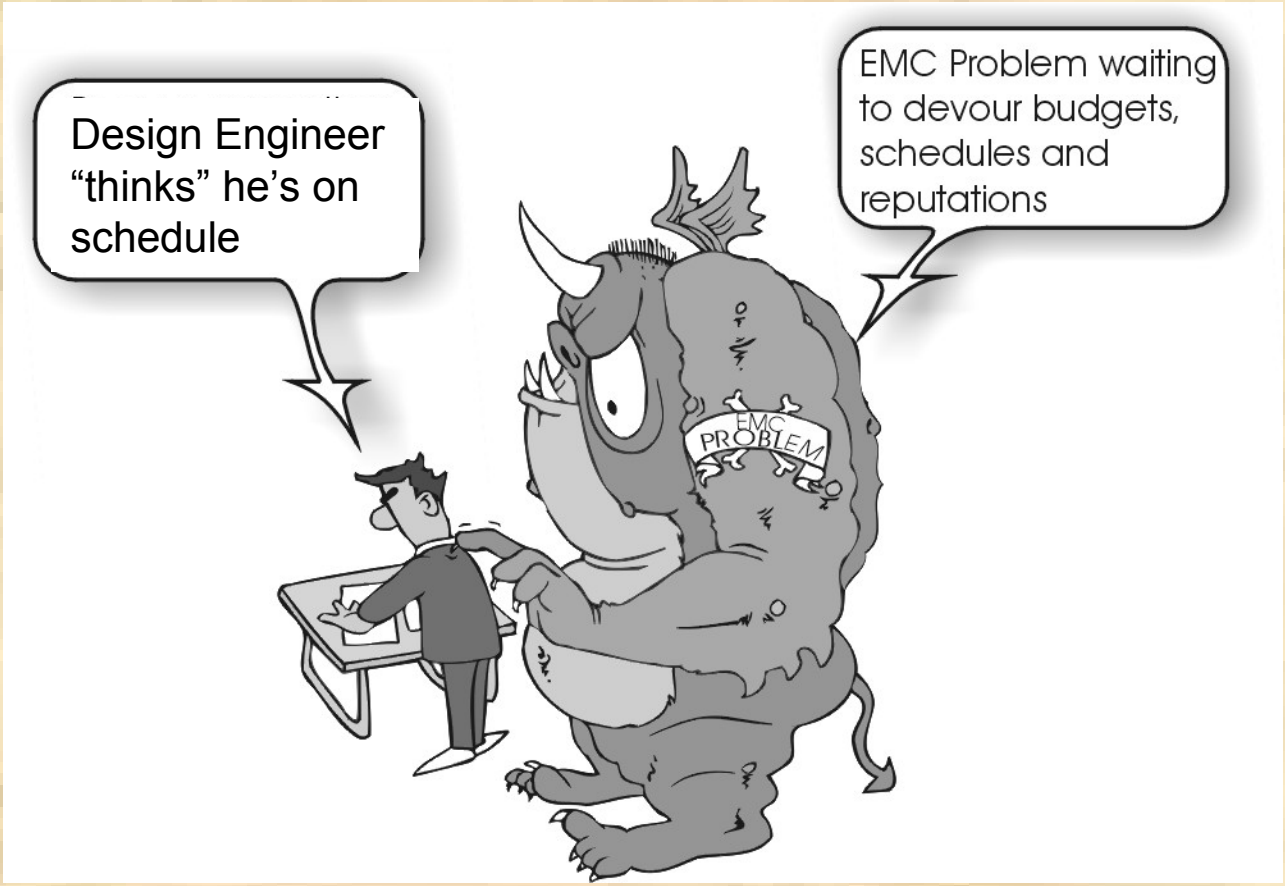
Course Outline

- Introduction
- EM Review
- Antennas
- Grounding
- Printed Circuit Board EMC Design
- Summary and Review

Details, Details, Details

- Course schedule
- Rest rooms
- Lunch
- Informal !!!

EMC Can Be Ugly



Why do we care?

- Interference with critical systems
- Self jamming of internal radio systems
- Physical destruction of sensitive electronics
- Susceptibility and emissions
- Legal requirements
- Examples

EM Review

- dB
- Time and Frequency Domain
- wavelength
- Integration
- Maxwell's Equations
- Skin Depth
- Inductance
- Capacitance
- Far field vs. near field

Decibel (dB)

- Unit of measure expressing a ratio of TWO quantities (no units)
  - 20 * LOG10 (1st number/ 2nd number)
- Absolute levels are related to a standard value
  - 20 * LOG10 (1st number/ standard value)

Decibel Examples

- A 10% pay raise would be only 0.8 dB!
- The Pacific Ocean is 6.3 dB larger than the Atlantic Ocean
- the ratio of 10000:1 is 80 dB
- The ratio of 0.000002345: 1 is -112 dB
- One order of magnitude = 20 dB
- Factor of 2 = 6 dB

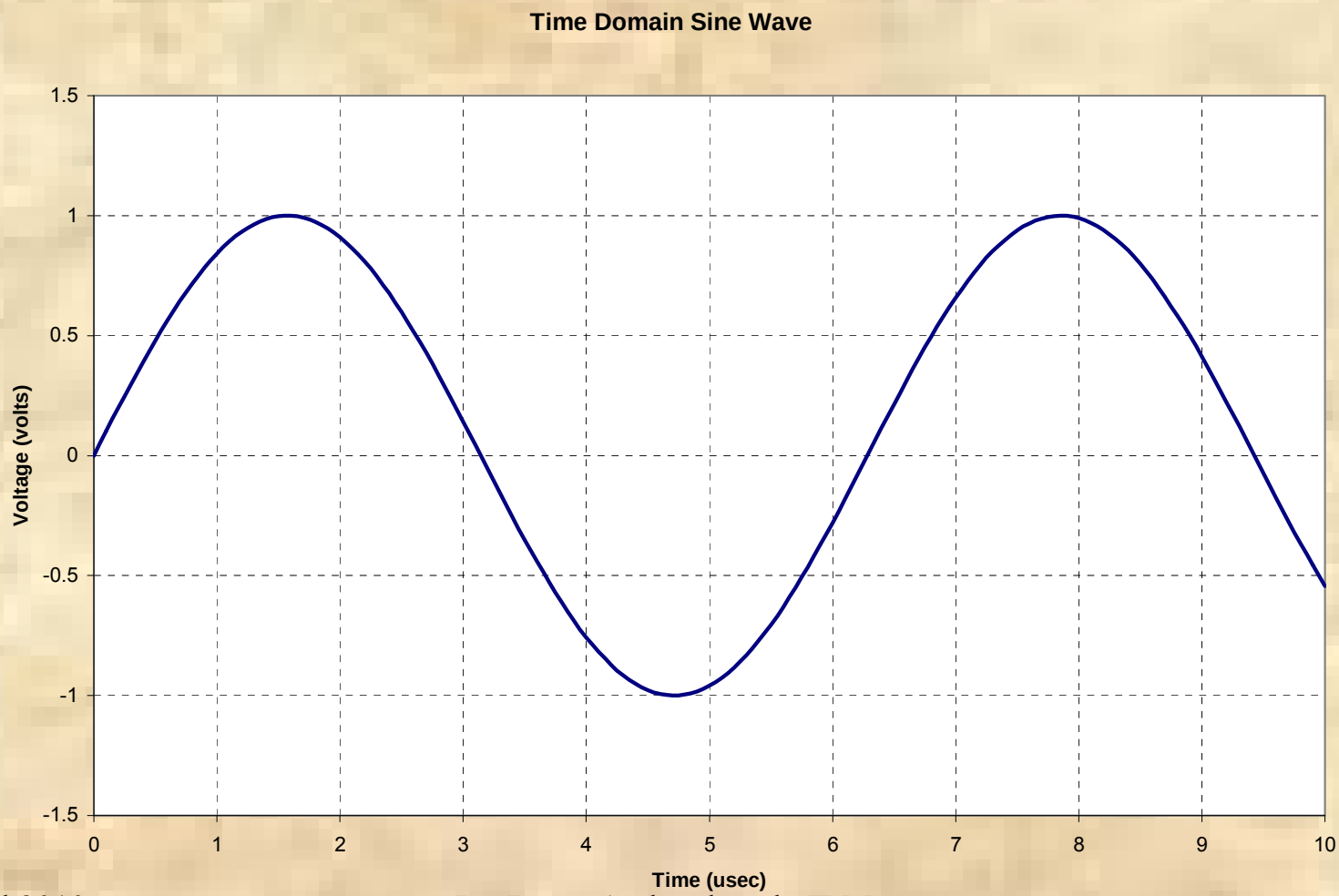
More on Decibels

- Absolute voltage is usually relative to 1 uv
  - dBuv
  - 20 * LOG10 (volts/1e-6)
- Absolute power is usually relative to 1 mw
  - dBm
  - 10 * LOG10 (power/1e-3)
  - Usually in a 50 ohm system

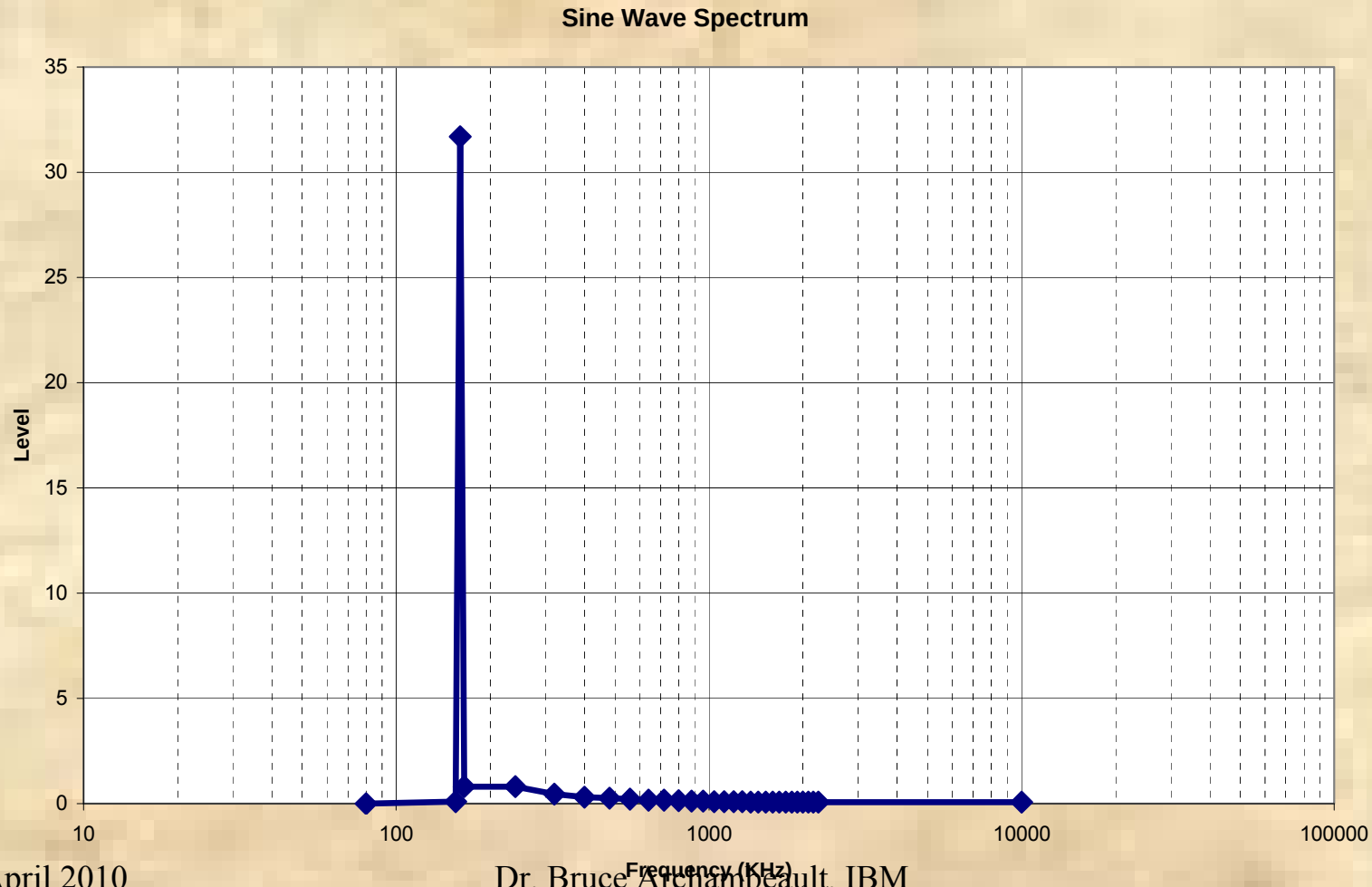
Time and Frequency Domain

- Different ways to look at the same thing
- Time domain is usually used by Logic design engineers and signal integrity engineers
- Frequency domain is usually used by EMC engineers

Time Domain Example
Sine Wave

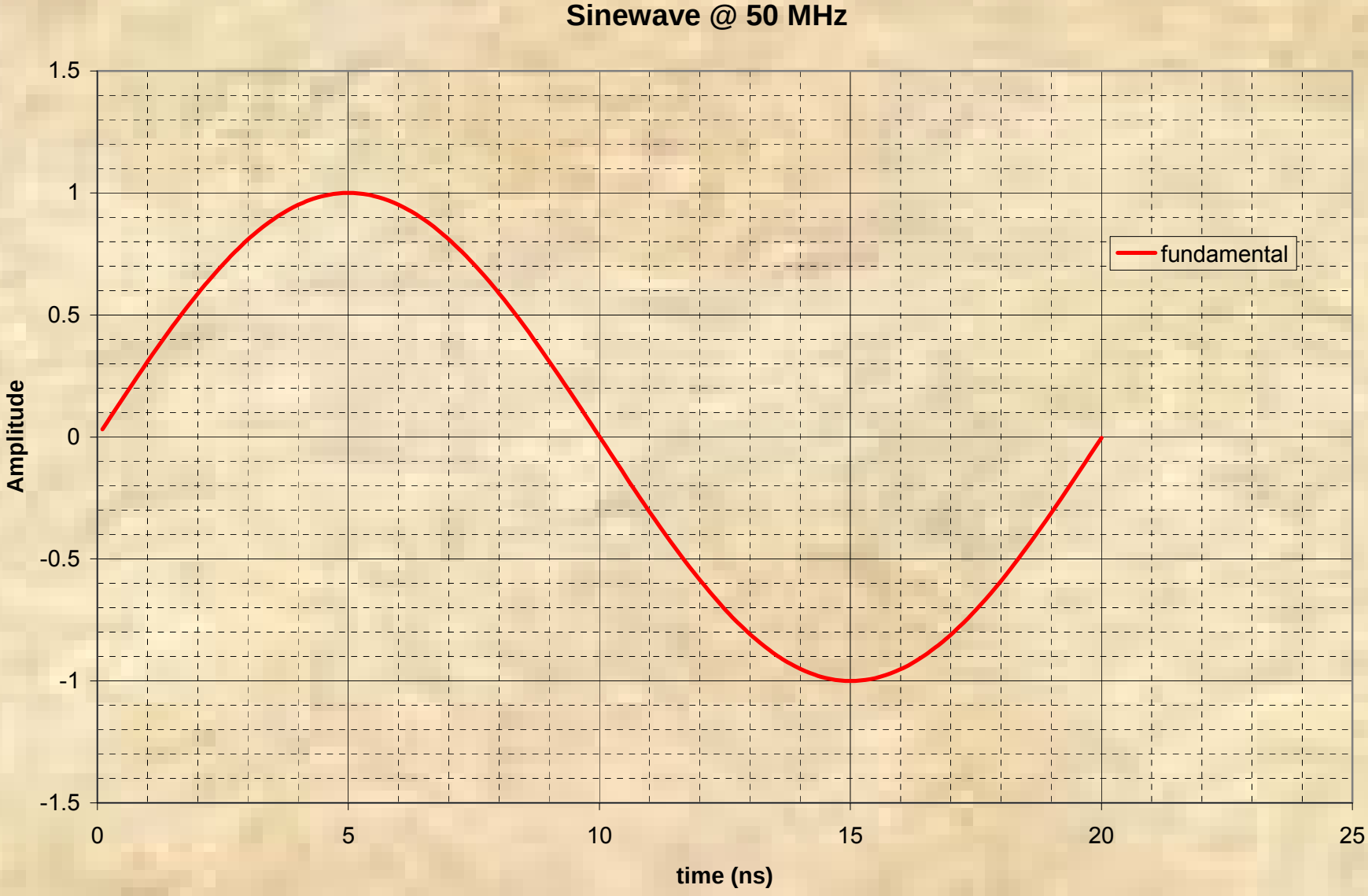


Frequency Domain Example
Sine Wave Spectrum

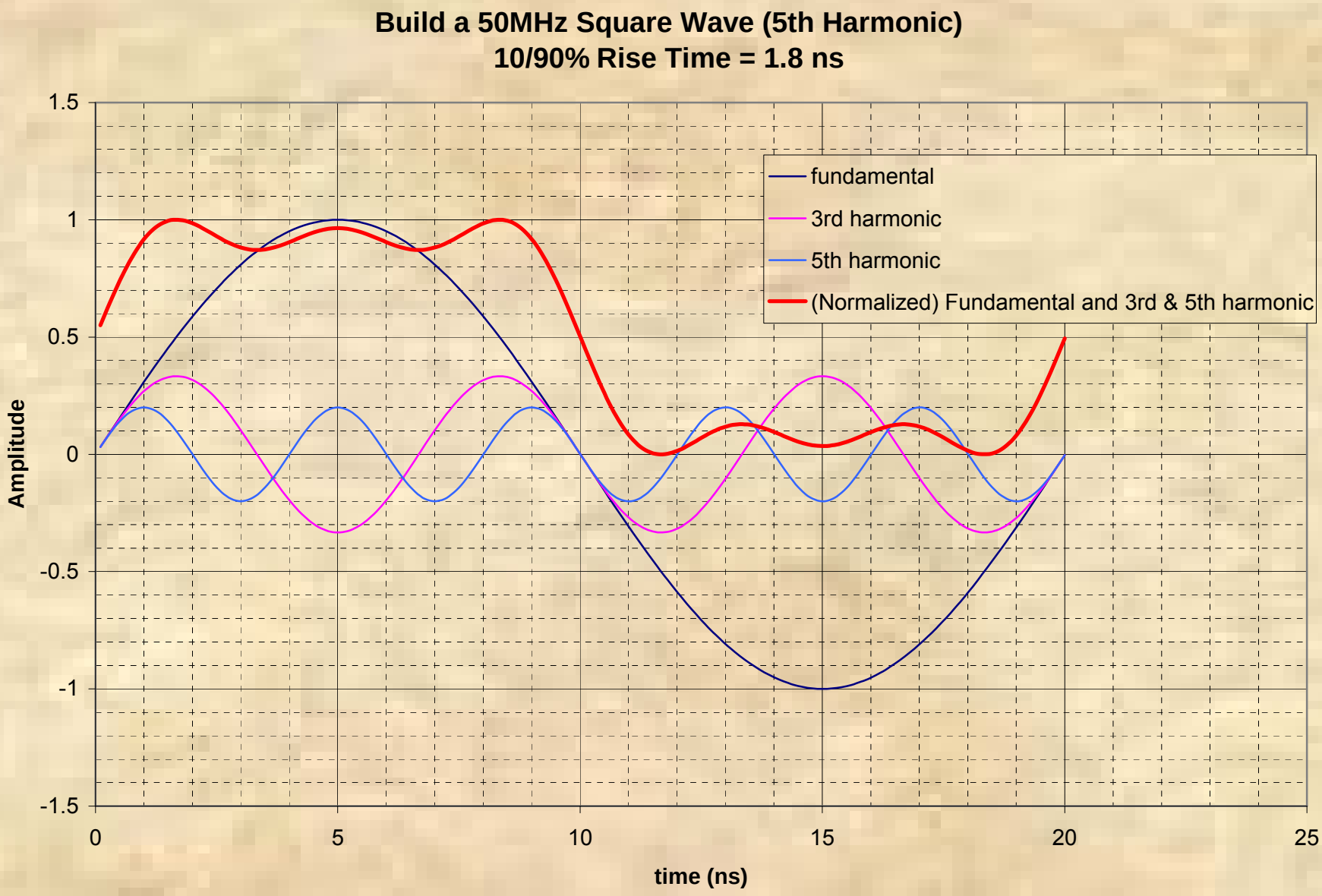


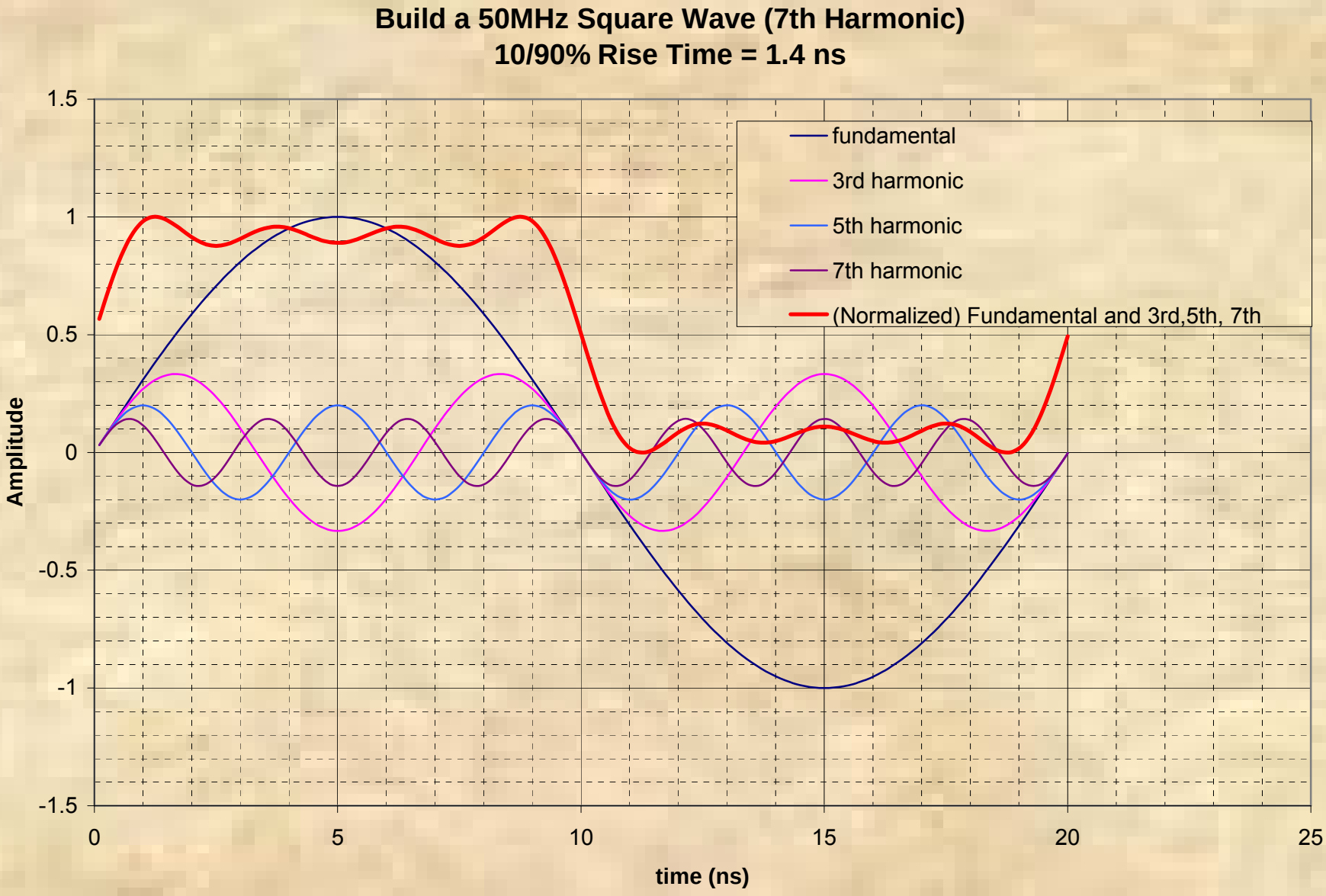
Perfect Square Wave

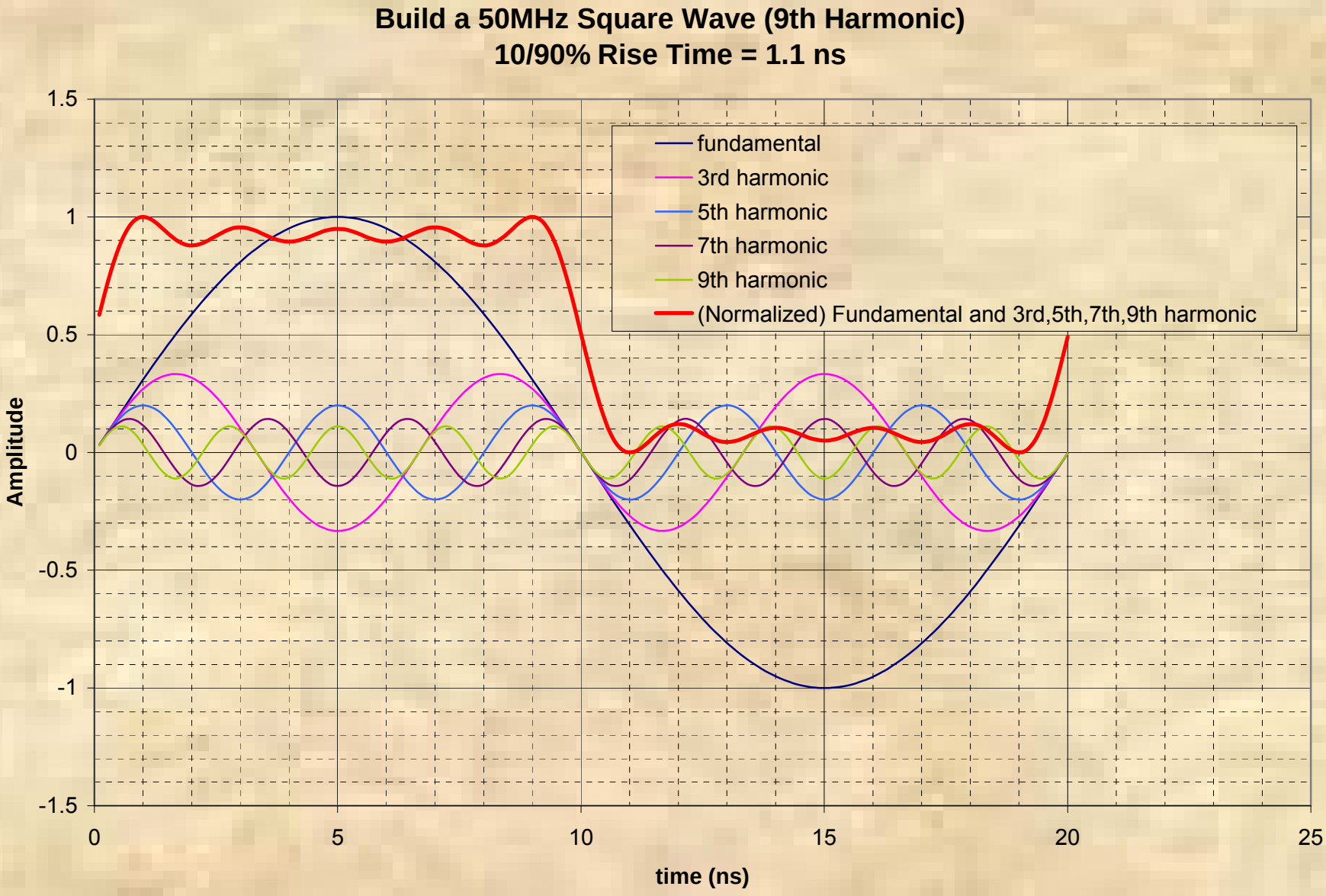
- Built from odd numbered harmonics of the fundamental frequency
- Harmonics add with 1/n relative amplitude
- Duty cycle = 50%

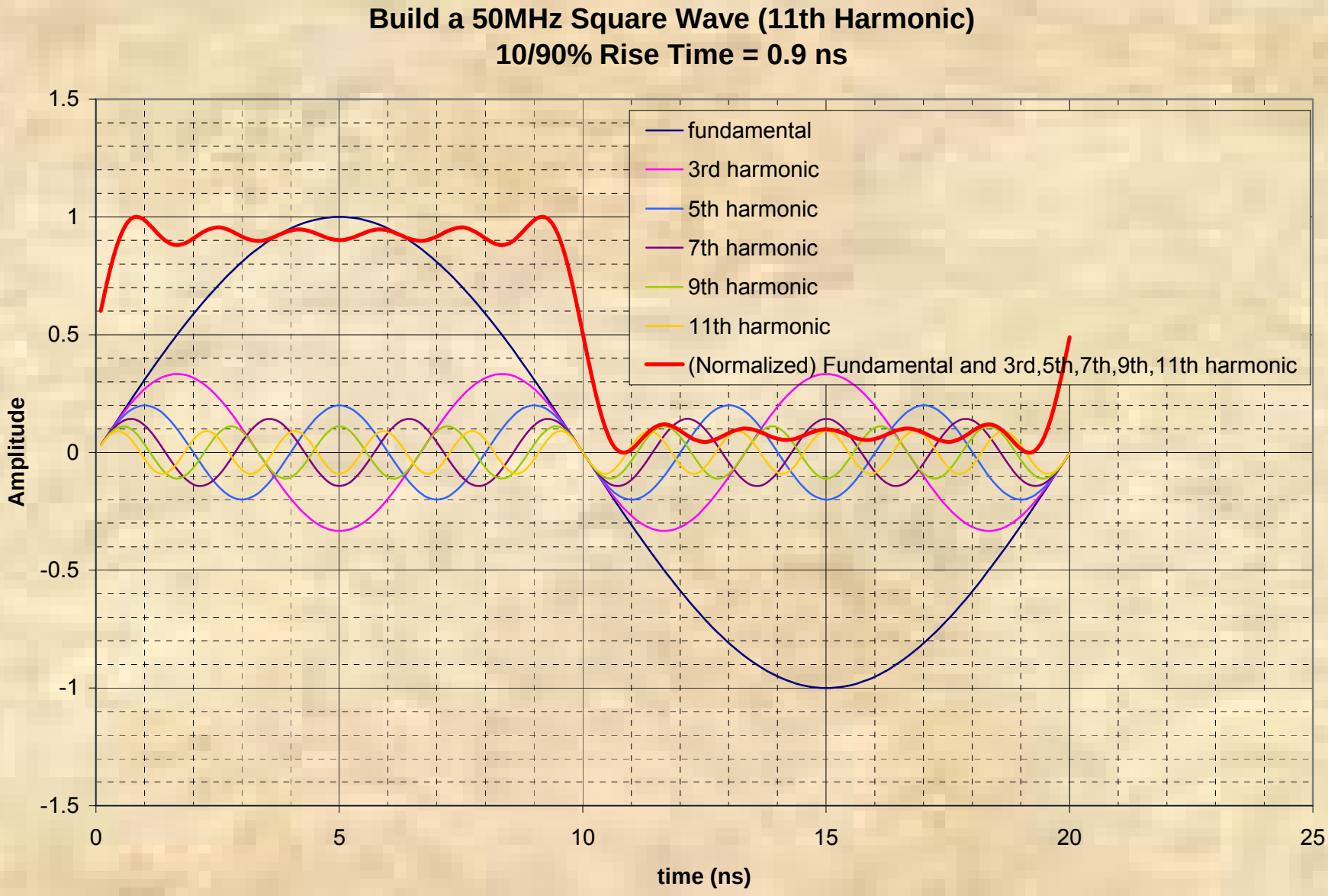

Sinewave @ 50 MHz
1.5
1
0.5
0
-0.5
-1
-1.5
Amplitude
0
5
10
15
20
25
time (ns)
fundamental

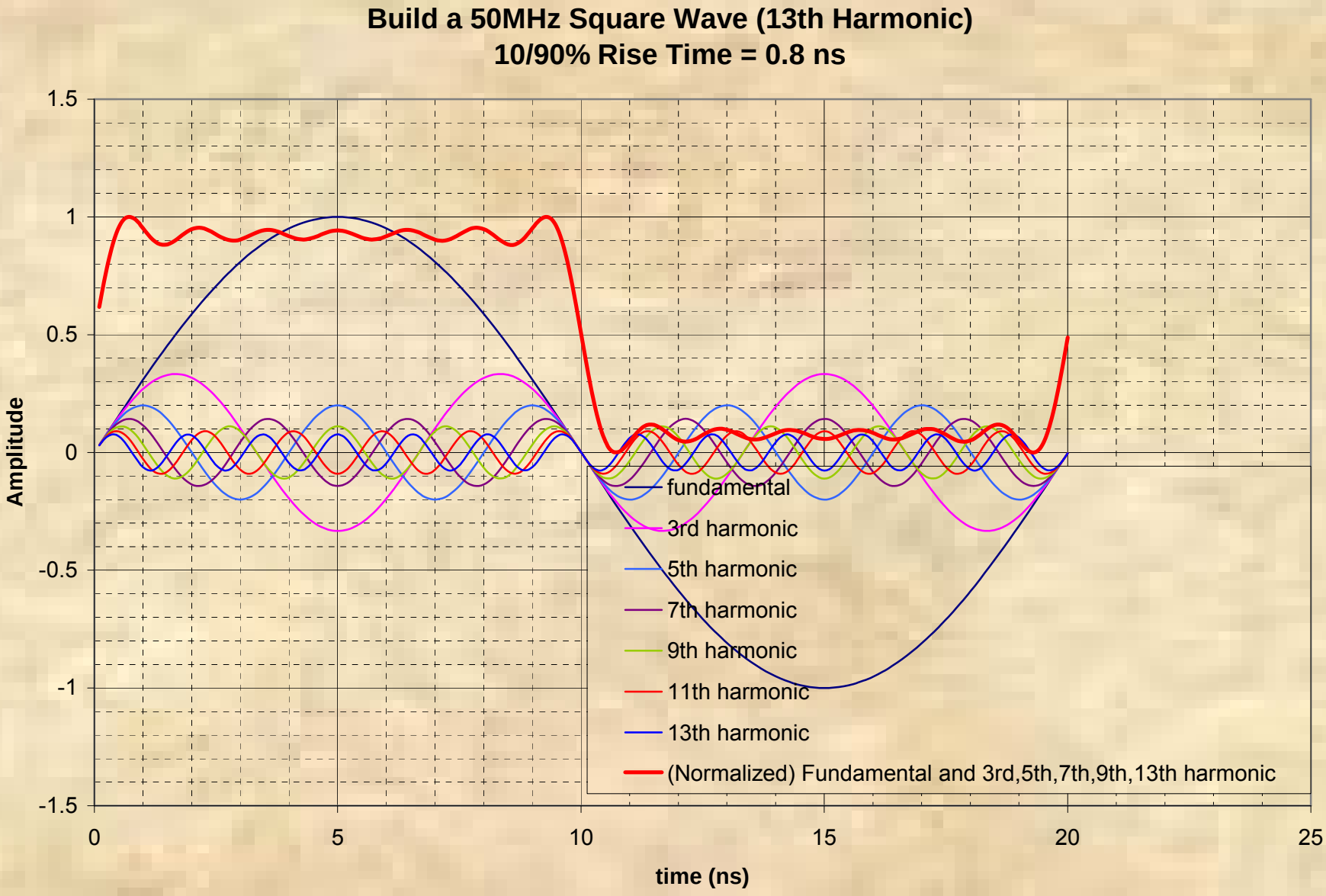

Build a 50MHz Square Wave (3rd Harmonic)
10/90% Rise Time = 2.8 ns
1.5
1
0.5
0
-0.5
-1
-1.5
Amplitude
0
5
10
15
20
25
time (ns)
fundamental
3rd harmonic
(Normalized) Fundamental and 3rd harmonic

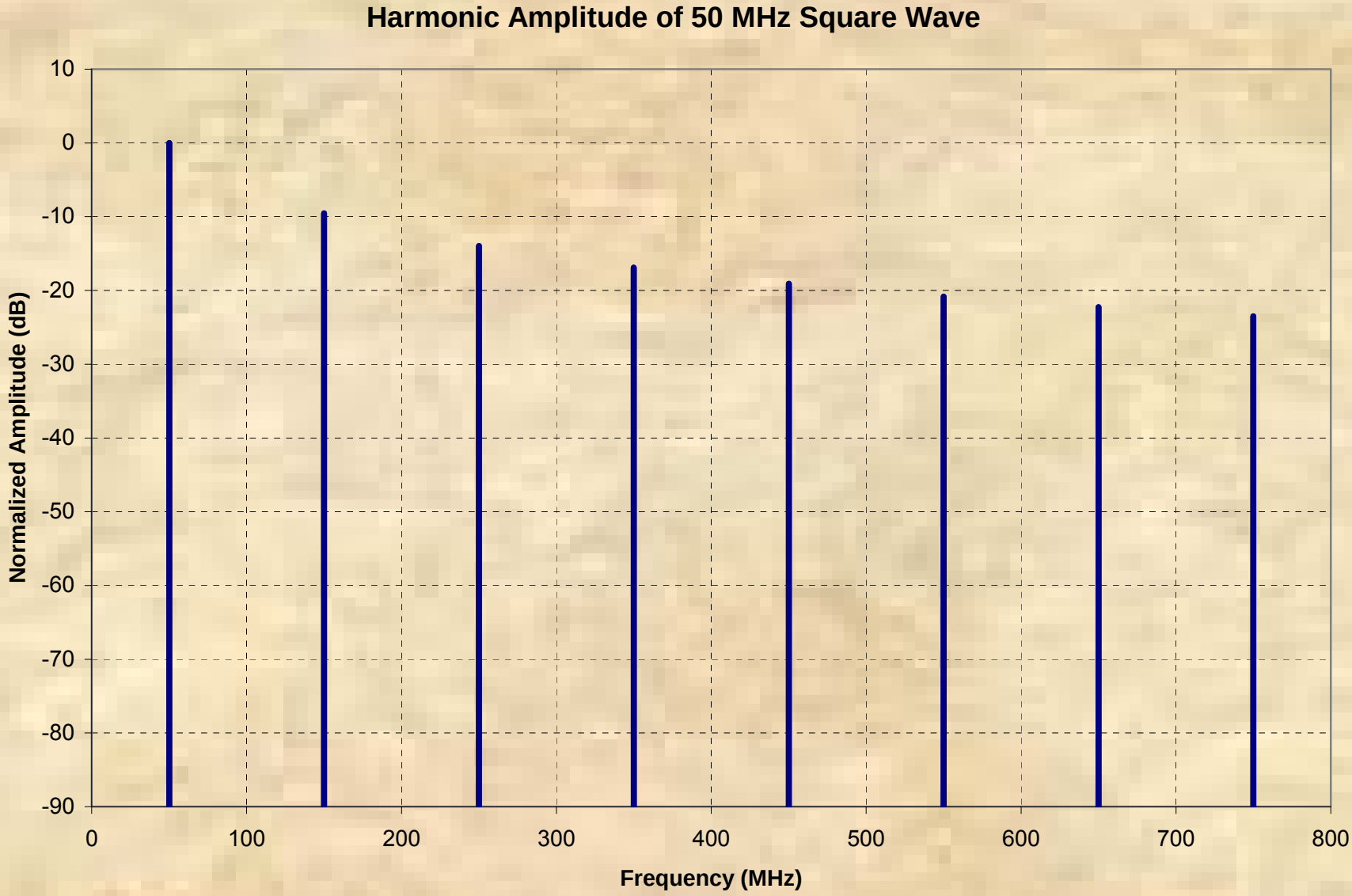

Build a 50MHz Square Wave (5th Harmonic)
10/90% Rise Time = 1.8 ns
1.5
1
0.5
0
-0.5
-1
-1.5
Amplitude
0
5
10
15
20
25
time (ns)
fundamental
3rd harmonic
5th harmonic
(Normalized) Fundamental and 3rd & 5th harmonic

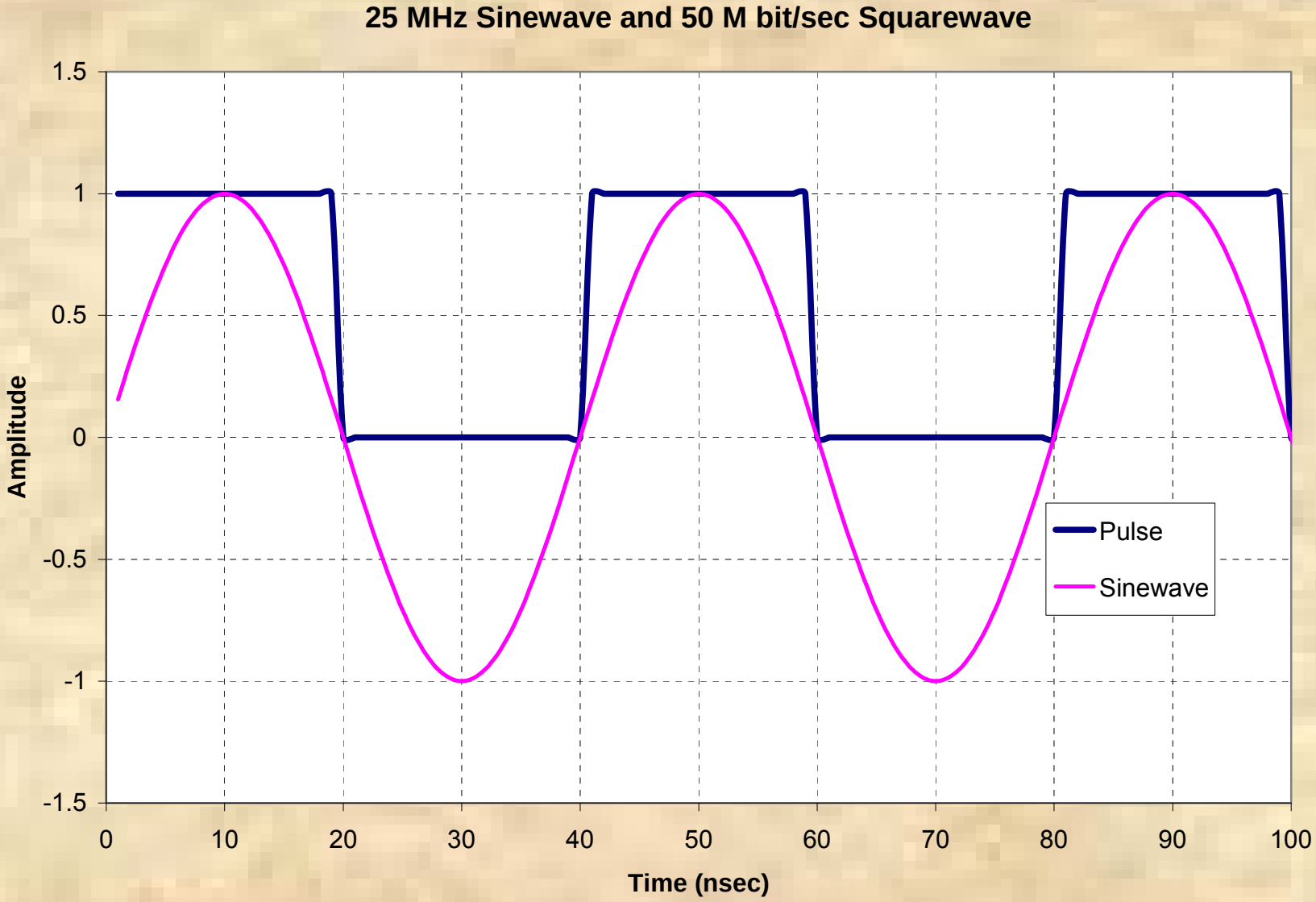

Build a 50MHz Square Wave (7th Harmonic)
10/90% Rise Time = 1.4 ns
1.5
1
0.5
0
-0.5
-1
-1.5
Amplitude
0
5
10
15
20
25
time (ns)
fundamental
3rd harmonic
5th harmonic
7th harmonic
(Normalized) Fundamental and 3rd,5th, 7th

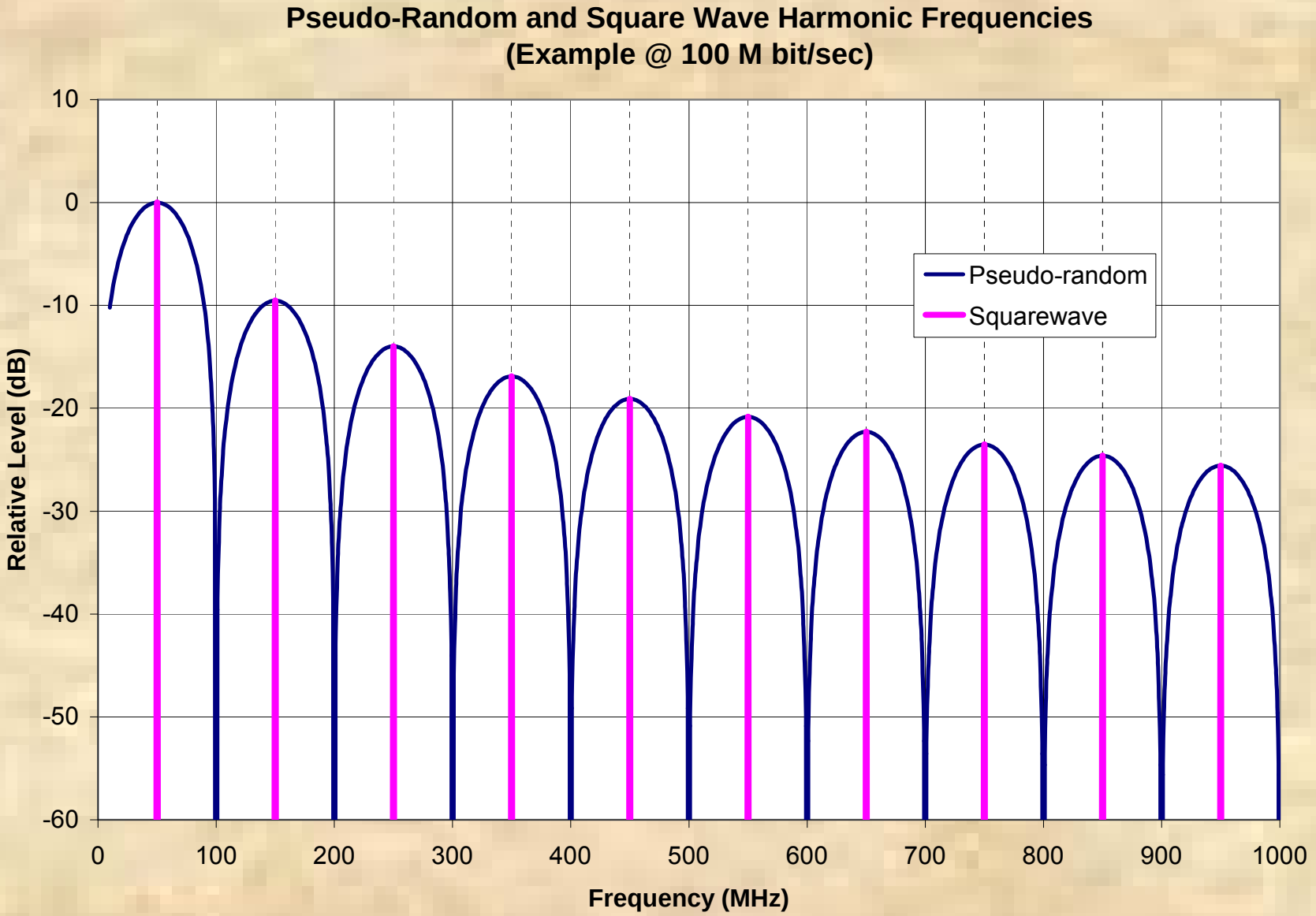

Build a 50MHz Square Wave (9th Harmonic)
10/90% Rise Time = 1.1 ns
fundamental
3rd harmonic
5th harmonic
7th harmonic
9th harmonic
(Normalized) Fundamental and 3rd,5th,7th,9th harmonic
Amplitude
time (ns)
1.5
1
0.5
0
-0.5
-1
-1.5
0
5
10
15
20
25


Build a 50MHz Square Wave (11th Harmonic)
10/90% Rise Time = 0.9 ns
fundamental
3rd harmonic
5th harmonic
7th harmonic
9th harmonic
11th harmonic
(Normalized) Fundamental and 3rd,5th,7th,9th,11th harmonic
Amplitude
time (ns)
1.5
1
0.5
0
-0.5
-1
-1.5
0
5
10
15
20
25


Build a 50MHz Square Wave (13th Harmonic)
10/90% Rise Time = 0.8 ns
Amplitude
time (ns)
1.5
1
0.5
0
-0.5
-1
-1.5
0
5
10
15
20
25
fundamental
3rd harmonic
5th harmonic
7th harmonic
9th harmonic
11th harmonic
13th harmonic
(Normalized) Fundamental and 3rd,5th,7th,9th,13th harmonic


Harmonic Amplitude of 50 MHz Square Wave
Normalized Amplitude (dB)
10
0
-10
-20
-30
-40
-50
-60
-70
-80
-90
0
100
200
300
400
500
600
700
800
Frequency (MHz)


25 MHz Sinewave and 50 M bit/sec Squarewave
1.5
1
0.5
0
-0.5
-1
-1.5
Amplitude
0
10
20
30
40
50
60
70
80
90
100
Time (nsec)
Pulse
Sinewave


Pseudo-Random and Square Wave Harmonic Frequencies
(Example @ 100 M bit/sec)
Relative Level (dB)
10
0
-10
-20
-30
-40
-50
-60
0
100
200
300
400
500
600
700
800
900
1000
Frequency (MHz)
Pseudo-random
Squarewave

Non-Perfect Waveforms

- Even harmonics appear with duty cycle not exactly 50%
- Even harmonics appear with rise/fall time unbalance
- Overshoot/undershoot causes additional harmonics

Field Propagation Speed

- Depends on
  - Permittivity (dielectric) ε
  - Permeability (magnetic) μ
- Free Space
  - Speed of Light c
  - 3 x 10^8 meters/second

$$c = \frac{1}{\sqrt{\varepsilon_0 \, \mu_0}}$$

$$v_p = \frac{c}{\sqrt{\varepsilon \, \mu}}$$

Wavelength

- Length of wave in free space (or other media)

$$\lambda = v_p / f$$

Examples (in air):

Wavelength = 1 meter @ 300MHz

Wavelength = 30 cm @ 1 GHz

Wavelength = 3 cm @ 10 GHz

Derivative

- How fast is *something* changing?

$$\frac{d}{dt}[something]$$

Changing with respect to time

$$\frac{d}{dx}[something]$$

Changing with respect to position (x)

Partial Derivative

- How fast is *something* changing for one variable?

$$\frac{\partial}{\partial t}\left[something\,(t,x)\right]$$

Changing with respect to time (as 'x' is constant)

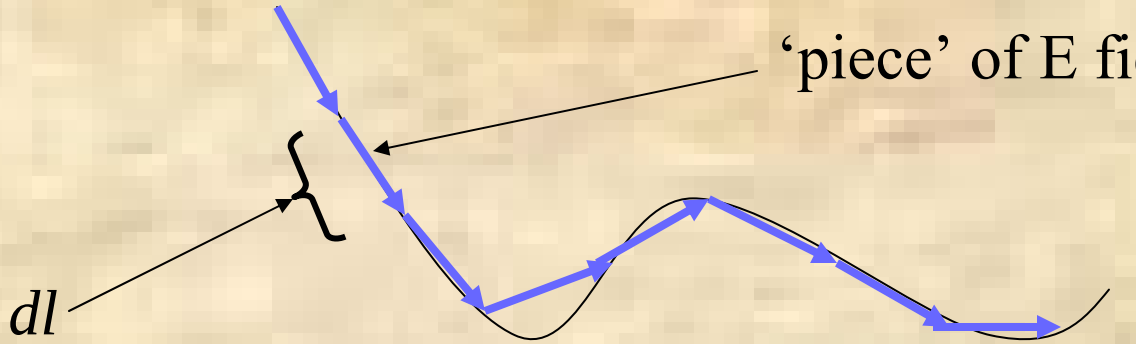
$$\frac{\partial}{\partial x}\left[something\,(t,x)\right]$$

Changing with respect to position (x) (as time is constant)

Integration

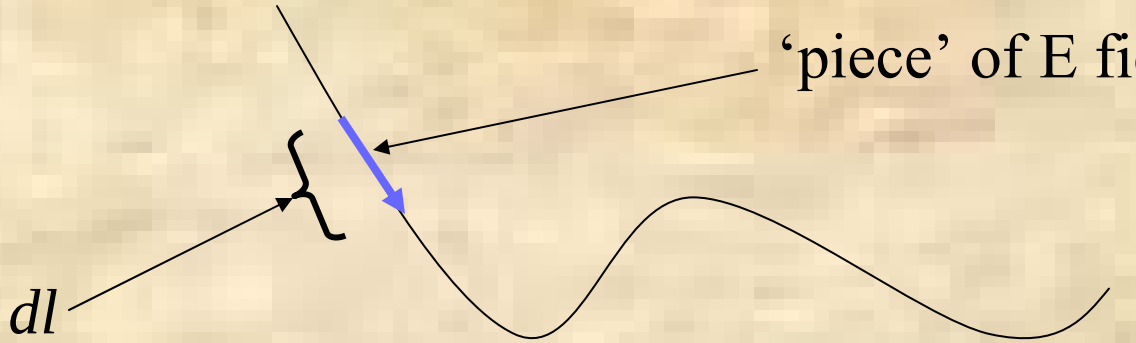
- Simply the sum of parts (when the parts are very small)
  - Line Integral --- sum of small line segments
  - Surface Integral -- sum of small surface patches
  - Volume Integral -- sum of small volume blocks

Line Integral
(find the length of the path)



$$V = -\int_{start}^{stop} (\vec{E} \bullet dl)$$

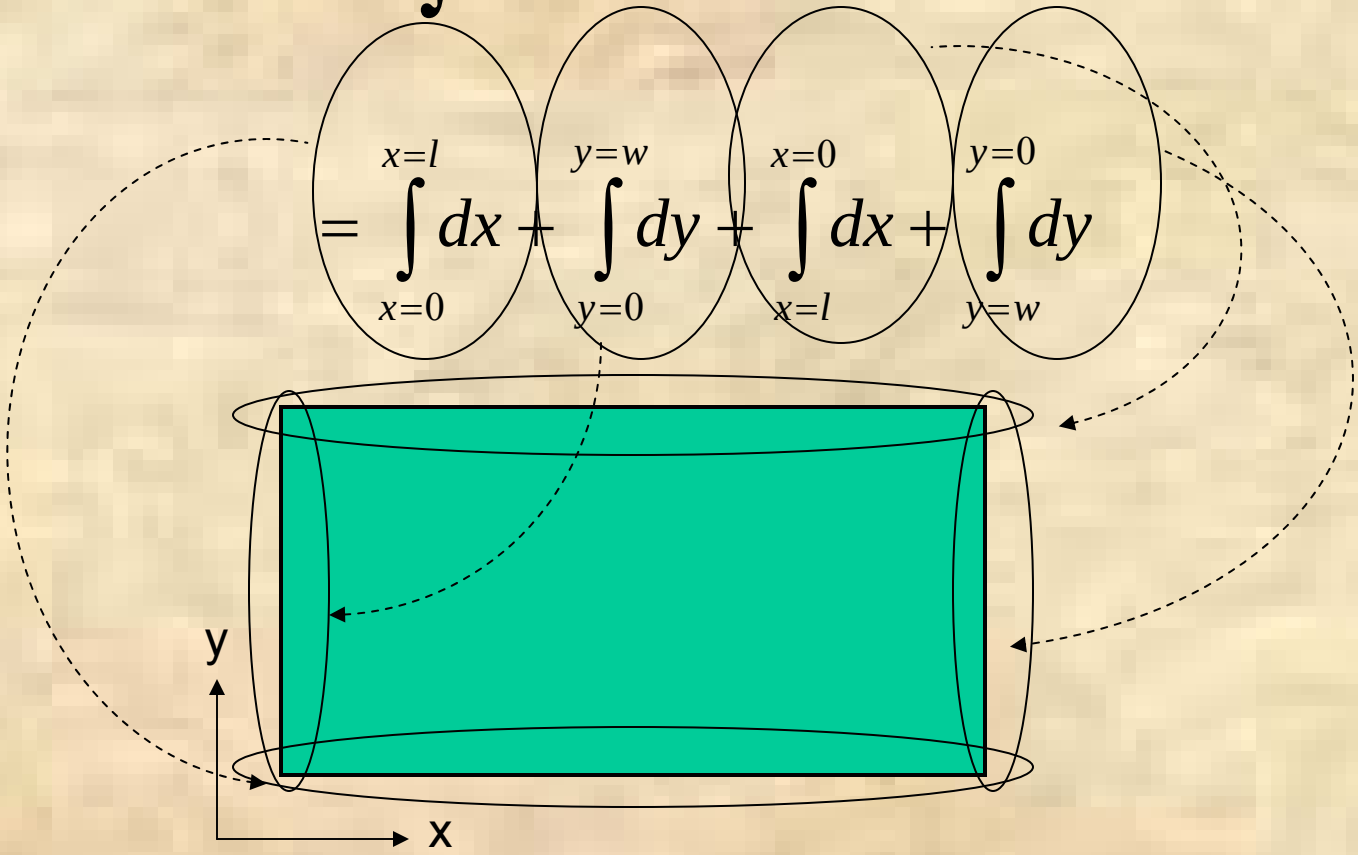
Line Integral



$$V = -\int_{start}^{stop} \left[\; (E_x * dx) + (E_y * dy) \; \right]$$

Line Integral -- Closed

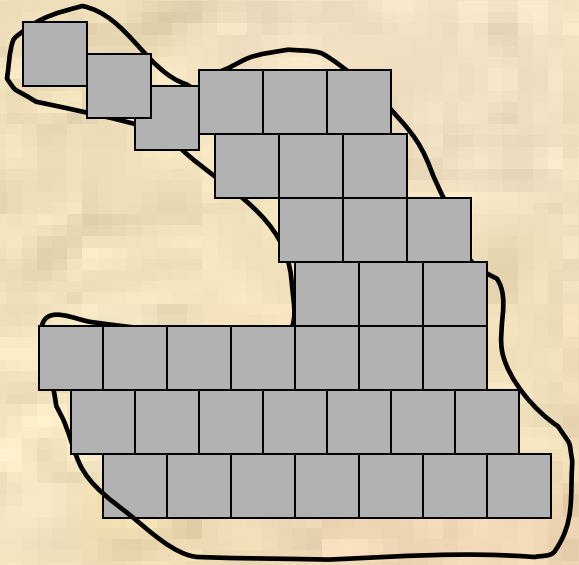
Circumference $= \oint$ *path around box*



Line Integral -- Closed

- Closed line integrals find the path length
- And/or the amount of some quantity along that closed path length

Surface Integral
(find the area of the surface)



$$Area = \int da$$

$$da = dx * dy$$

$$Area = \iint dx * dy$$

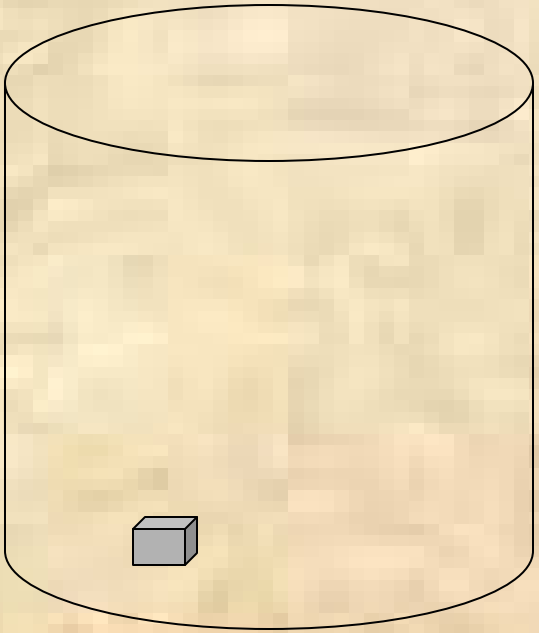
As *dx* and *dy* become smaller and smaller, the area is better calculated

Closed Surface Integral

- Find the surface area of a closed shape

$$\oiint shape\ da$$

Volume Integral
(find the volume of an object)



$$Volume = \int dv$$

$$dv = dx * dy * dz$$

$$Volume = \iiint [dx * dy * dz]$$

From Math to Electromagnetics

Electromagnetics

In the Beginning

- Electric and Magnetic effects not connected
- Electric and magnetic effects were due to 'action from a distance'
- Faraday was the 1st to propose a relationship between electric lines of force and time-changing magnetic fields
  - Faraday was very good at experiments and 'figuring out' how things work

Maxwell

- Discovered the link between the “electro” and the “magnetic”
- Scotland’s greatest contribution to the world next to Scotch
- Maxwell, Heaviside and Hertz

Maxwell's Equations are NOT Hard!

$$\nabla \times H = J + \frac{\partial D}{\partial t}$$

$$\nabla \times E = -\frac{\partial B}{\partial t}$$

Maxwell's Equations – Differential Form

A difference in Magnetic Field across a small piece of space

A change in Electric Flux Density with respect to time

$$\nabla \times H = J + \frac{\partial D}{\partial t}$$

A difference in Electric Field across a small piece of space

$$\nabla \times E = -\frac{\partial B}{\partial t}$$

A change in Magnetic Flux Density with respect to time

Maxwell's Equations are not Hard!

- Change in H-field across space ≈ Change in E-field (at that point) with time
- Change in E-field across space ≈ Change in H-field (at that point) with time
- (Roughly speaking, and ignoring constants)

Other Famous Equations

- Faraday's Law
- Gauss' Law
- Ampere's Law
- Stokes Theorem
- Many others

Near Field vs. Far Field

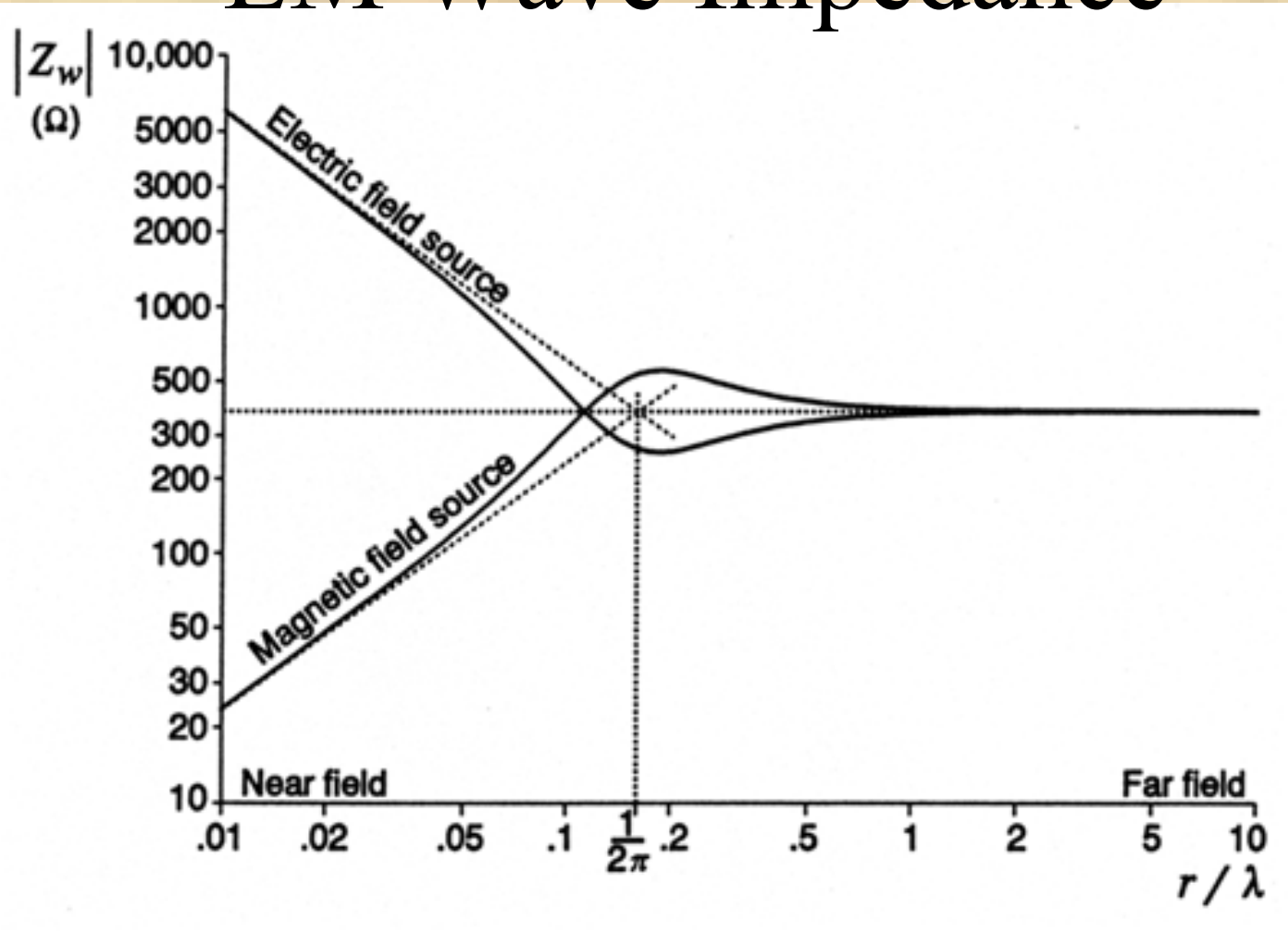
- Distance / Frequency
- Source Size
- Transition Distance Depends On Magnitude Of Error Allowed
- If Truly Far-Field Then Source Can Usually Be Modeled Simply
- Equations and Graphs Assume Far-Field Simplified Case
- Real Life Problems Are Seldom Simple Due to Multiple Effects

In the Far Field

$$Z = \frac{\vec{E}}{\vec{H}} = 377 ohms$$

- Electric field source (dipole, etc) has high impedance near to the source
- Magnetic field source (loop, etc) has low impedance near to the source

EM Wave Impedance



Important Concepts for Effective PCB Design

- Design intentionally
- Pass the first time!

Skin Depth

- Current flows only near surface at high frequencies

$$\delta = \frac{1}{\sqrt{\pi f \mu \sigma}}$$

Frequency	Skin Depth	Skin Depth
60 Hz	260 mils	8.5 mm
1 KHz	82 mils	2.09 mm
10 KHz	26 mils	0.66 mm
100 KHz	8.2 mils	0.21 mm
1 MHz	2.6 mils	0.066 mm
10 MHz	0.82 mils	0.021 mm
100 MHz	0.26 mils	0.0066 mm
1 GHz	0.0823 mils	0.0021 mm

Current Migrates to Outer Portions of the Conductor at High Frequencies

Resistance is determined by the area of the copper conductor actually used at each frequency!

At High Frequencies

- Resistive loss and dielectric loss are present
- Inductance will usually dominate

Inductance

- Current flow through metal = inductance!
- Fundamental element in EVERYTHING
- Loop area first order concern
- Inductive impedance increases with frequency and is MAJOR concern at high frequencies

$$X_L = 2\pi fL$$

Current Loop = Inductance

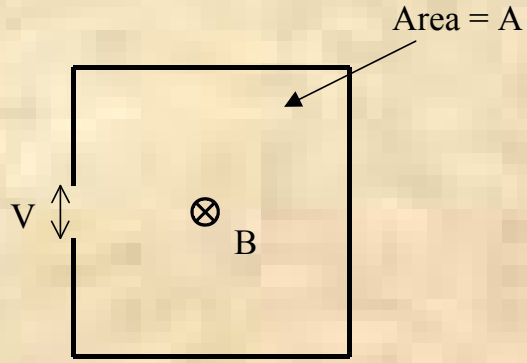
Courtesy of Elya Joffe

Inductance Definition

- Faraday's Law

$$\oint \bar{E} \cdot dl = -\iint \frac{\partial \bar{B}}{\partial t} \cdot d\bar{S}$$

- For a simple rectangular loop



$$V = -A\frac{\partial B}{\partial t}$$

Self Inductance

- Isolated circular loop

$$L \approx \mu_0 a\left(\ln\frac{8a}{r_0} - 2\right)$$

- Isolated rectangular loop

$$L = \frac{2\mu_0 a}{\pi}\left(\ln\frac{p+\sqrt{1+p^2}}{1+\sqrt{2}} + \frac{1}{p} - 1 + \sqrt{2} - \frac{1}{p}\sqrt{1+p^2}\right)$$

Note that inductance is directly influenced by loop ***AREA*** and less influenced by conductor size!

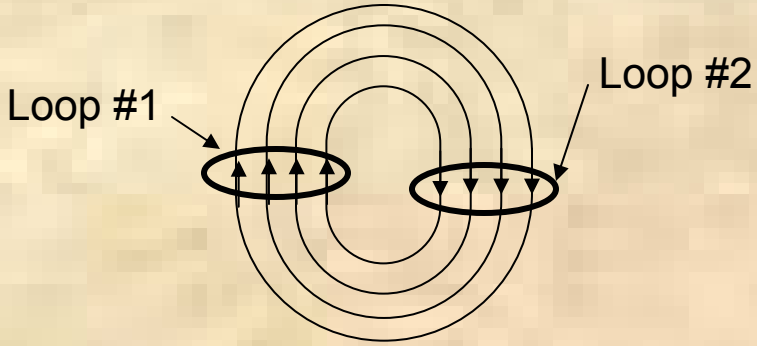
$$p = \frac{length\ of\ \ side}{wire\ radius}$$

Mutual Inductance

$$\Phi_2 = M_{21} I_1$$

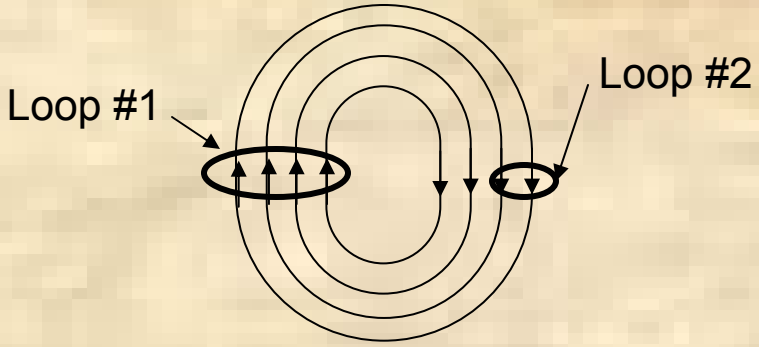
$$M_{21} = \frac{\Phi_2}{I_1}$$

How much magnetic flux is induced in loop #2 from a current in loop #1?

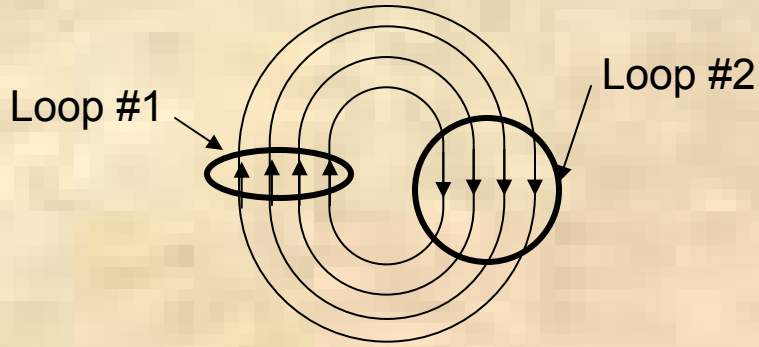


$$\Phi_2 = \int_{S_2} \vec{B}_1(r) \cdot \hat{n}\, dS_2$$

Mutual Inductance



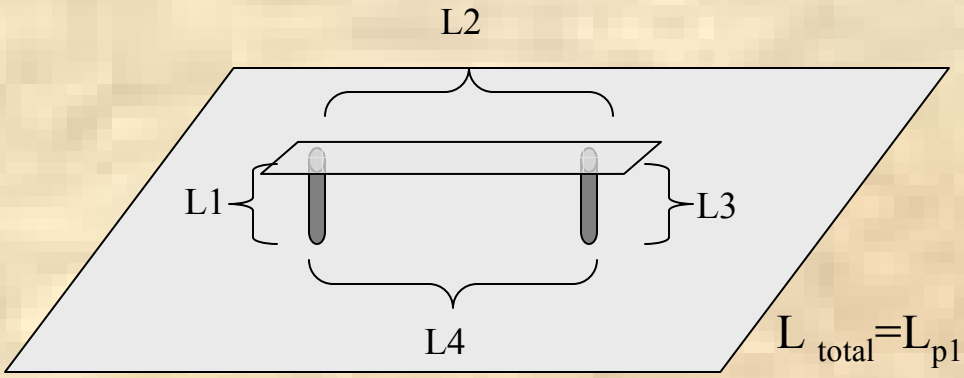
Less loop area in loop #2 means less magnetic flux in loop #2 and less mutual inductance



Less loop area perpendicular to the magnetic field in loop #2 means less magnetic flux in loop #2 and less mutual inductance

Partial Inductance

- Simply a way to break the overall loop into pieces in order to find total inductance



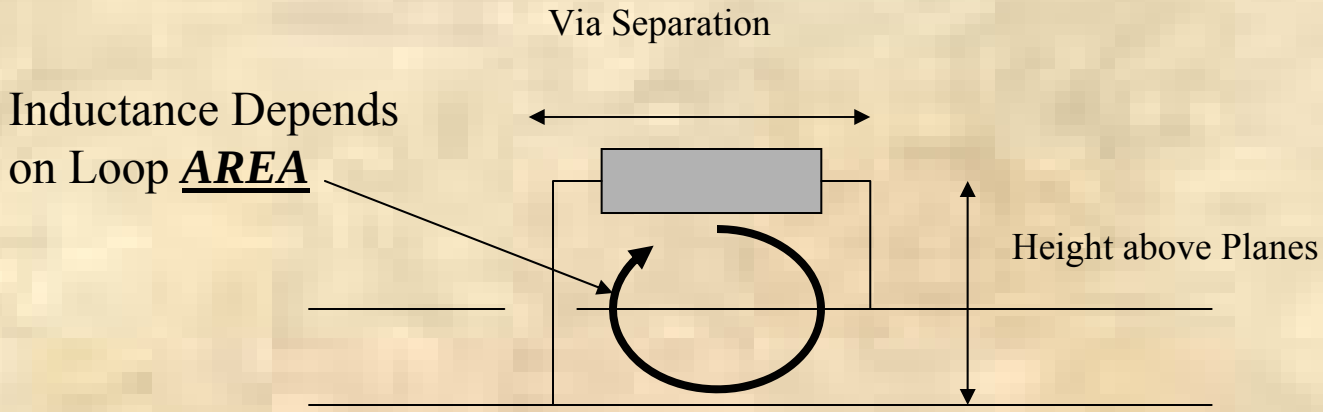
$$L_{total} = L_{p11} + L_{p22} + L_{p33} + L_{p44} - 2L_{p13} - 2L_{p24}$$

Important Points About Inductance

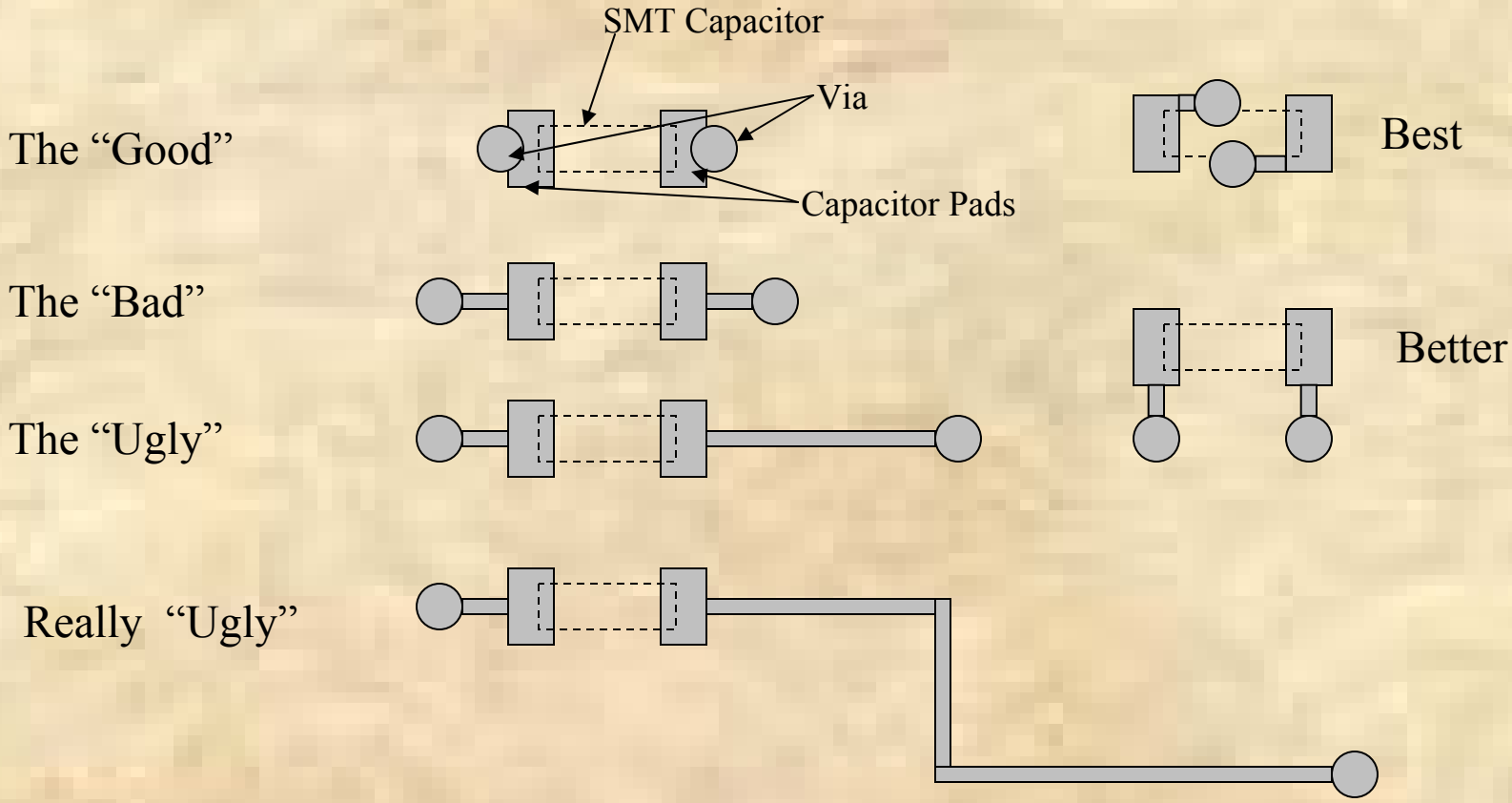
- Inductance is everywhere
- Loop area most important
- Inductance is everywhere

Example
Decoupling Capacitor Mounting

- **Keep vias as close to capacitor pads as possible!**



Via Configuration Can Change Inductance



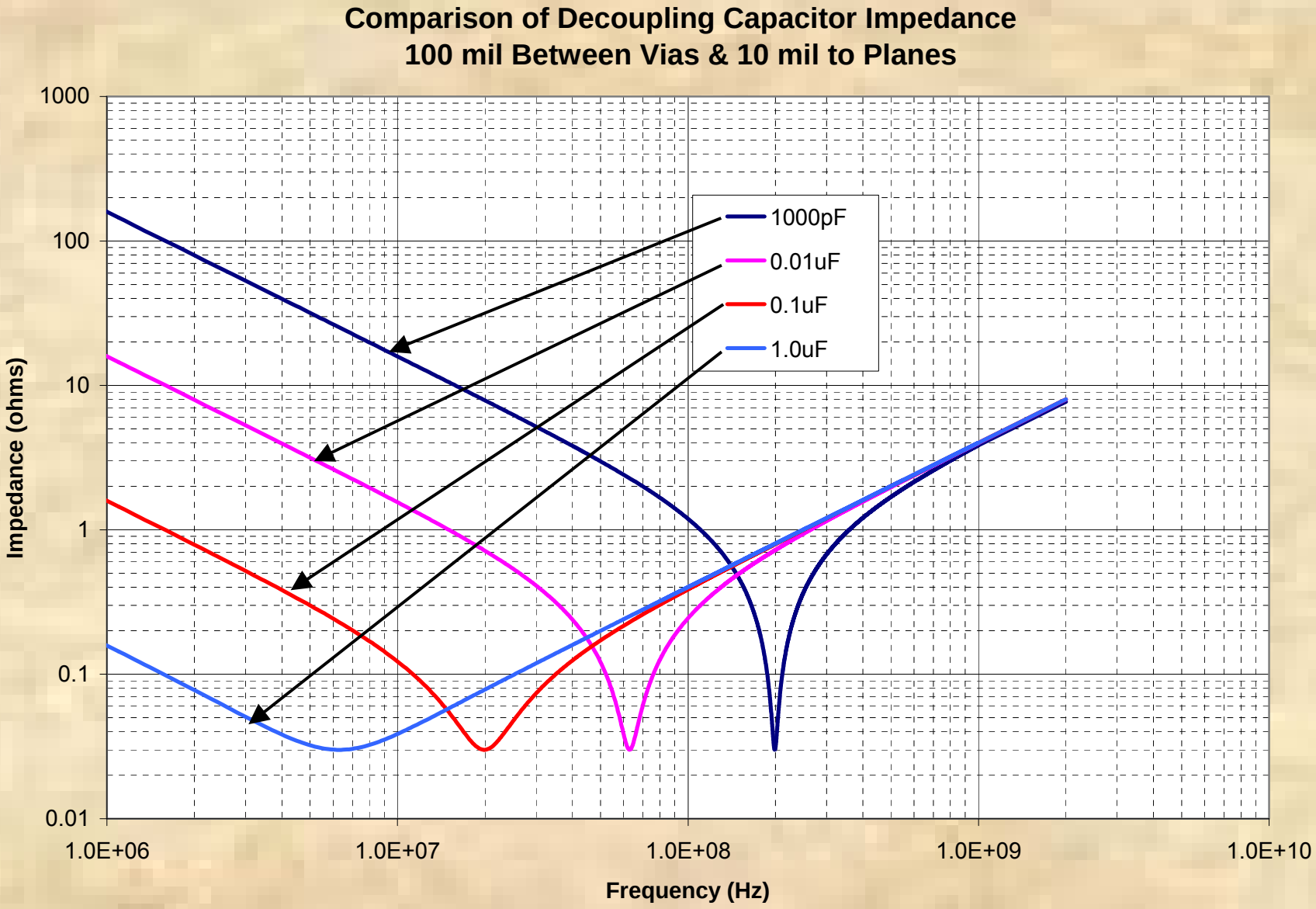
What is Capacitance?

$$C = \frac{Q}{V} \qquad Q = CV$$

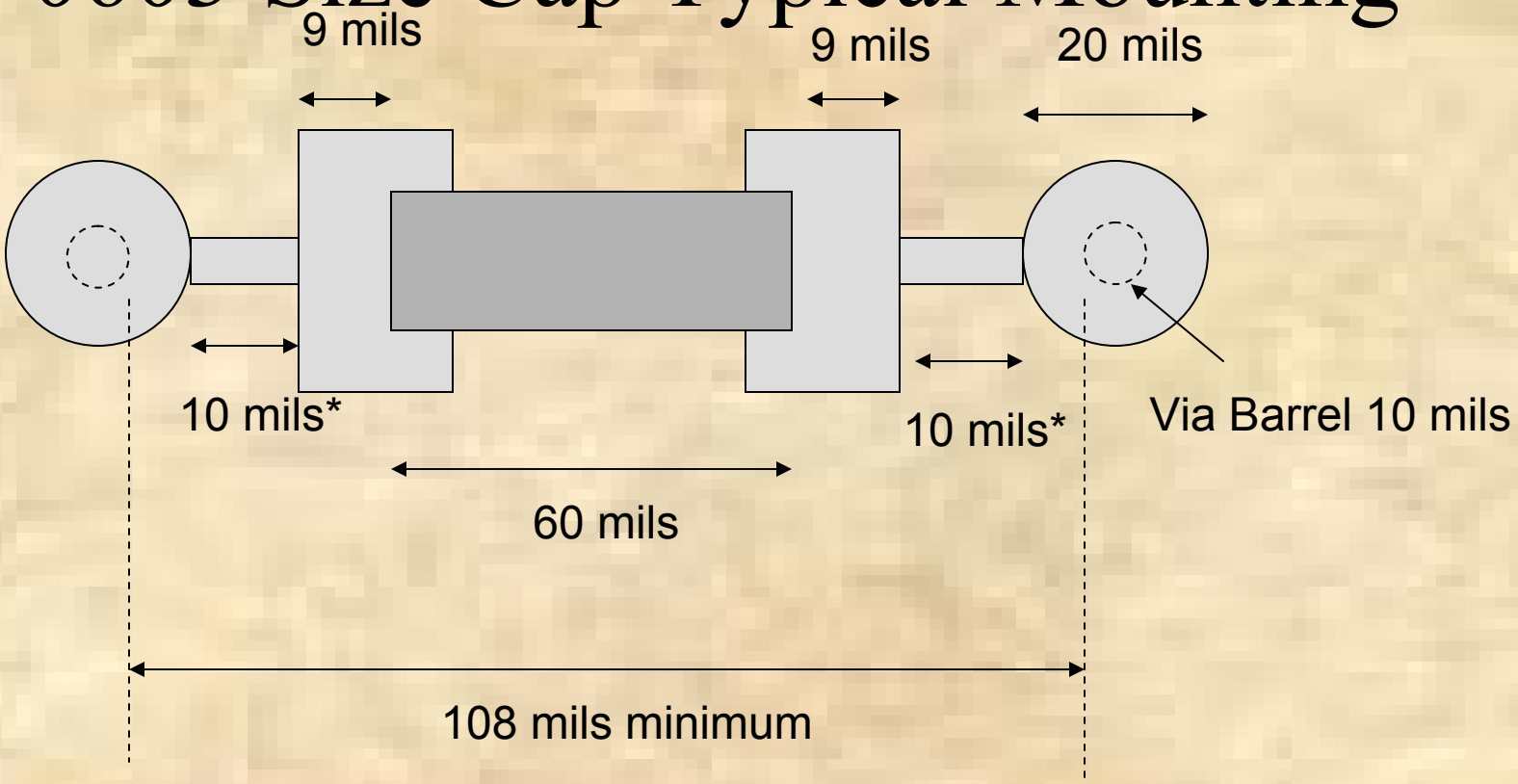
- Capacitance is the ability of a structure to hold charge (electrons) for a given voltage
- Amount of charge stored is dependant on the size of the capacitance (and voltage)

High Frequency Capacitors

- Myth or Fact?

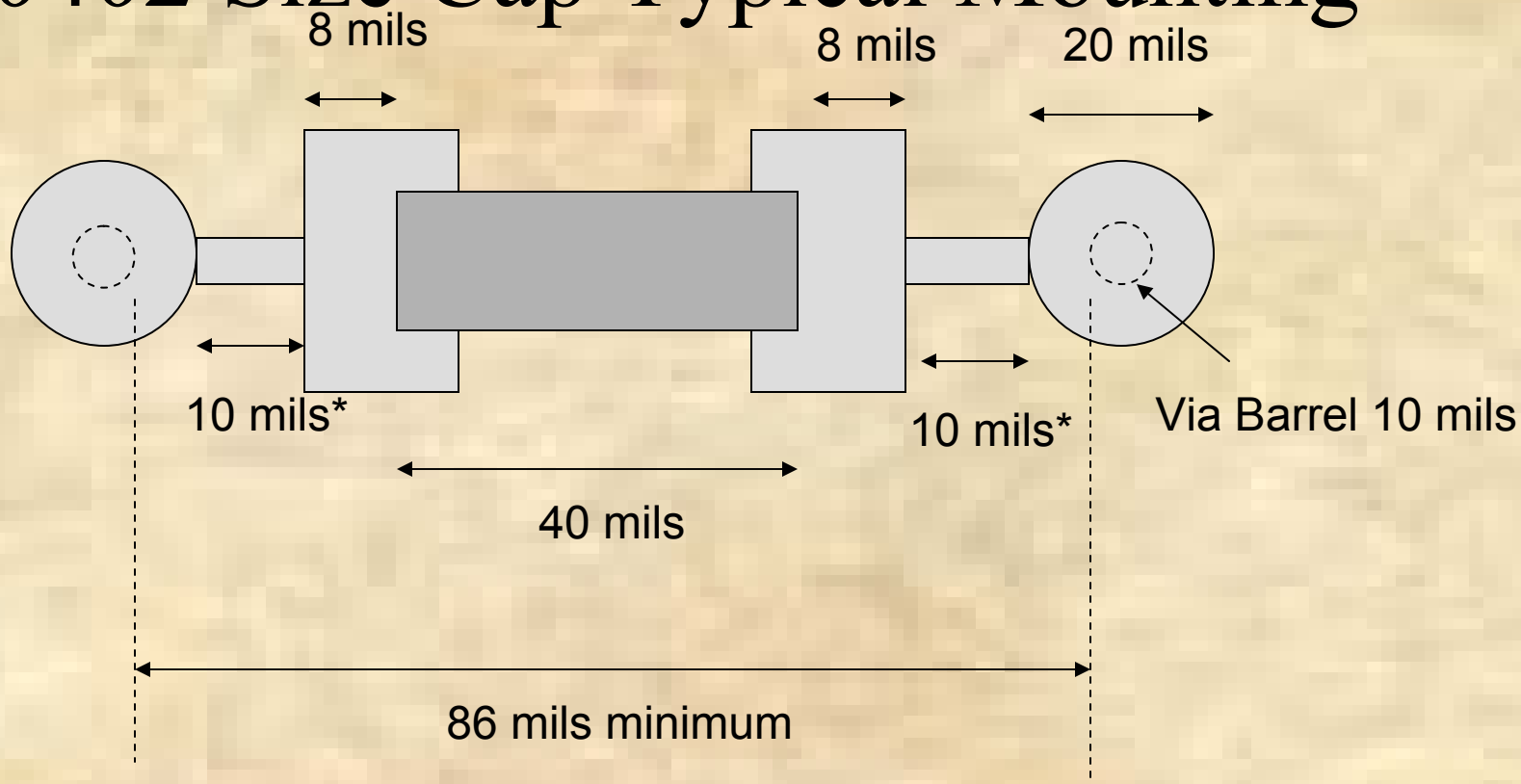

Comparison of Decoupling Capacitor Impedance
100 mil Between Vias & 10 mil to Planes
Impedance (ohms)
1000
100
10
1
0.1
0.01
1.0E+06
1.0E+07
1.0E+08
1.0E+09
1.0E+10
Frequency (Hz)
1000pF
0.01uF
0.1uF
1.0uF

0603 Size Cap Typical Mounting



*Note: Minimum distance is 10 mils but more typical distance is 20 mils

0402 Size Cap Typical Mounting



*Note: Minimum distance is 10 mils but more typical distance is 20 mils

Connection Inductance for Typical Capacitor Configurations

Distance into board to planes (mils)	0805 typical/minimum (148 mils between via barrels)	0603 typical/minimum (128 mils between via barrels)	0402 typical/minimum (106 mils between via barrels)
10	1.2 nH	1.1 nH	0.9 nH
20	1.8 nH	1.6 nH	1.3 nH
30	2.2 nH	1.9 nH	1.6 nH
40	2.5 nH	2.2 nH	1.9 nH
50	2.8 nH	2.5 nH	2.1 nH
60	3.1 nH	2.7 nH	2.3 nH
70	3.4 nH	3.0 nH	2.6 nH
80	3.6 nH	3.2 nH	2.8 nH
90	3.9 nH	3.5 nH	3.0 nH
100	4.2 nH	3.7 nH	3.2 nH

Connection Inductance for Typical Capacitor Configurations with 50 mils from Capacitor Pad to Via Pad

Distance into board to planes (mils)	0805 (208 mils between via barrels)	0603 (188 mils between via barrels)	0402 (166 mils between via barrels)
10	1.7 nH	1.6 nH	1.4 nH
20	2.5 nH	2.3 nH	2.0 nH
30	3.0 nH	2.8 nH	2.5 nH
40	3.5 nH	3.2 nH	2.8 nH
50	3.9 nH	3.5 nH	3.1 nH
60	4.2 nH	3.9 nH	3.5 nH
70	4.5 nH	4.2 nH	3.7 nH
80	4.9 nH	4.5 nH	4.0 nH
90	5.2 nH	4.7 nH	4.3 nH
100	5.5 nH	5.0 nH	4.6 nH

EM Summary

- Electromagnetics is not hard
  - Must get past the messy math
- Understanding what the basic equations mean is important
- ***CURRENT*** is important
- "Ground" is a place for potatoes and carrots!
- Where does the return current flow?
  - #1 cause of EMC related problems

PCB Design for EMI Control

- Design decisions *WILL* affect EMI emissions as well as internal system interoperability
- Thinking about signals/currents will help make the right choice!

THINK

- Not here to give list of rules, or “do’s” and “don’ts”
- UNDERSTAND WHY
- NO MAGIC!

No Longer Separate!

- Signal Integrity
- Functionality
- EMC
  - Emissions
  - Susceptibility

‘Ground’

- **Ground is a place where potatoes and carrots thrive!**
- ‘Earth’ or ‘reference’ is more descriptive
- Original use of “GROUND”
- Inductance is everywhere

$$X_L = 2\pi f L$$

What we Really Mean when we say ‘Ground’

- Signal Reference
- Power Reference
- Safety Earth
- Chassis Shield Reference

‘Ground’ is NOT a Current Sink!

- Current leaves a driver on a trace and must return (somehow) to its source
- This seems basic, but it is often forgotten, and is most often the cause of EMC problems

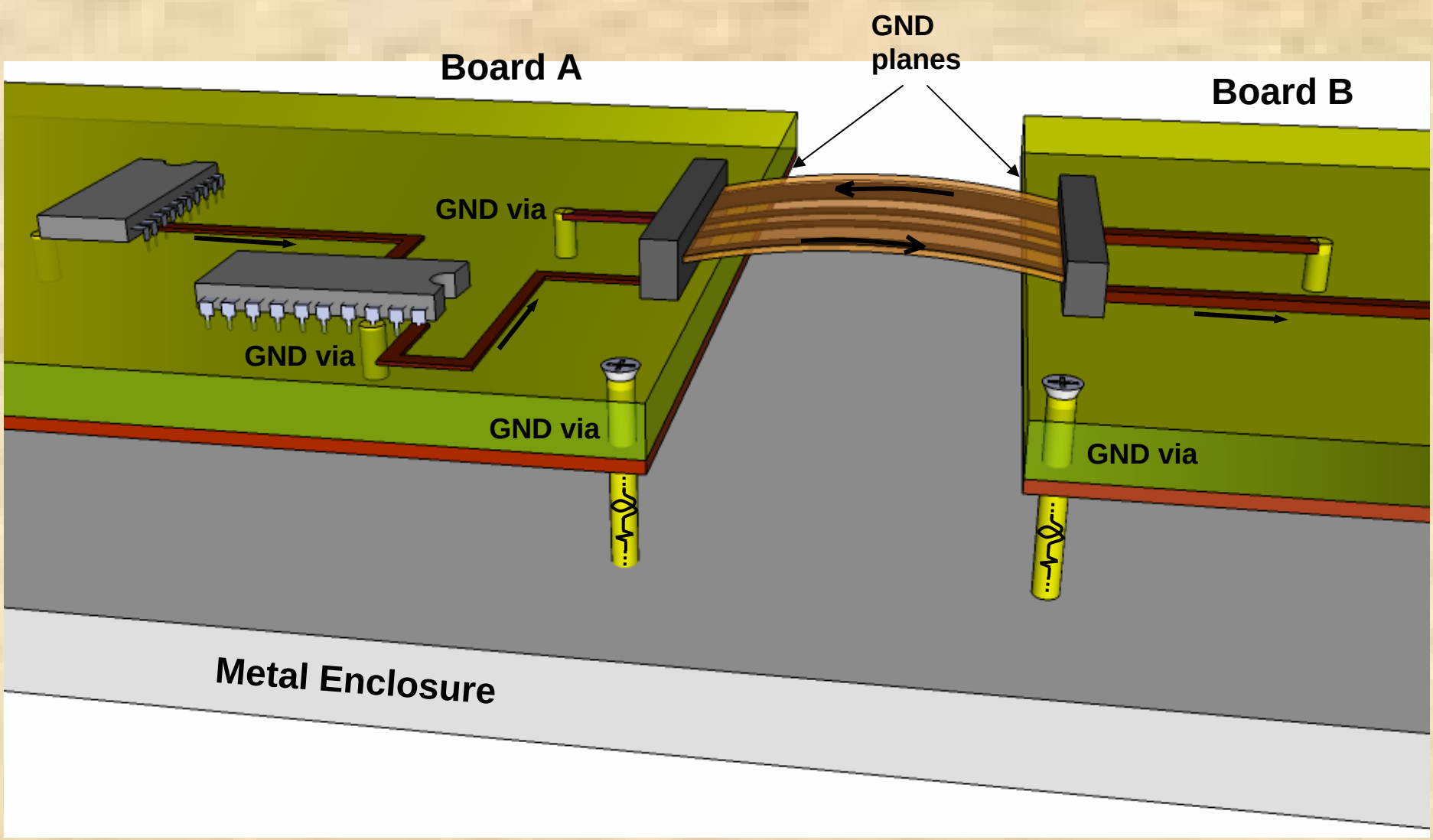
Single Point ‘Ground’ Myth

- At high frequencies, inductance makes this impossible!
- At high frequencies, parasitic capacitance makes this impossible!
- Depends on the amount of ‘Ground’ error your system can stand…..

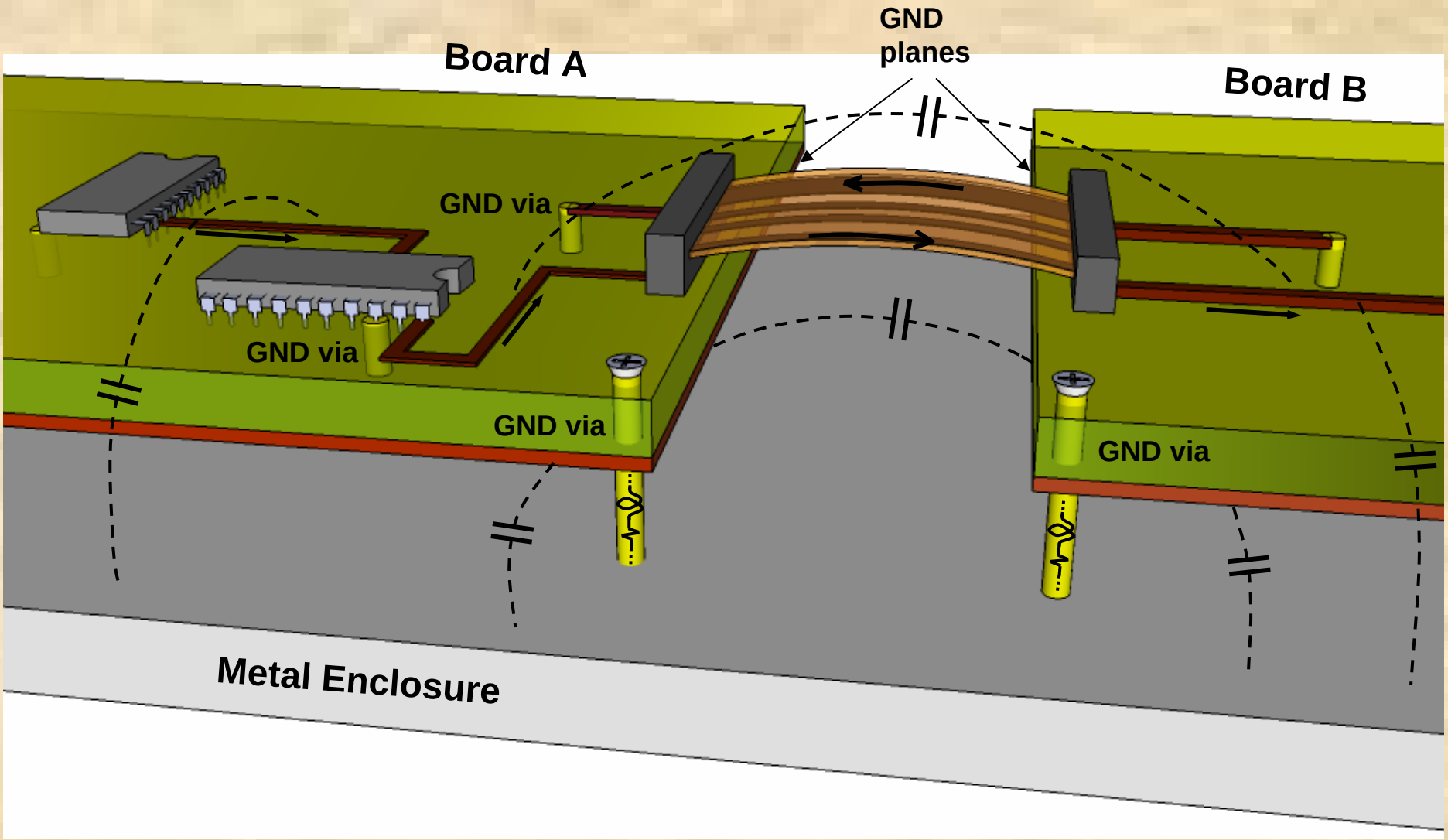
‘Grounding’ Needs Low Impedance at Highest Frequency

- Steel Reference Plate
  - 4 milliohms/sq @ 100KHz
  - 40 milliohms/sq @ 10 MHz
  - 400 milliohms/sq @ 1 GHz
- A typical via is about 2 nH
  - @ 100 MHz Z = 1.3 ohms
  - @ 500 MHz Z = 6.5 ohms
  - @ 1000 MHz Z = 13 ohms
  - @ 2000 MHz Z = 26 ohms

Single-Point Ground Concept

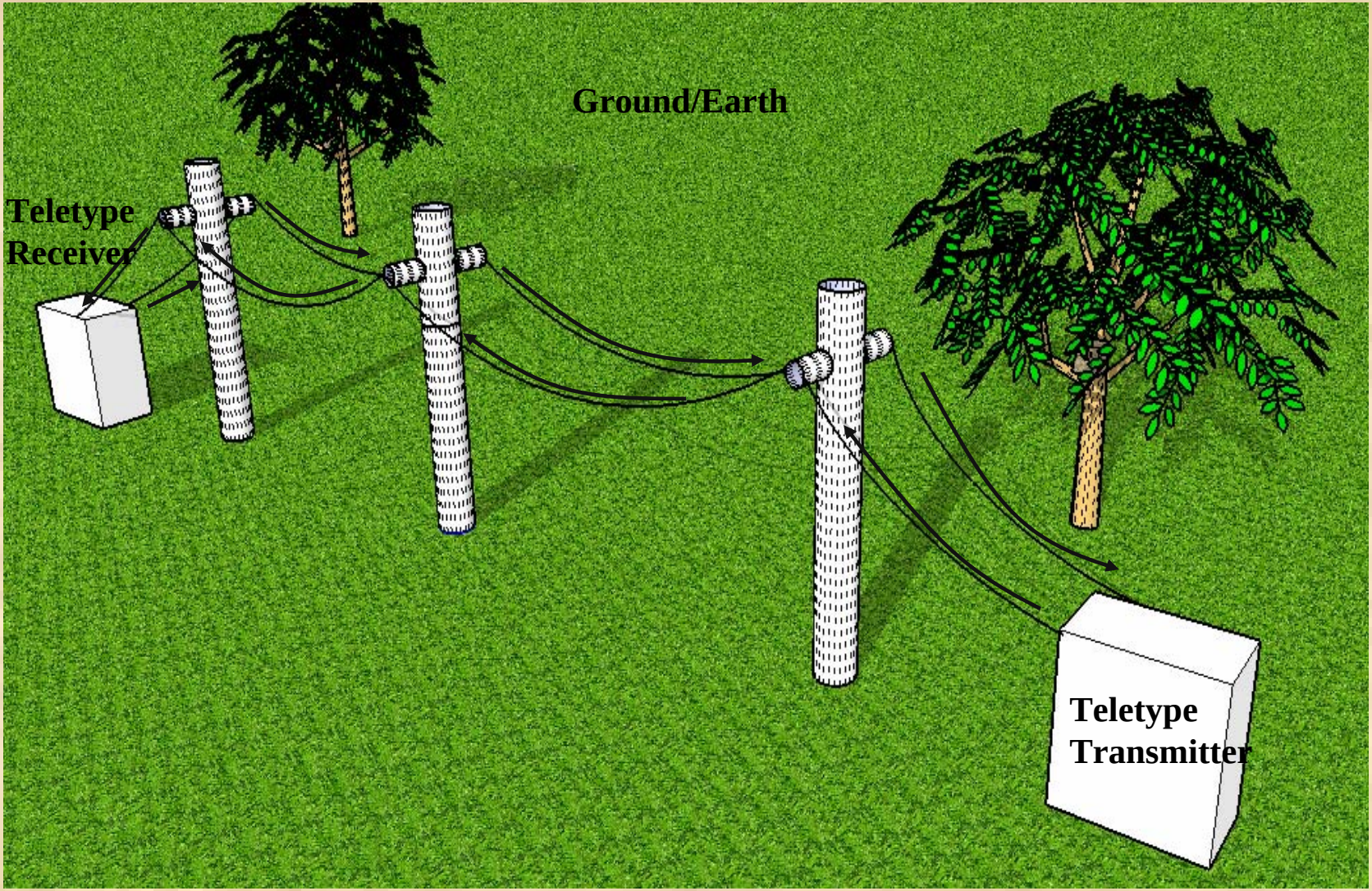


Reality Overcomes Single-Point Ground Intentions



Where did the Term "GROUND" Originate?

- Original Teletype connections
- Lightning Protection


Ground/Earth
Teletype
Receiver
Teletype
Transmitter

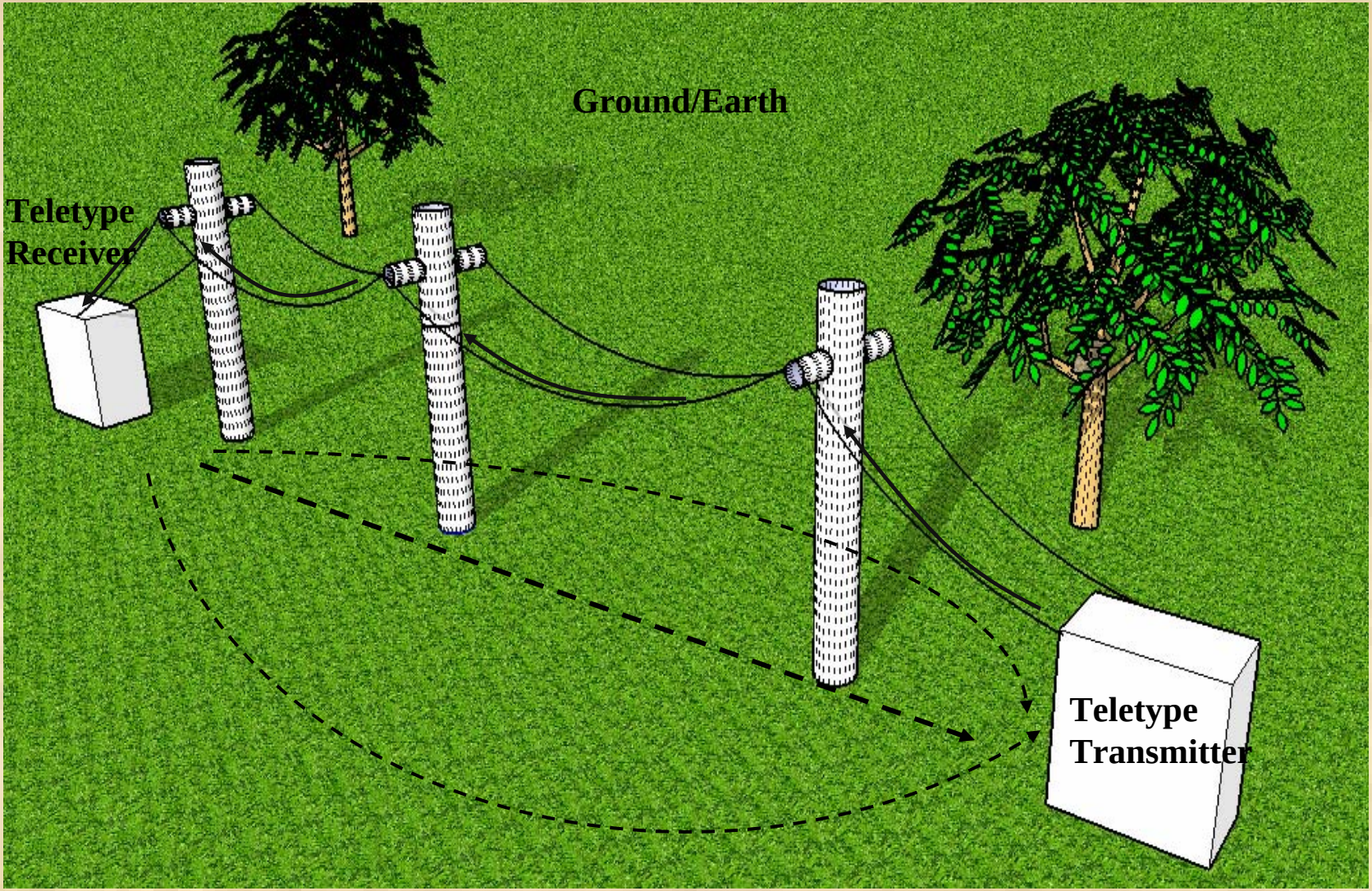
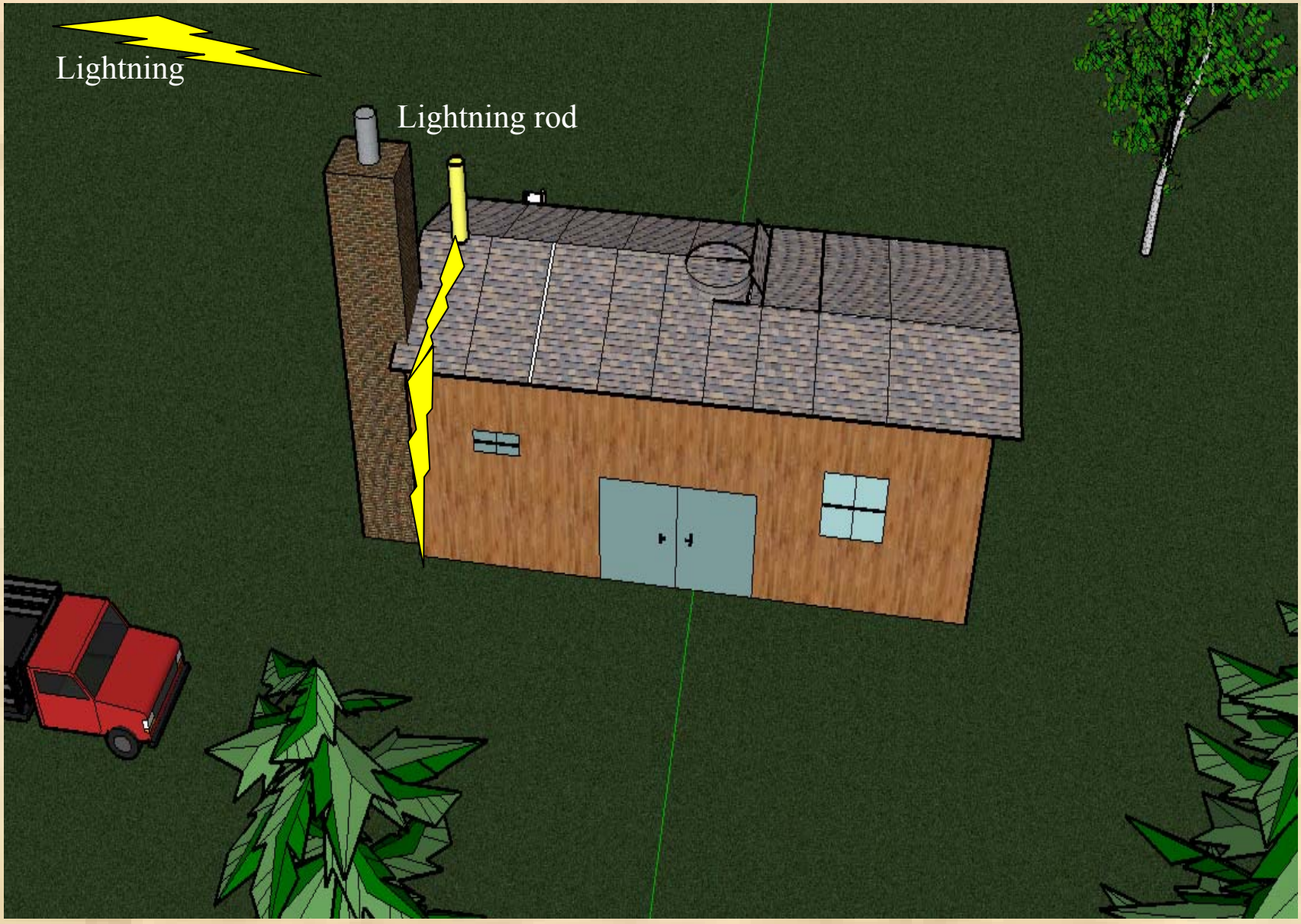

Ground/Earth
Teletype
Receiver
Teletype
Transmitter

FIG 7

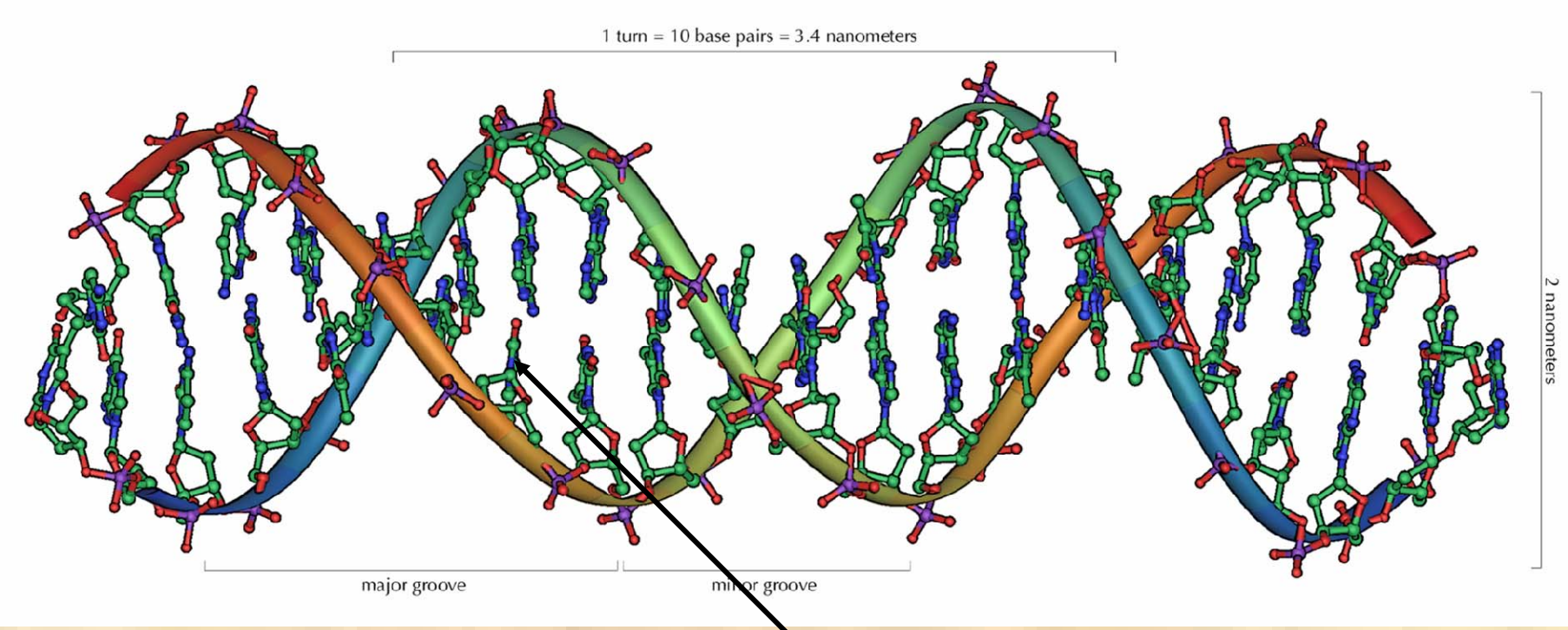
Lightning striking house

Lightning effect without rod

Lightning effect with rod



News from the Human Genome Project

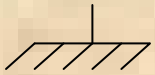


“GROUND” is good gene

What we Really Mean when we say ‘Ground’

- Signal Reference
- Power Reference
- Safety Earth
- Chassis Shield Reference

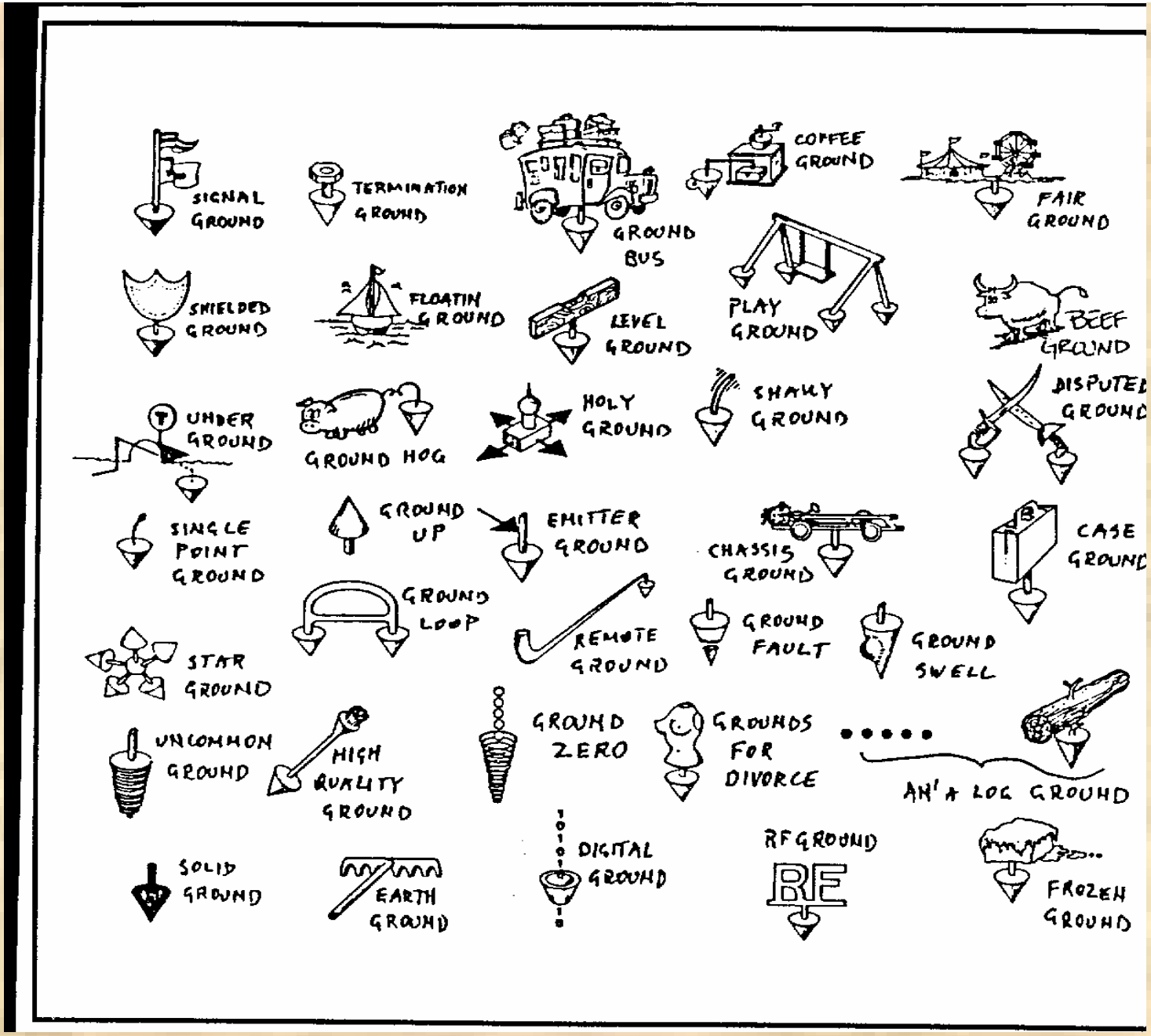
Circuit
“Ground”



Chassis
“Ground”

Digital
“Ground”

Analog
“Ground”

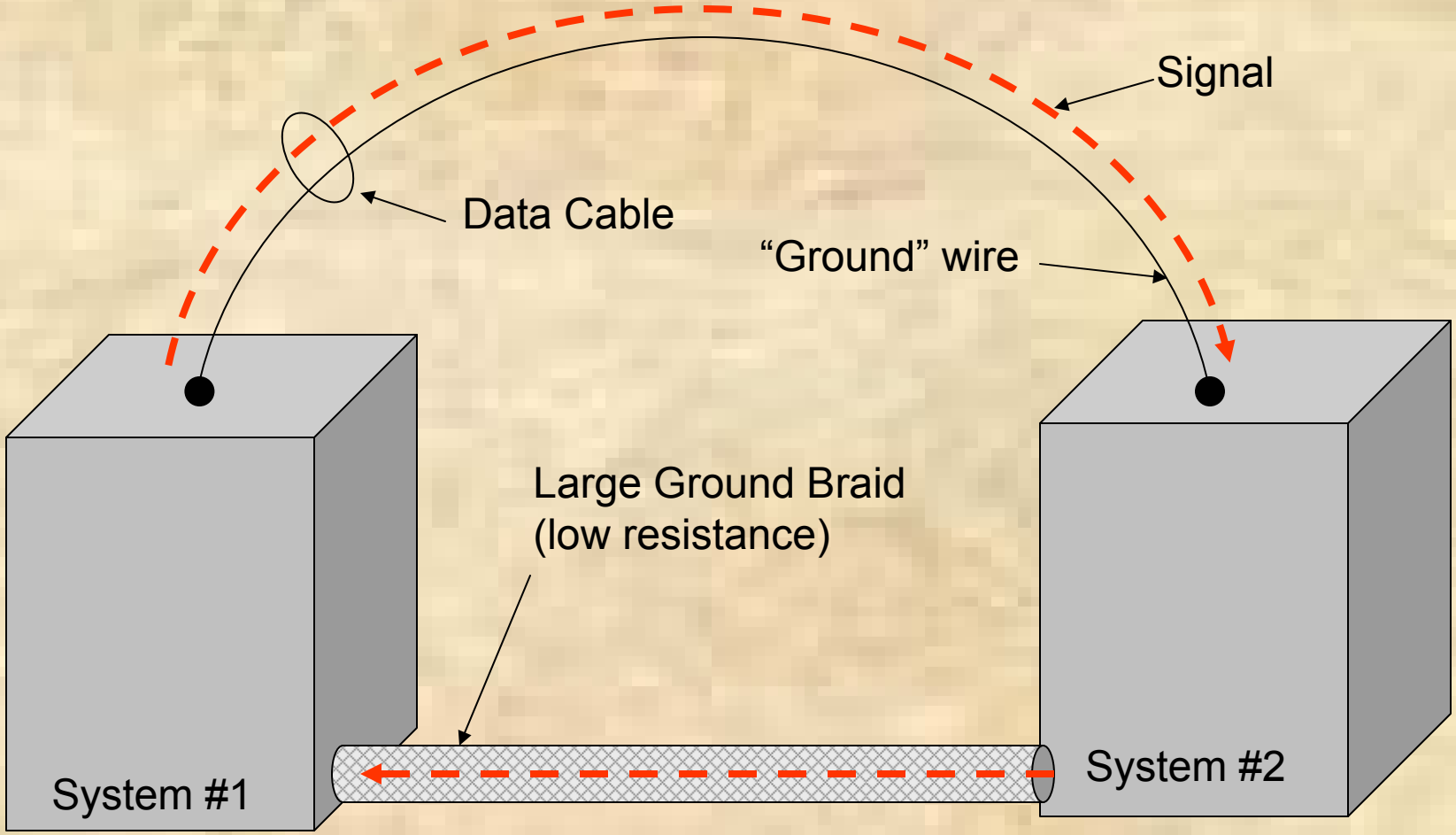

SIGNAL GROUND
TERMINATION GROUND
GROUND BUS
COFFEE GROUND
FAIR GROUND
SHIELDED GROUND
FLOATIN GROUND
LEVEL GROUND
PLAY GROUND
BEEF GROUND
UNDER GROUND
GROUND HOG
HOLY GROUND
SHAKY GROUND
DISPUTED GROUND
SINGLE POINT GROUND
GROUND UP
EMITTER GROUND
CHASSIS GROUND
CASE GROUND
GROUND LOOP
REMOTE GROUND
GROUND FAULT
GROUND SWELL
STAR GROUND
UNCOMMON GROUND
HIGH QUALITY GROUND
GROUND ZERO
GROUNDS FOR DIVORCE
AN' A LOG GROUND
SOLID GROUND
EARTH GROUND
DIGITAL GROUND
RF GROUND
RF
FROZEN GROUND

Current Path

- Current will ALWAYS follow the path of least *impedance*
  - Low frequencies → lowest *resistance*
  - High frequencies → lowest *inductance*
  - Change over ~ 100 KHz

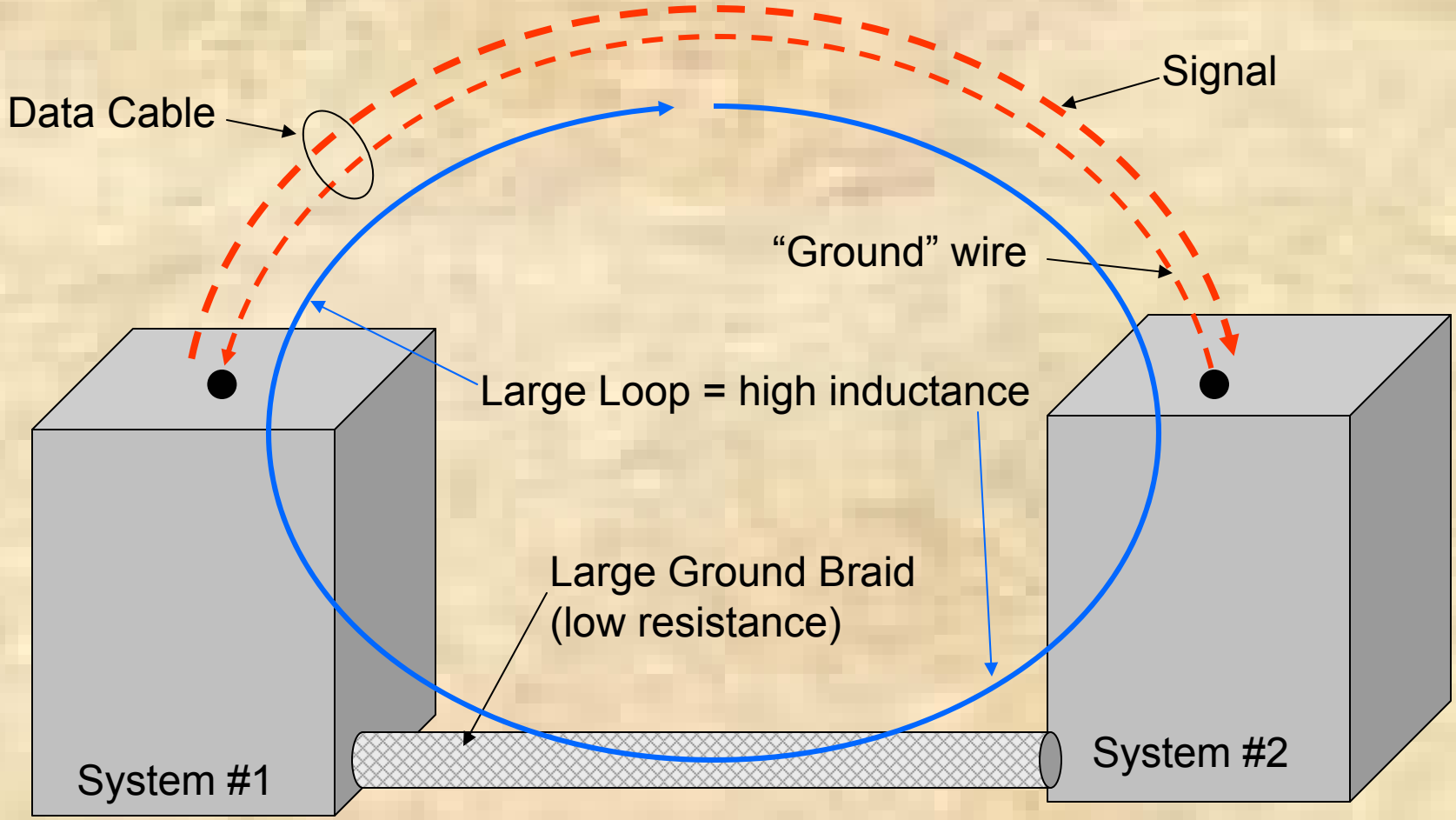
Low Frequency Return Current

Path of Least RESISTANCE

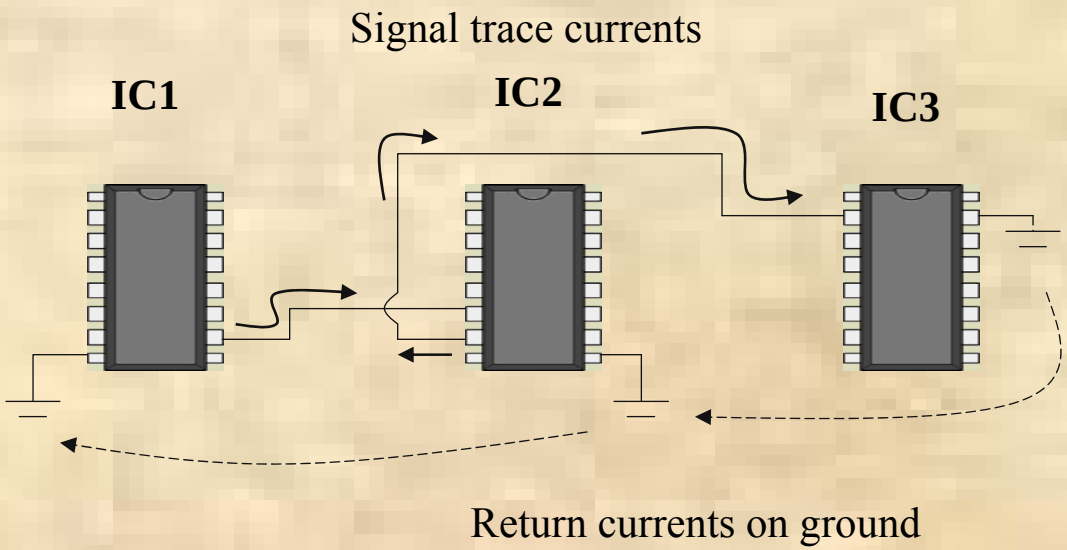


High Frequency Return Current

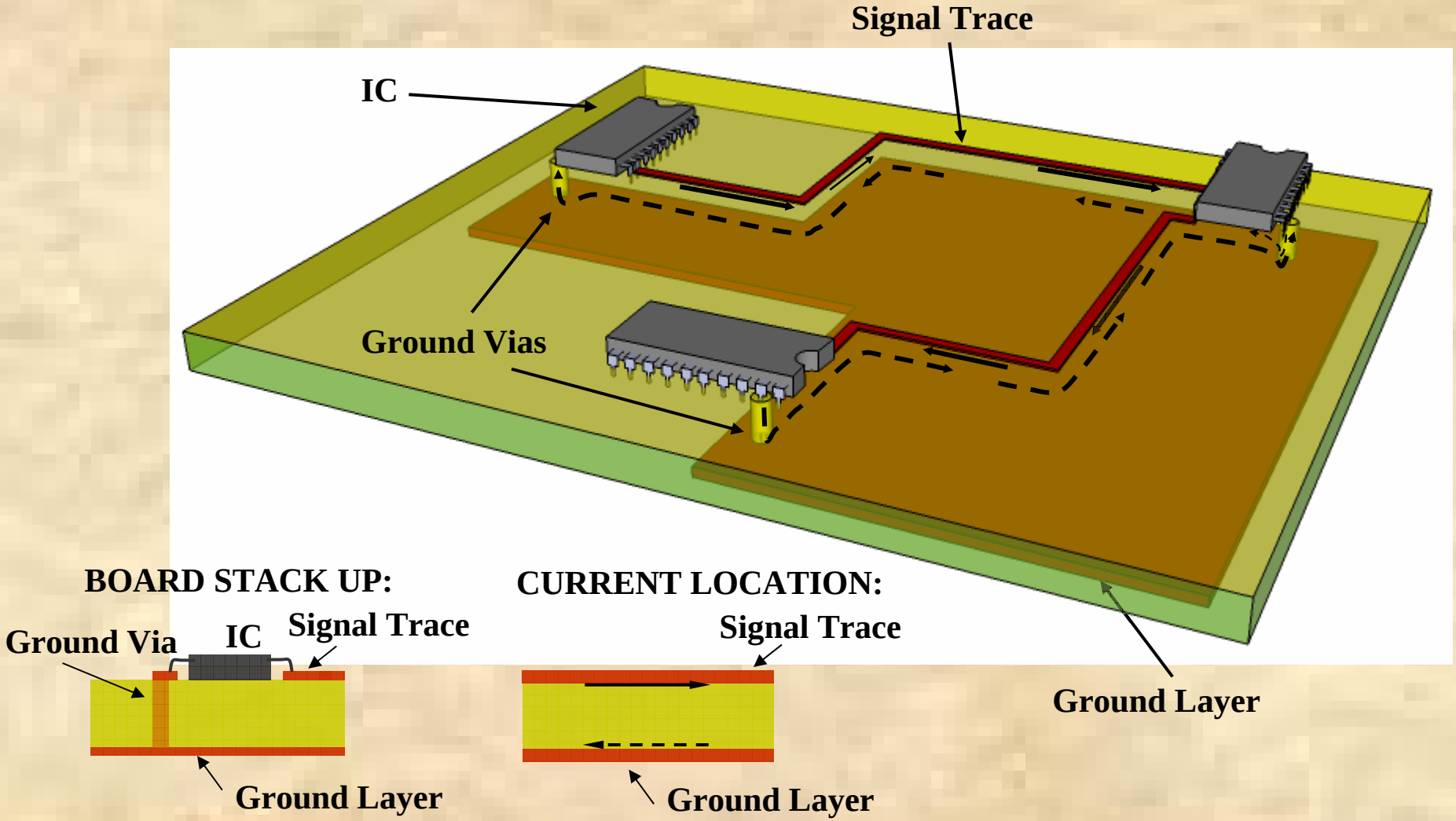
Path of Least Inductance



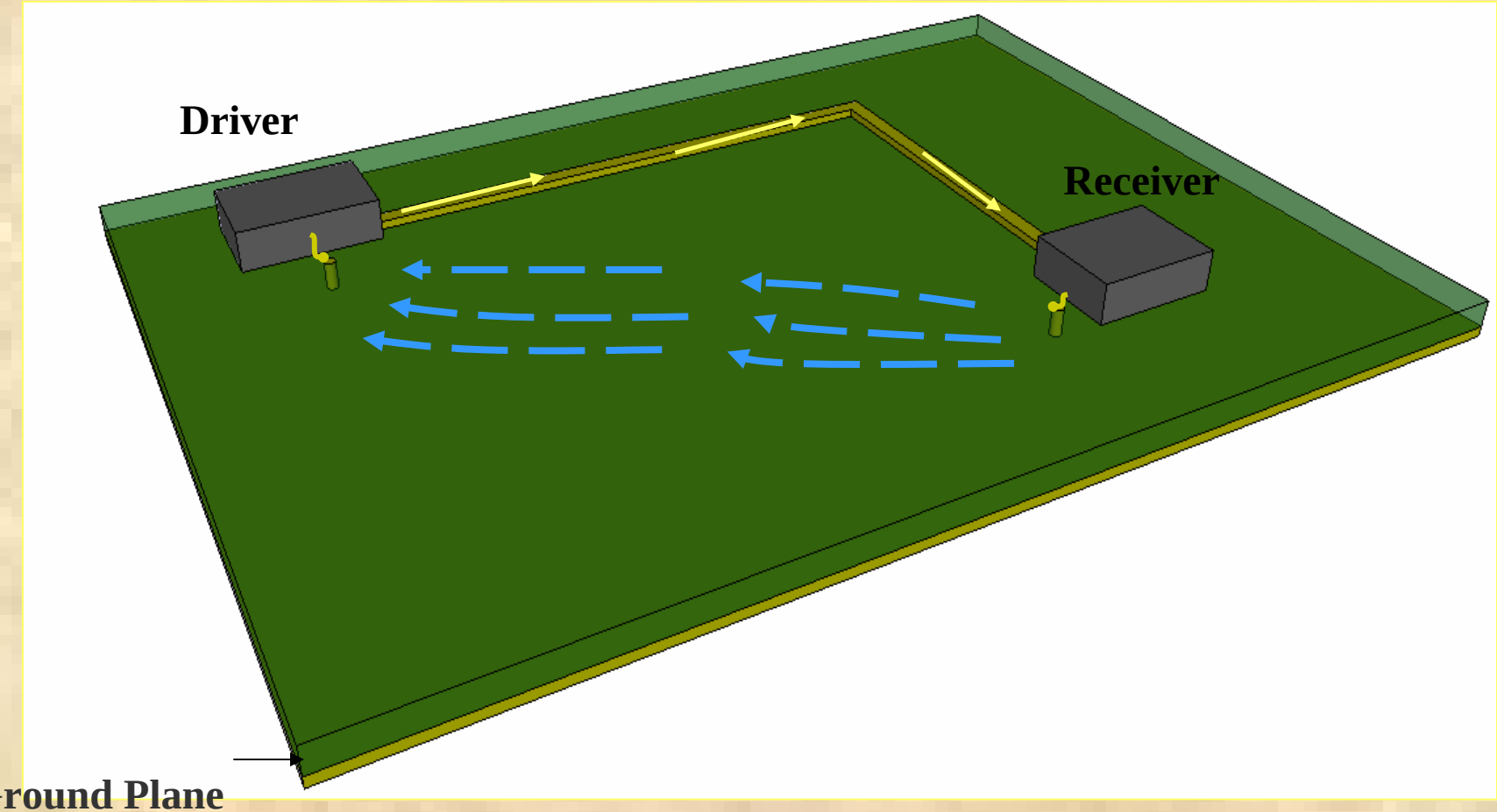
Schematic with return current shown



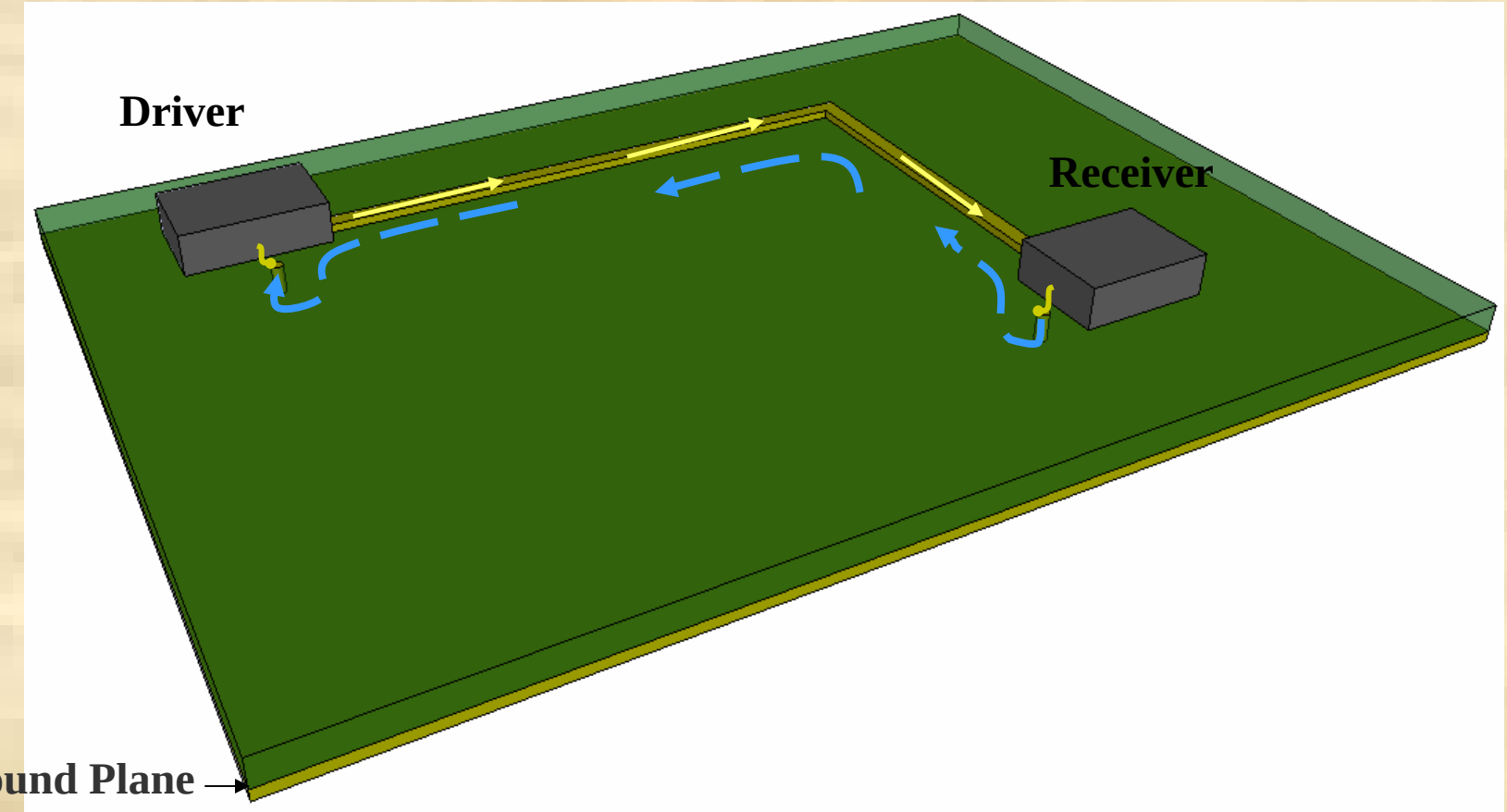
Actual Current Return is 3-Dimensional



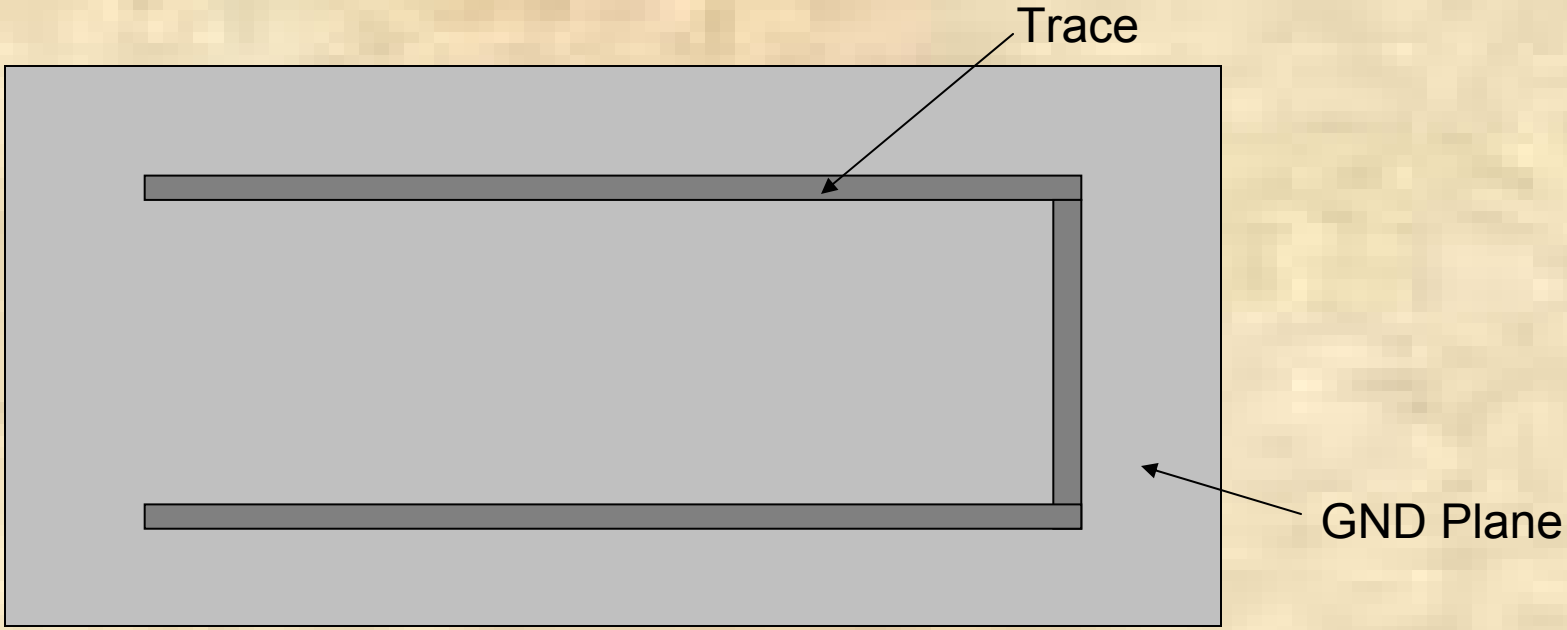
Low Frequency Return Currents Take Path of Least ***Resistance***



High Frequency Return Currents Take Path of Least ***Inductance***



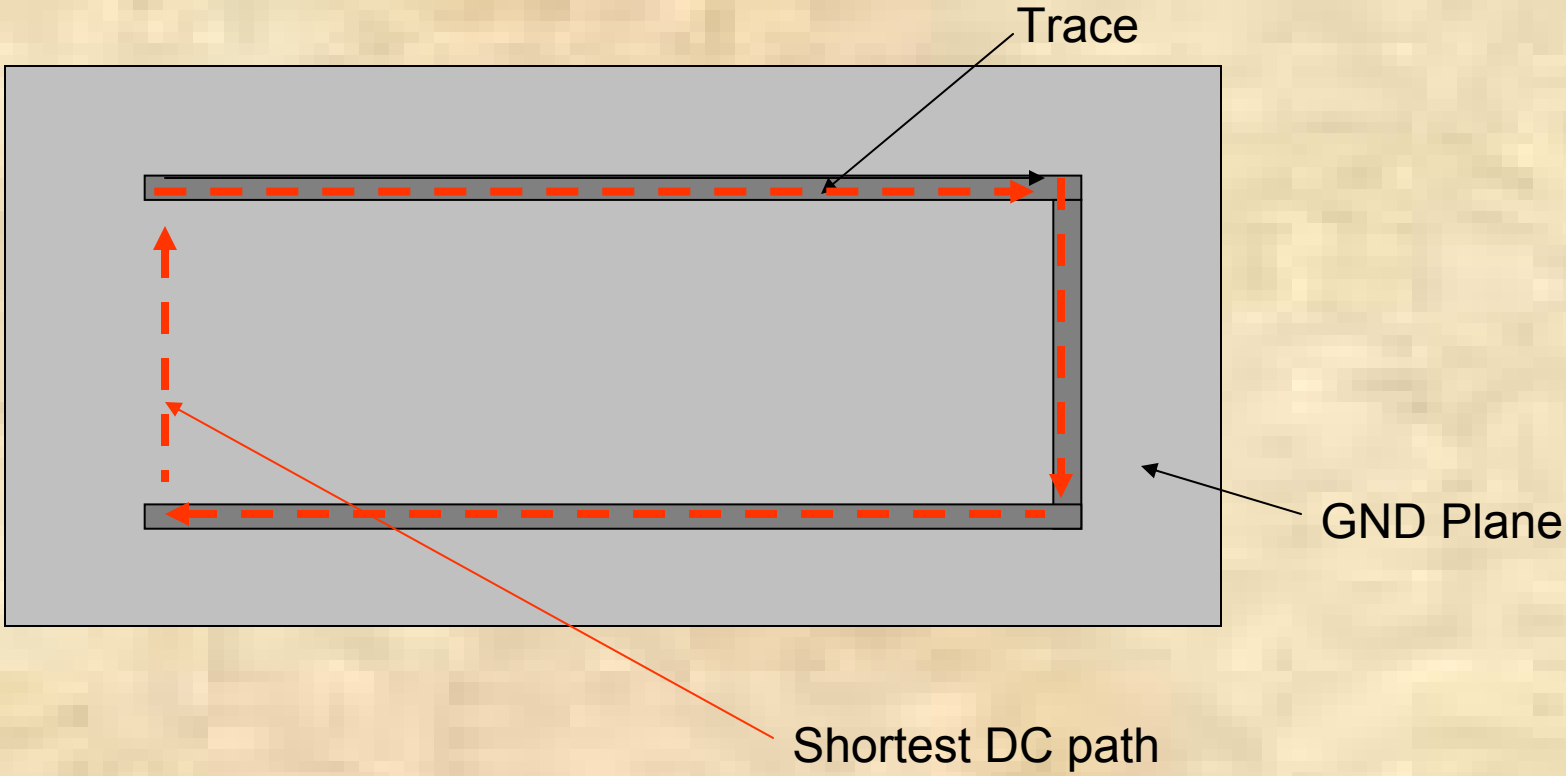
PCB Example for Return Current Impedance



22” trace

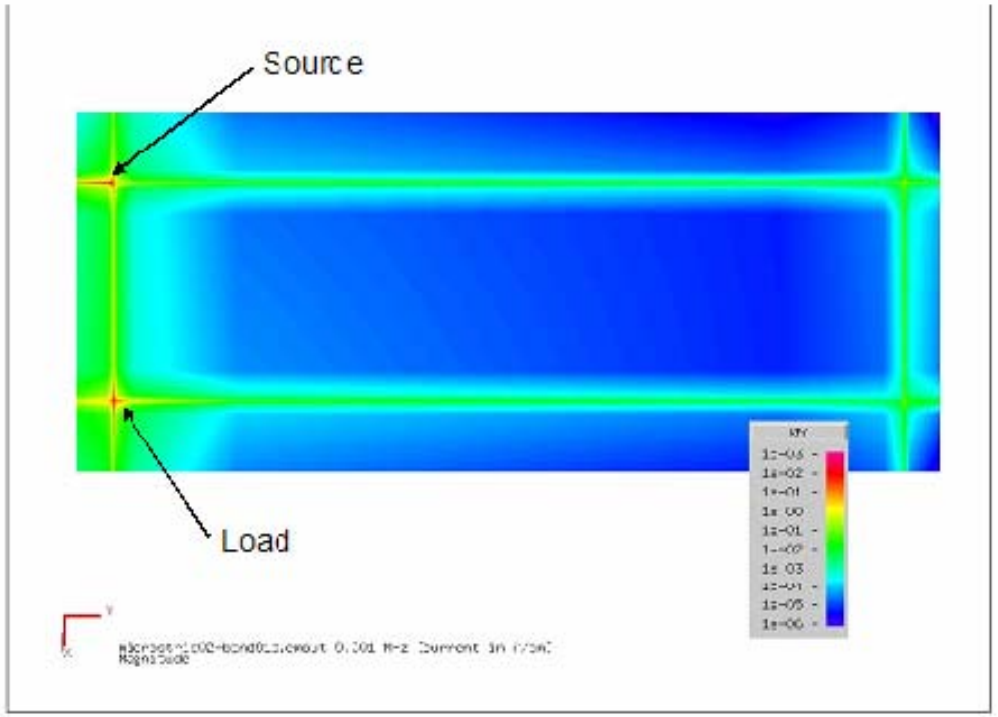
10 mils wide, 1 mil thick, 10 mils above GND plane

PCB Example for Return Current Impedance

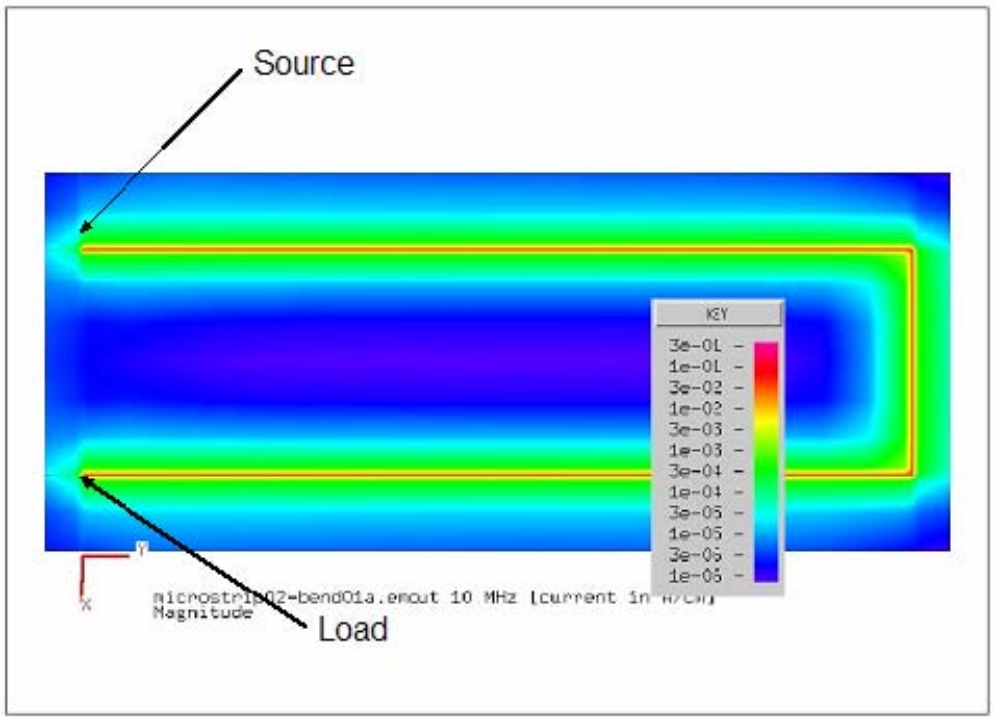


For longest DC path, current returns under trace

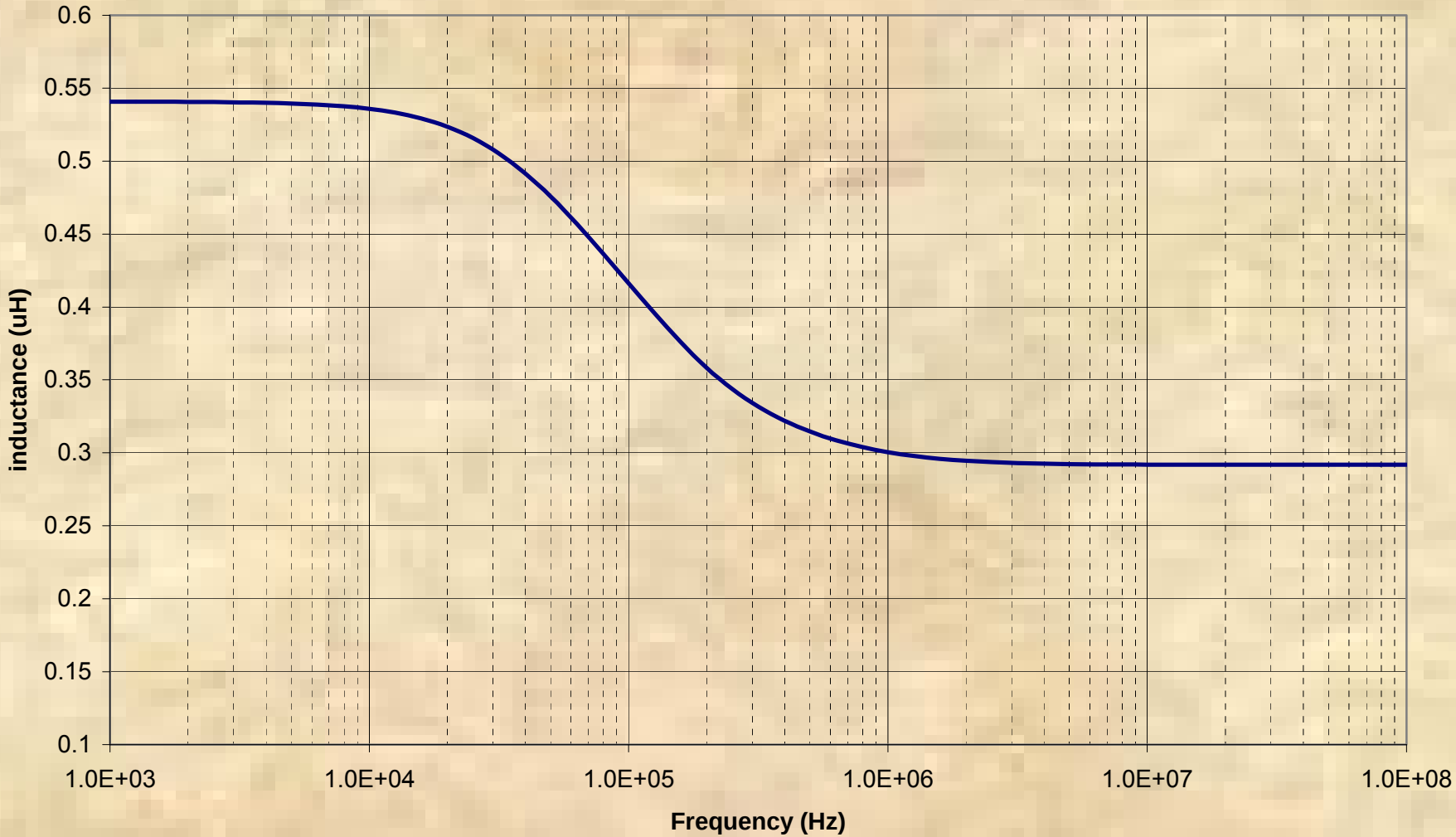
MoM Results for Current Density Frequency = 1 KHz



MoM Results for Current Density Frequency = 1 MHz

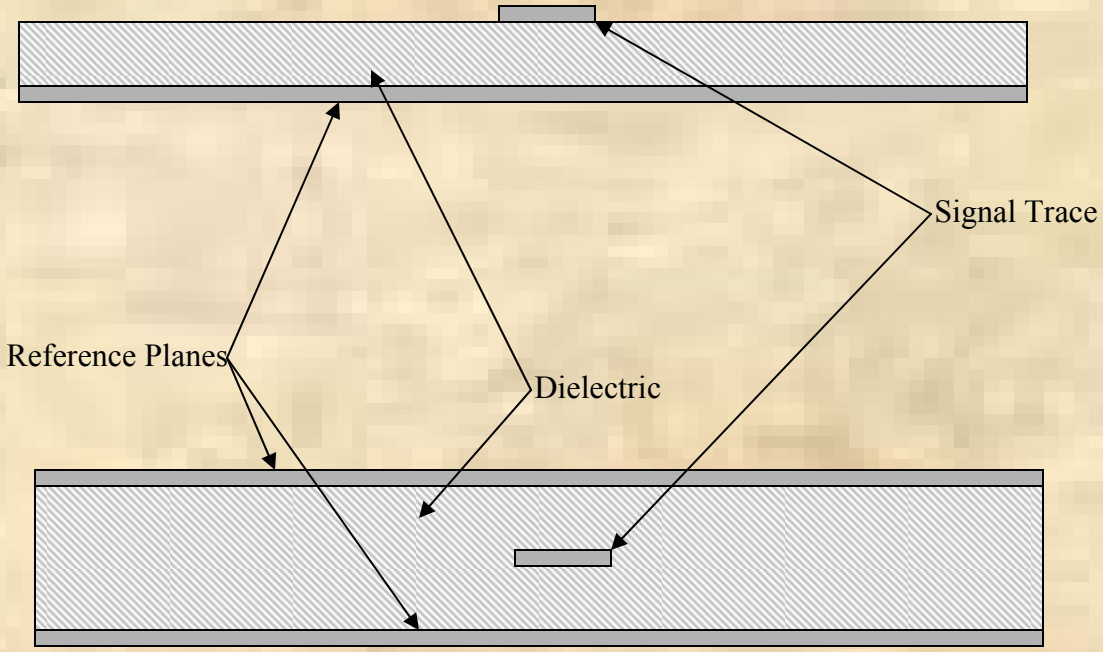


U-shaped Trace Inductance
PowerPEEC Results



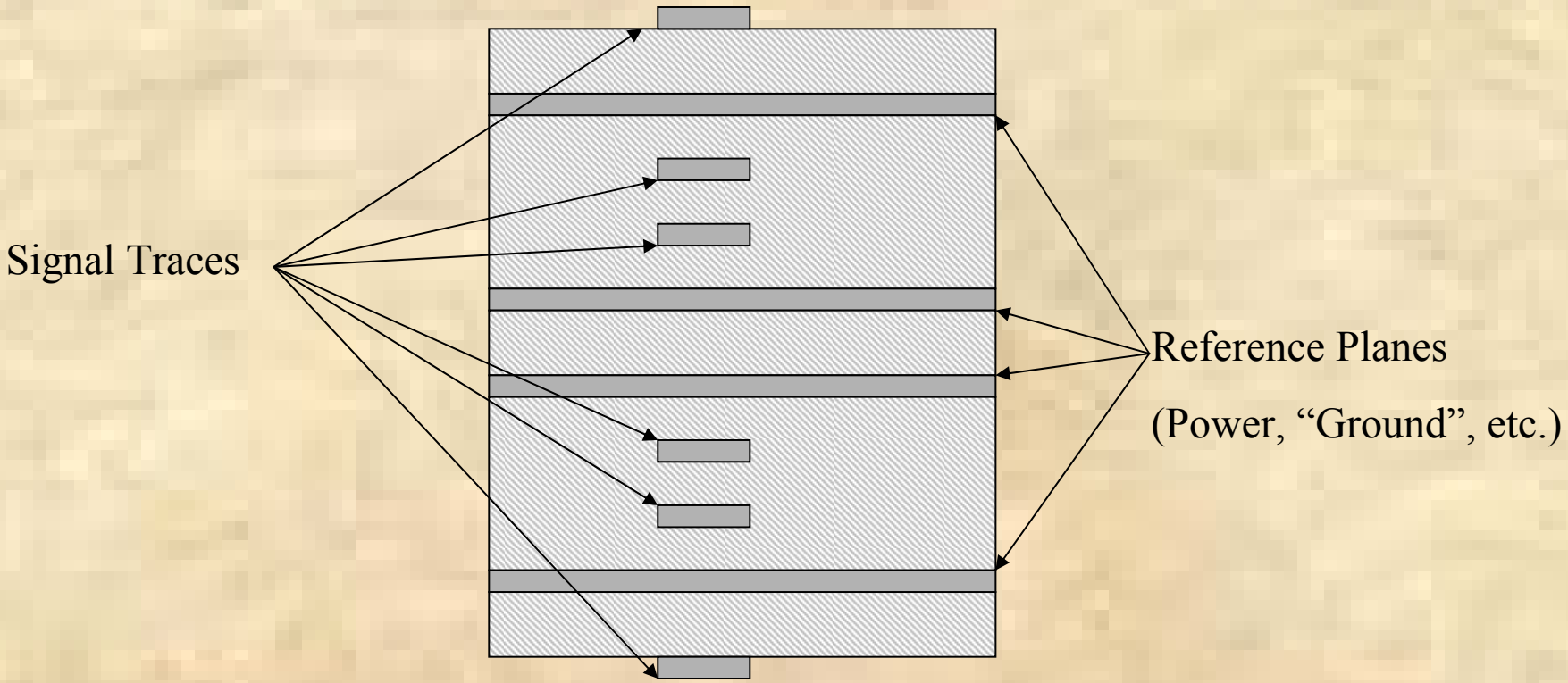
Traces/nets over a Reference Plane

Microstrip Transmission Line

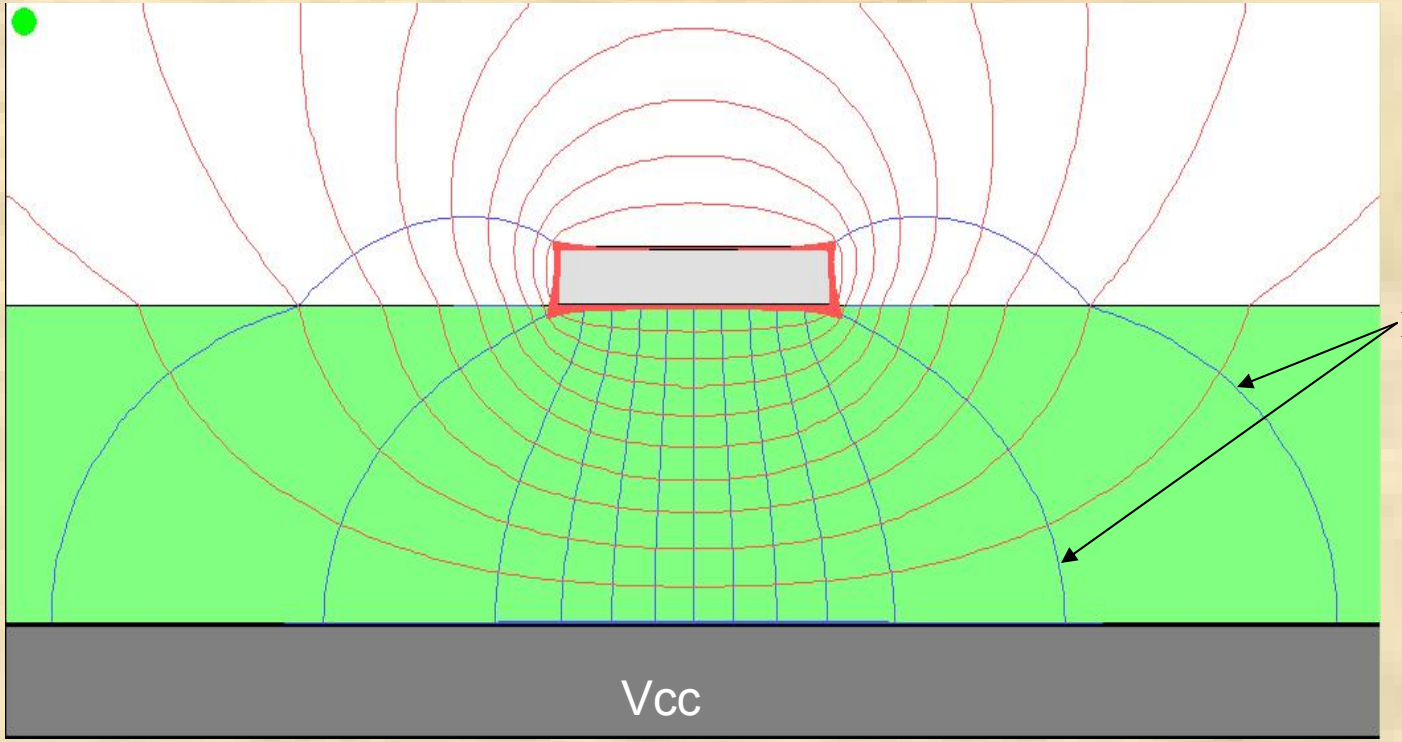


Stripline Transmission Line

Traces/nets and Reference Planes in Many Layer Board Stackup



Microstrip Electric/Magnetic Field Lines
(8mil wide trace, 8 mils above plane, 65 ohm)

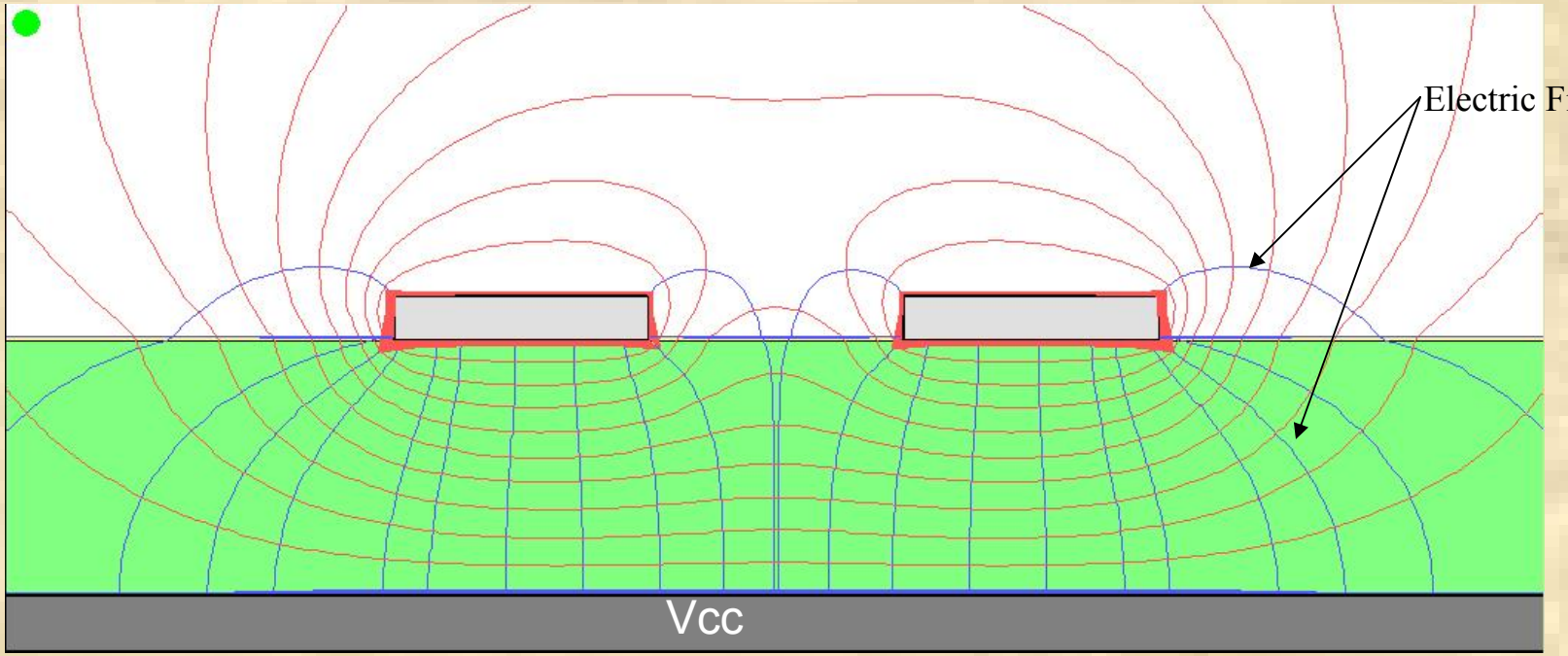


Courtesy of Hyperlynx

Microstrip Electric/Magnetic Field Lines

Common Mode

8 mil wide trace, 8 mils above plane, 65/115 ohm)

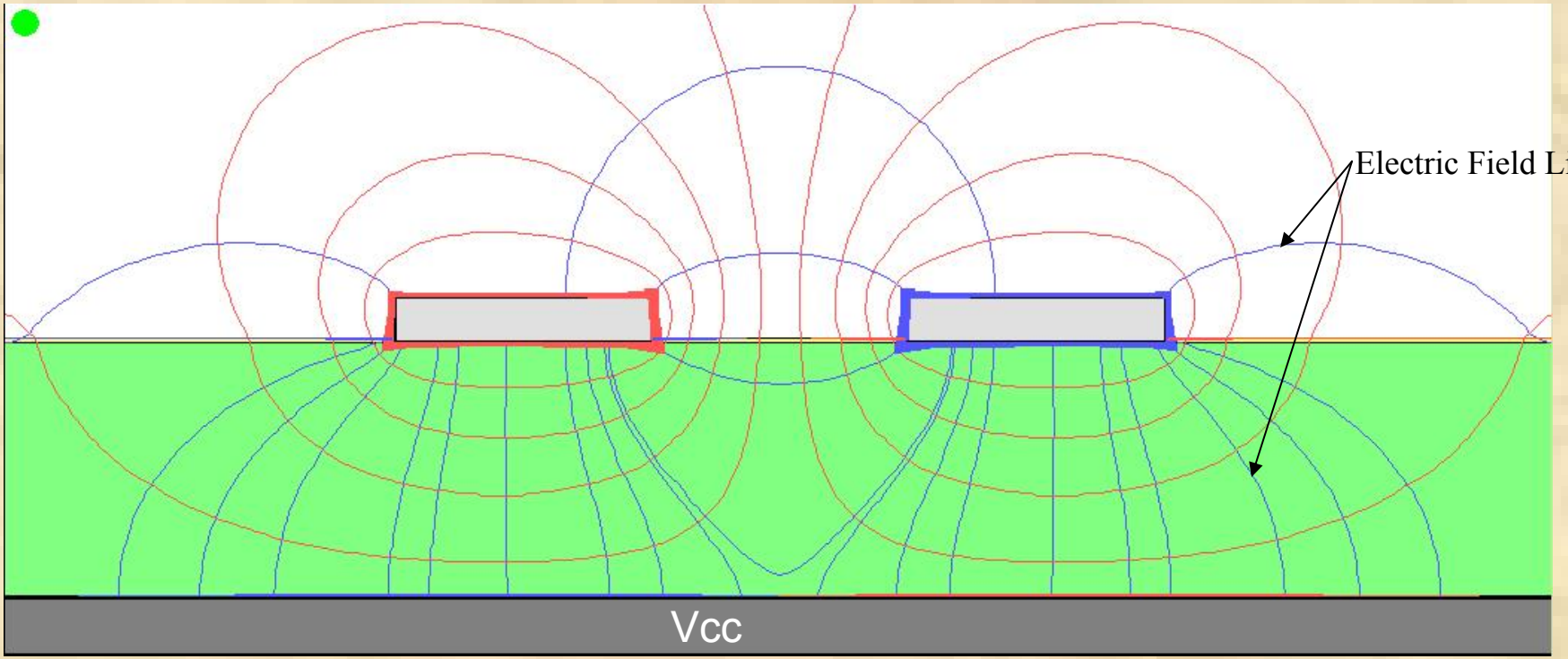


Courtesy of Hyperlynx

Microstrip Electric/Magnetic Field Lines

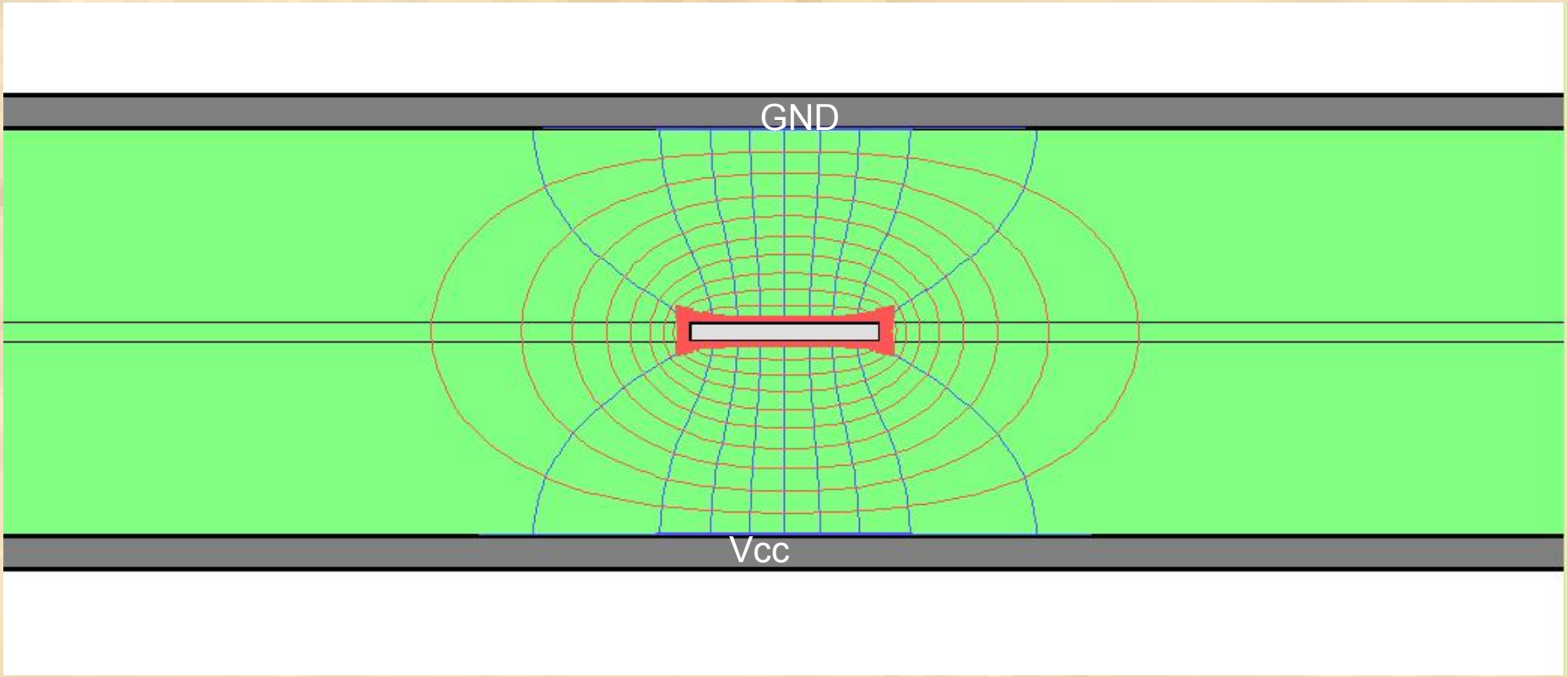
Differential Mode

8 mil wide trace, 8 mils above plane, 65/115 ohm)



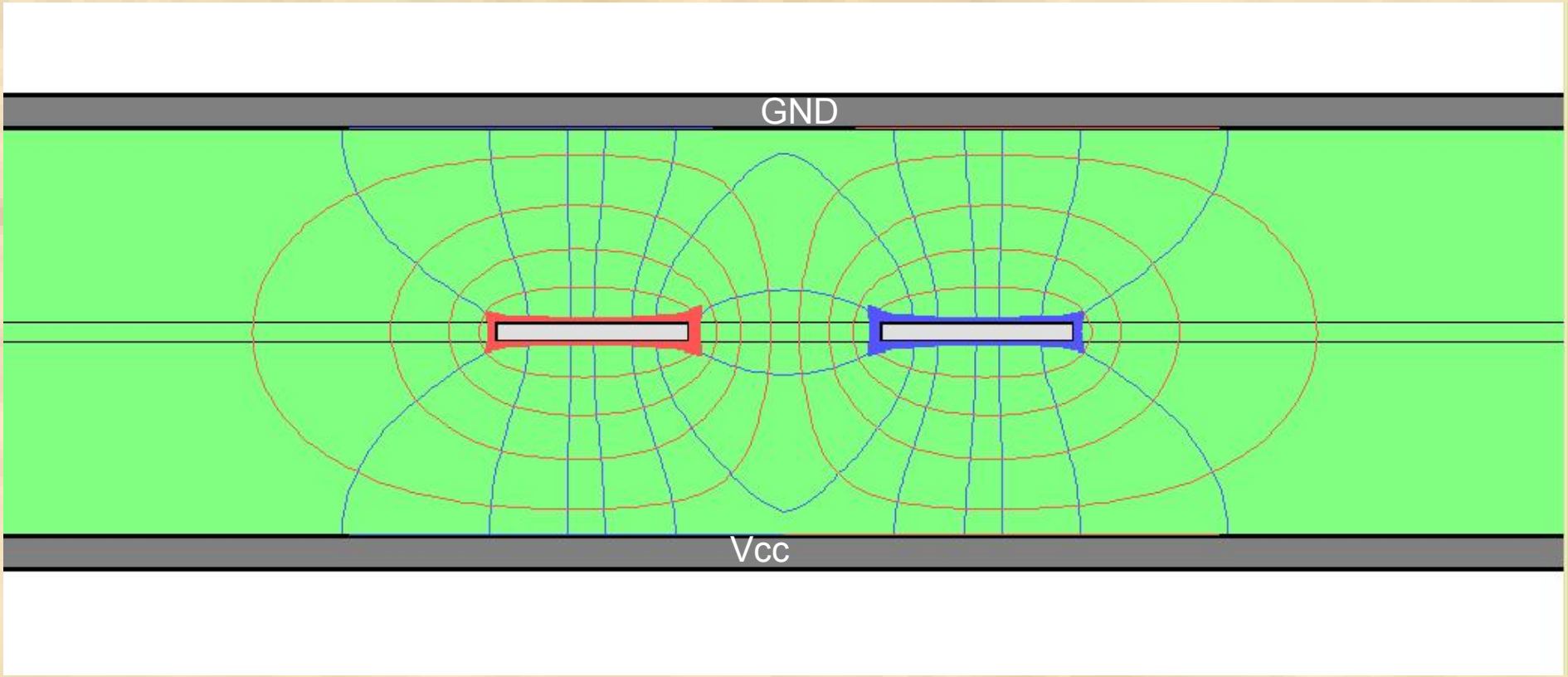
Courtesy of Hyperlynx

Electric/Magnetic Field Lines
Symmetrical Stripline



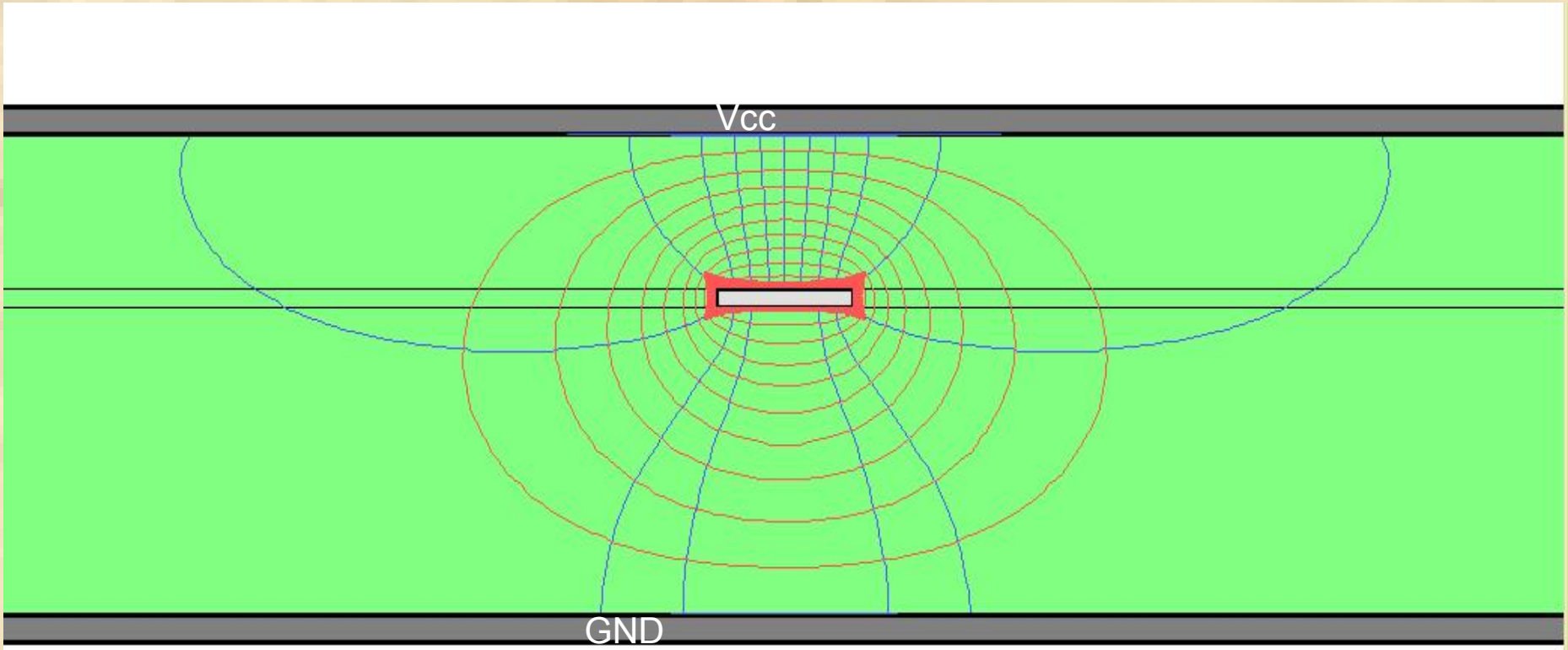
Courtesy of Hyperlynx

Electric/Magnetic Field Lines
Symmetrical Stripline (Differential)



Courtesy of Hyperlynx

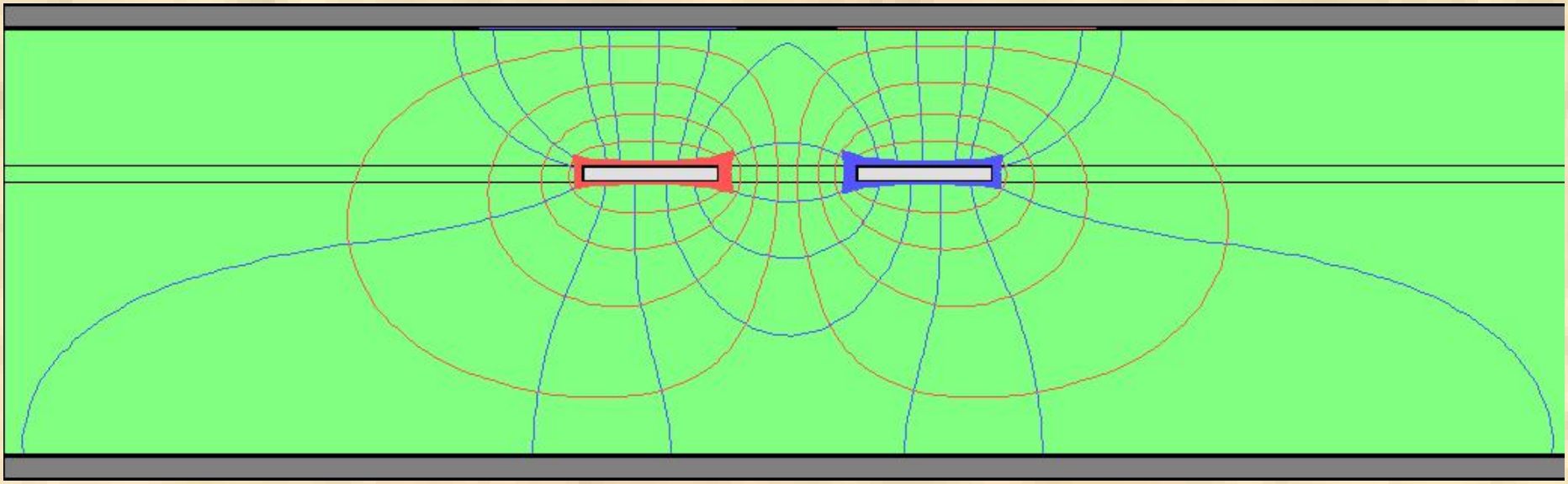
Electric/Magnetic Field Lines
Asymmetrical Stripline



Courtesy of Hyperlynx

Electric/Magnetic Field Lines

Asymmetrical Stripline (Differential)



Courtesy of Hyperlynx

Pseudo-Differential Nets

- Are the drivers really differential? Or complementary single ended nets?
- True differential requires no nearby reference plane
- Currents *will* exist on reference plane

Pseudo-Differential Nets
Reference Plane Currents

- Signal integrity is greatly helped by 'differential' nets
- Currents in reference plane
  - Balanced only if:
    - Traces are equal length (within 10-20 mils)
    - Drivers are EXACTLY balanced
  - Not likely!

What About Pseudo-Differential Nets?

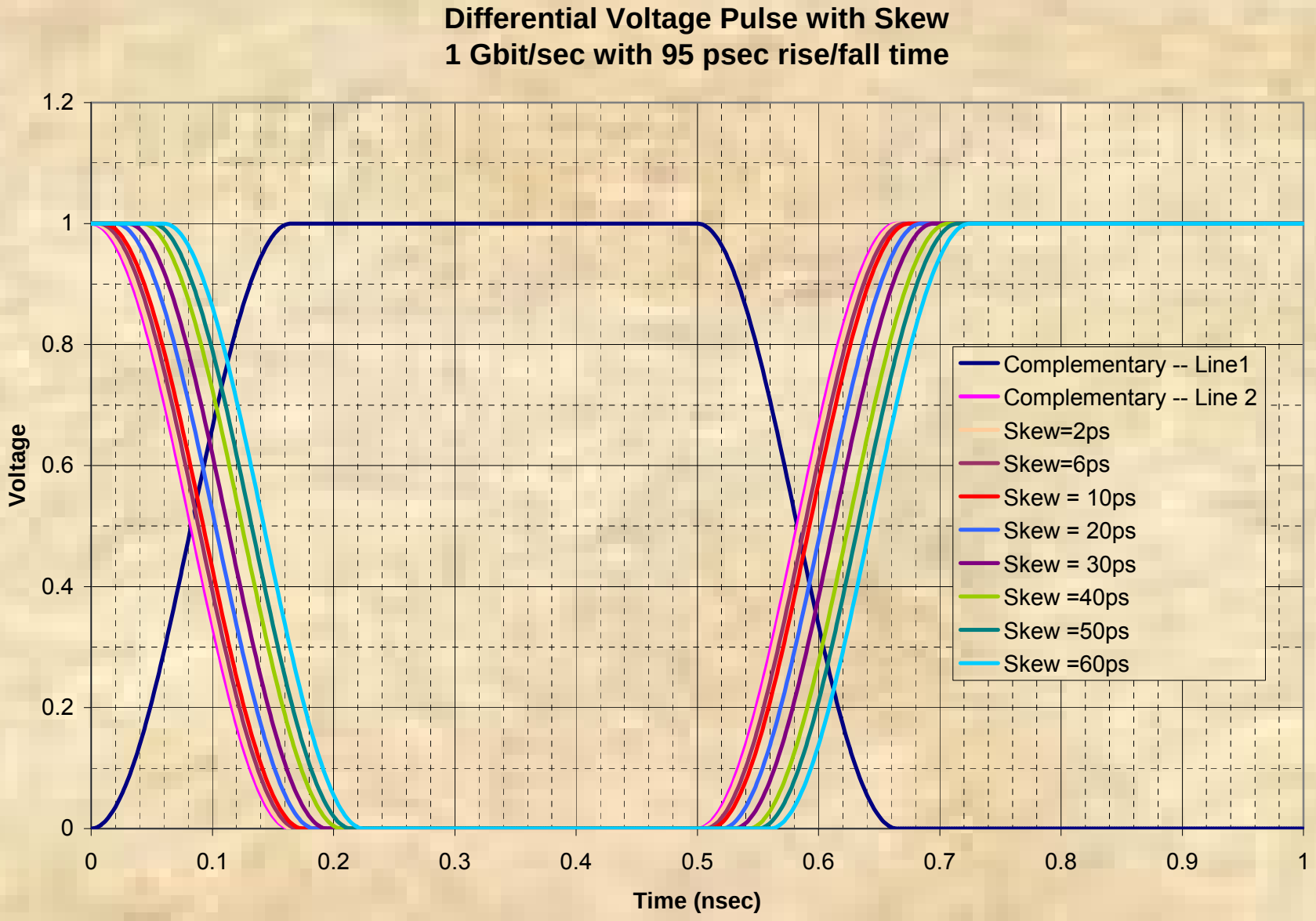
- So-called differential traces are NOT truly differential
  - Two complementary single-ended drivers
    - Relative to ‘ground’
  - Receiver is differential
    - Senses difference between two nets (independent of ‘ground’)
    - Provides good immunity to common mode noise
    - Good for signal quality/integrity

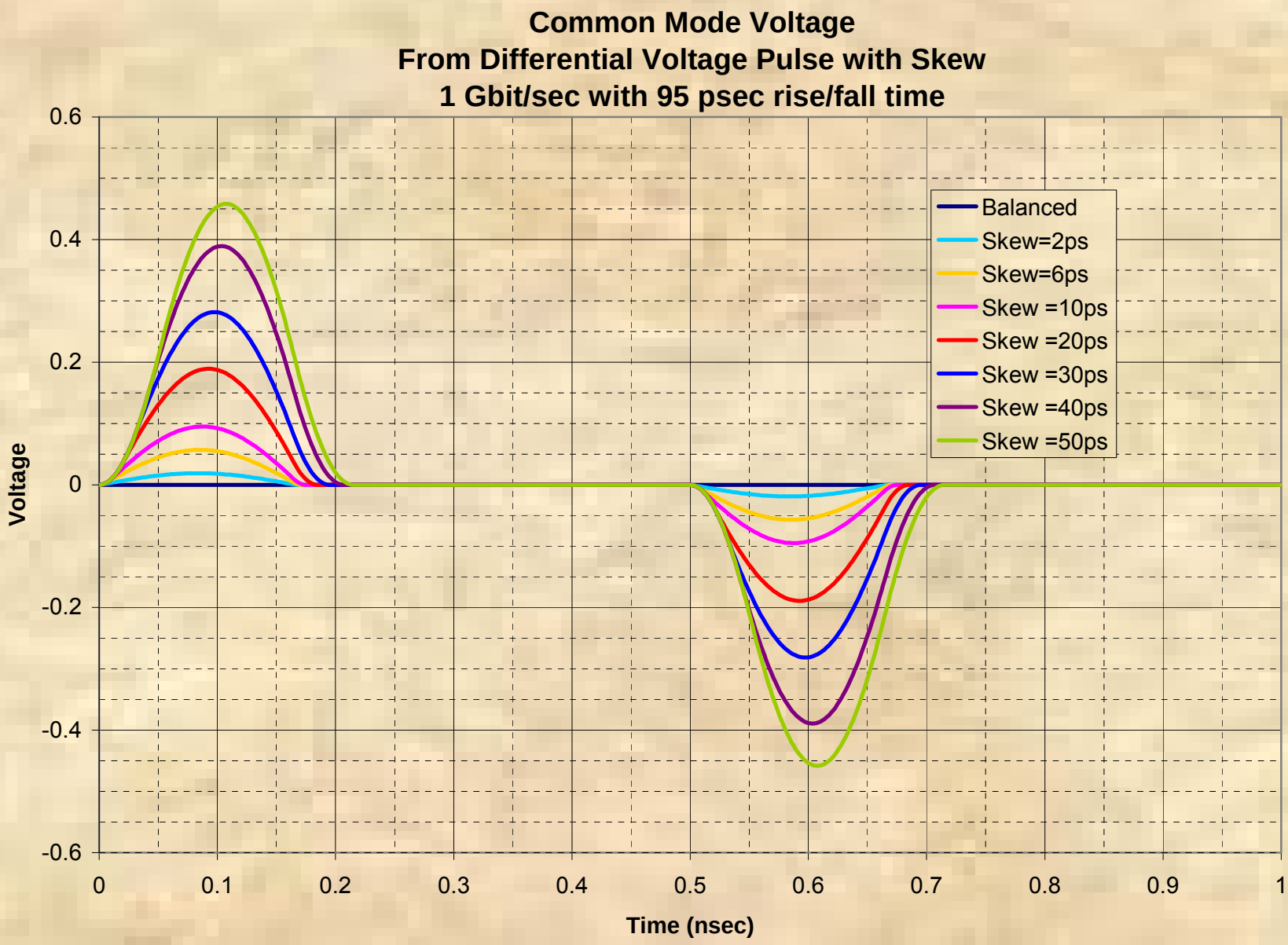
Pseudo-Differential Nets Current in Nearby Plane

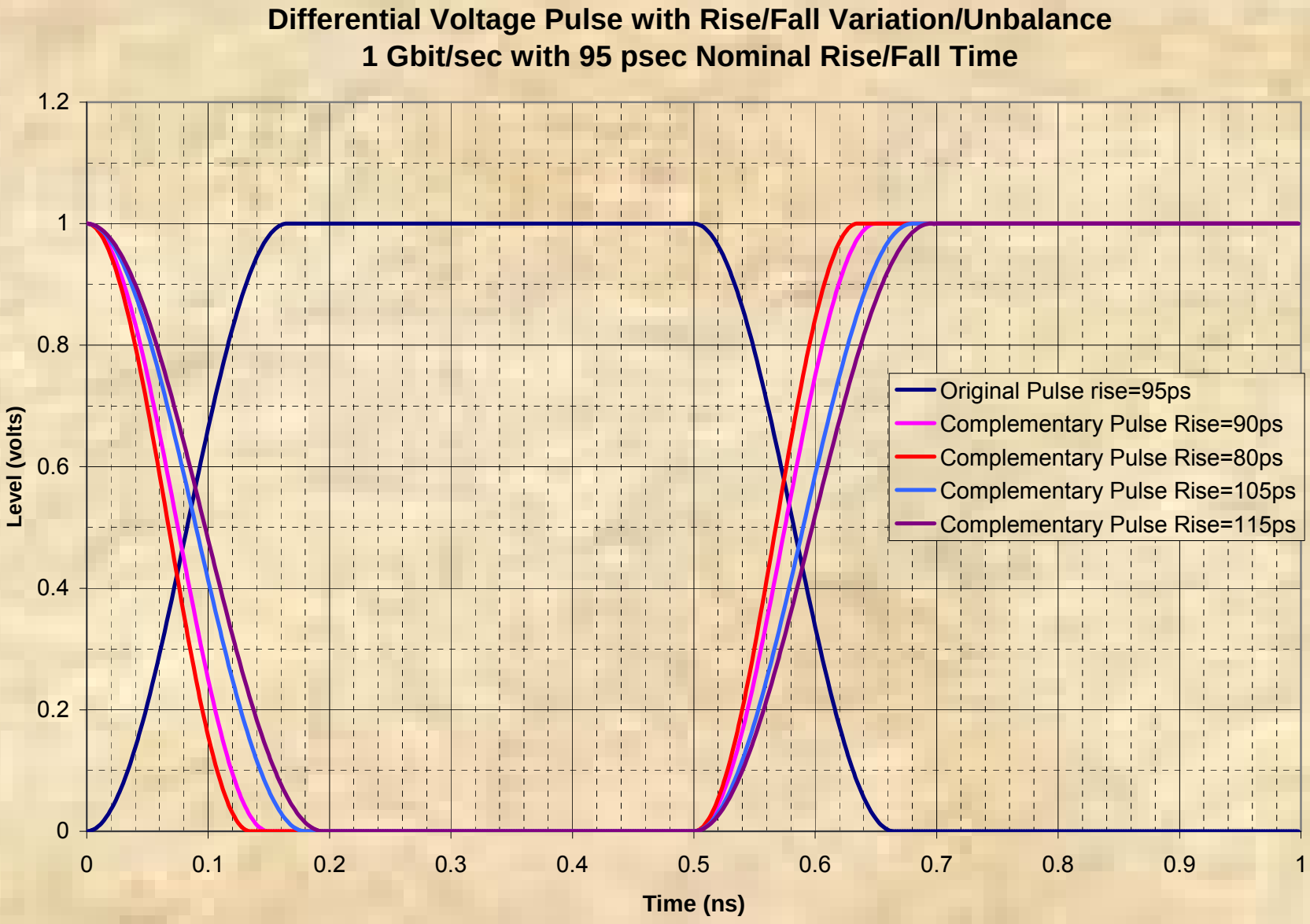
- Balanced/Differential currents have matching current in nearby plane
  - No issue for discontinuities
- Any unbalanced (common mode) currents have return currents in nearby plane that must return to source!
  - All normal concerns for single-ended nets apply!

Pseudo-Differential Nets

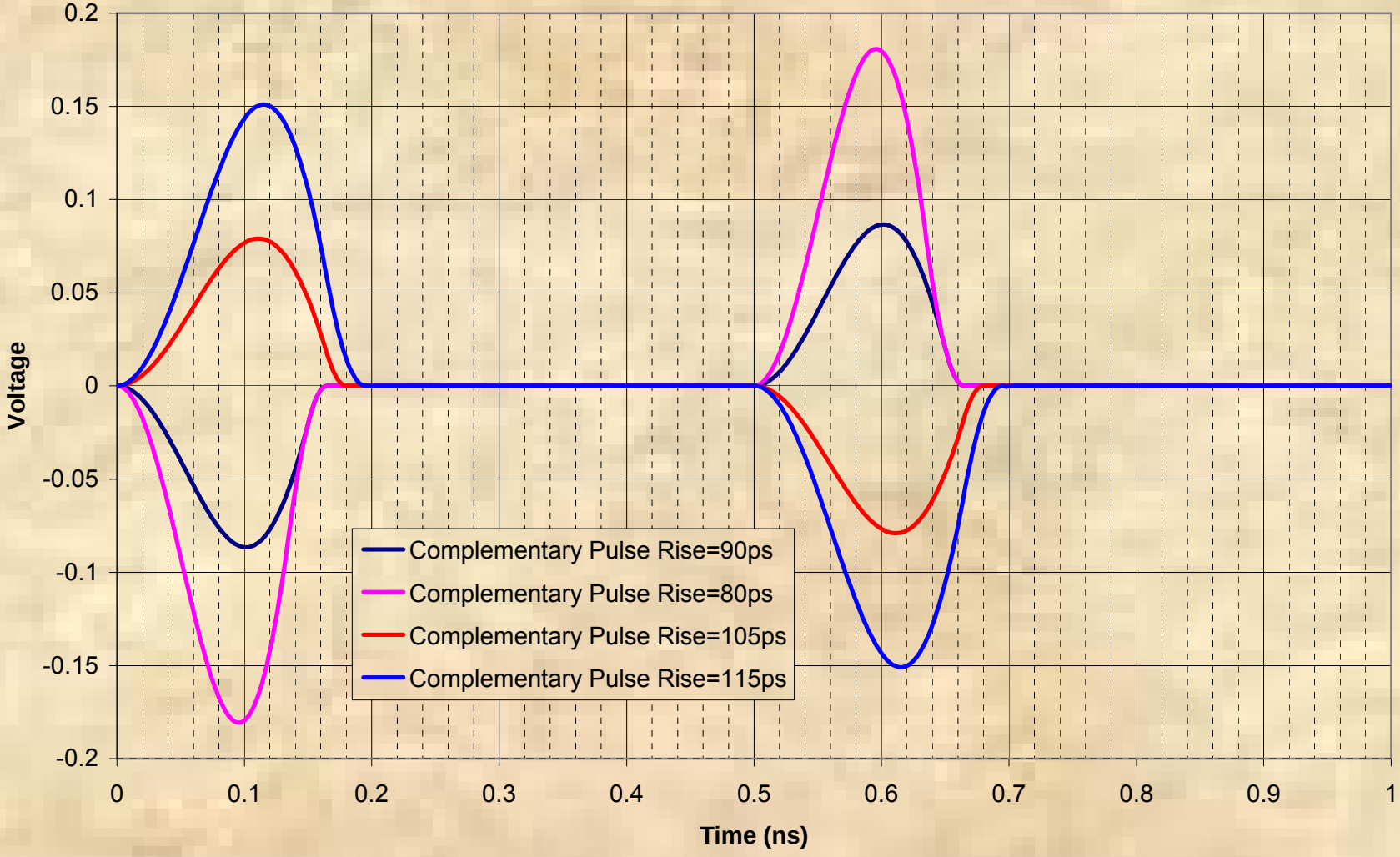
- Not really ‘differential’, since more closely coupled to nearby plane than each other
- Skew and rise/fall variation cause common mode currents!


Differential Voltage Pulse with Skew
1 Gbit/sec with 95 psec rise/fall time
Voltage
Time (nsec)
1.2
1
0.8
0.6
0.4
0.2
0
0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1
Complementary -- Line1
Complementary -- Line 2
Skew=2ps
Skew=6ps
Skew = 10ps
Skew = 20ps
Skew = 30ps
Skew =40ps
Skew =50ps
Skew =60ps

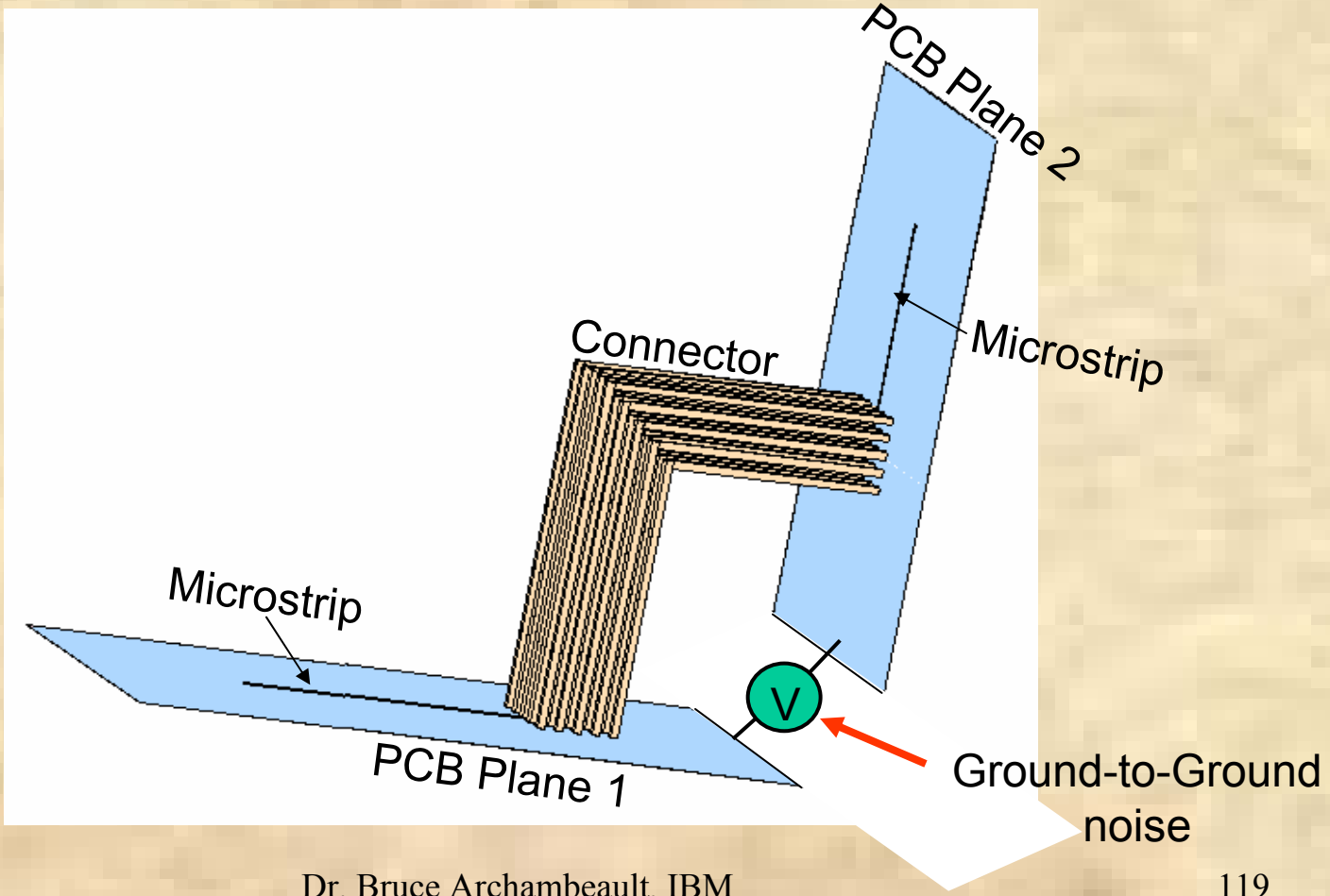

Common Mode Voltage
From Differential Voltage Pulse with Skew
1 Gbit/sec with 95 psec rise/fall time
Voltage
Time (nsec)
0.6
0.4
0.2
0
-0.2
-0.4
-0.6
0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1
Balanced
Skew=2ps
Skew=6ps
Skew =10ps
Skew =20ps
Skew =30ps
Skew =40ps
Skew =50ps


Differential Voltage Pulse with Rise/Fall Variation/Unbalance
1 Gbit/sec with 95 psec Nominal Rise/Fall Time
Level (volts)
Time (ns)
1.2
1
0.8
0.6
0.4
0.2
0
0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1
Original Pulse rise=95ps
Complementary Pulse Rise=90ps
Complementary Pulse Rise=80ps
Complementary Pulse Rise=105ps
Complementary Pulse Rise=115ps

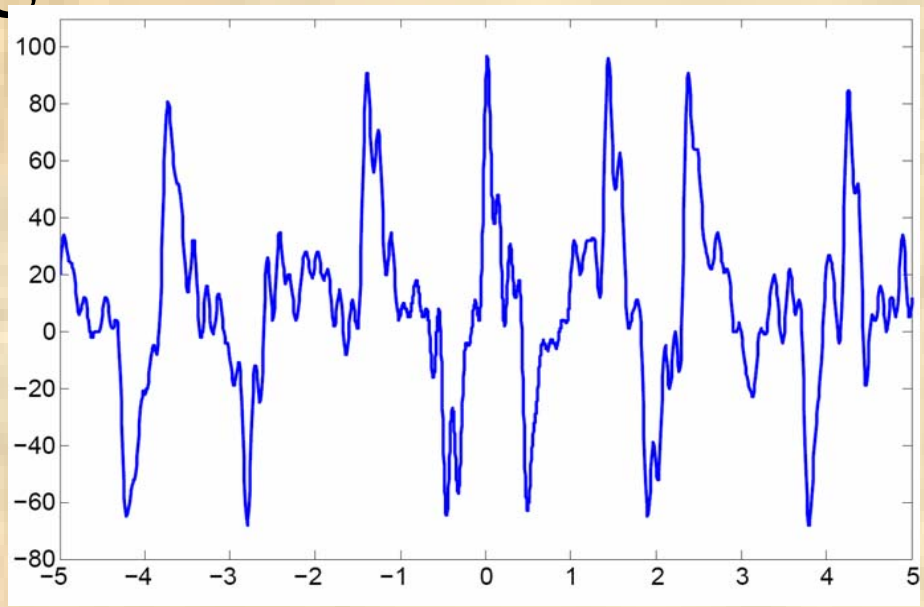
Common Mode Voltage
From Differential Voltage Pulse with Various Rise/Fall Unbalance
1 Gbit/sec with 95 psec Nominal Rise/Fall Time



Board-to-Board Differential Pair Issues



Example Measured Differential Individual Signal-to-GND

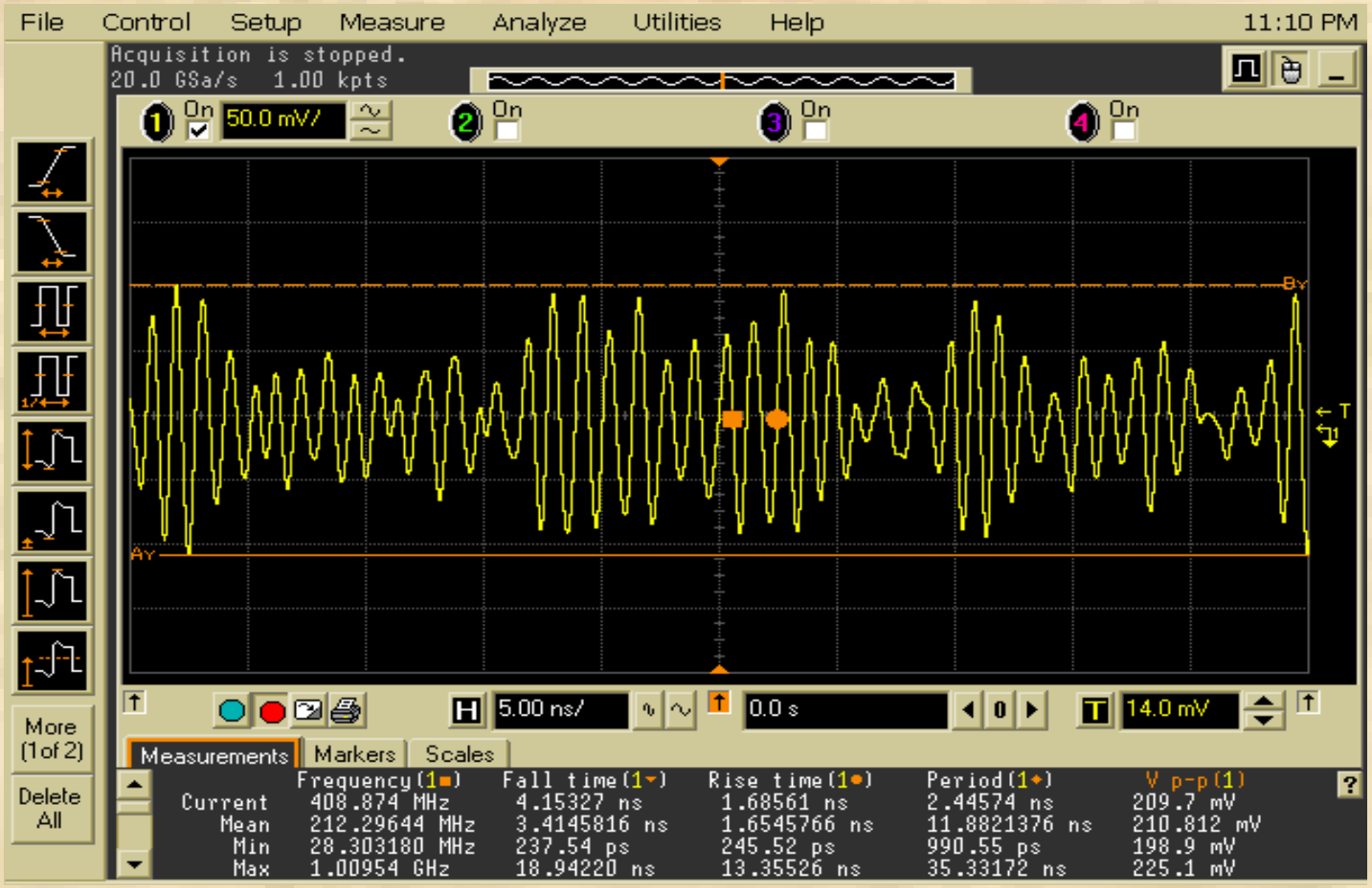


500 mV P-P (each)

Individual Differential Signals ADDED

Common Mode Noise
170 mV P-P

Measured GND-to-GND Voltage

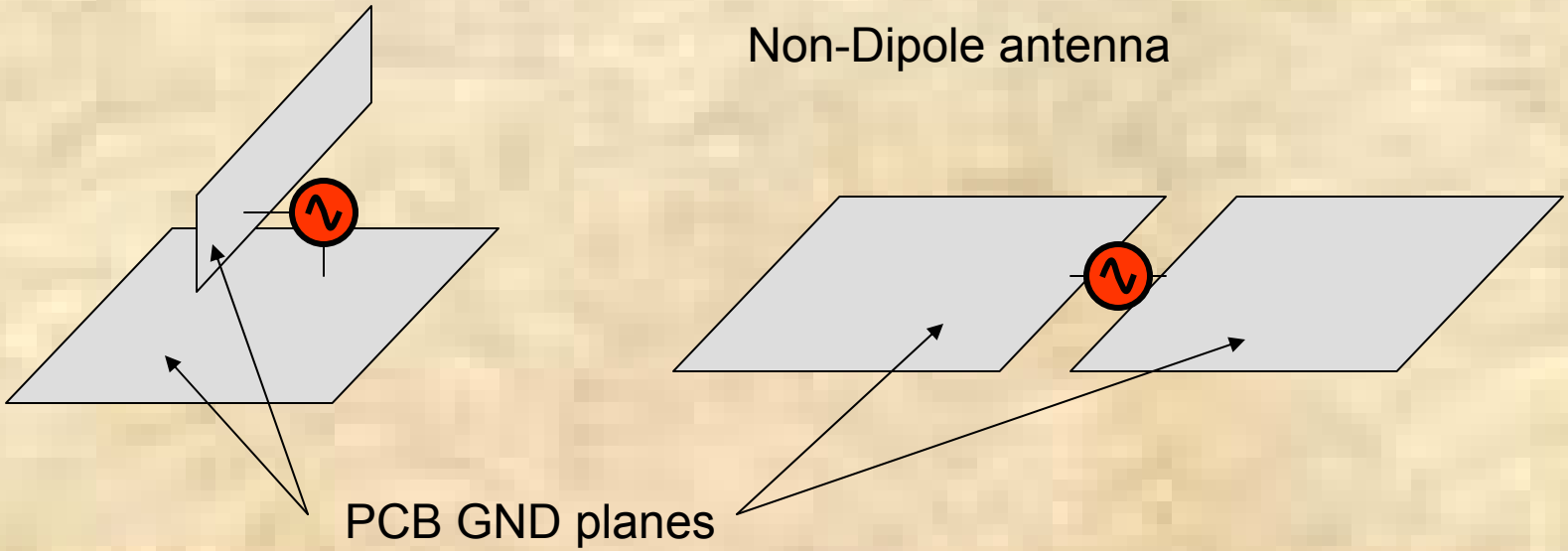


205 mV P-P

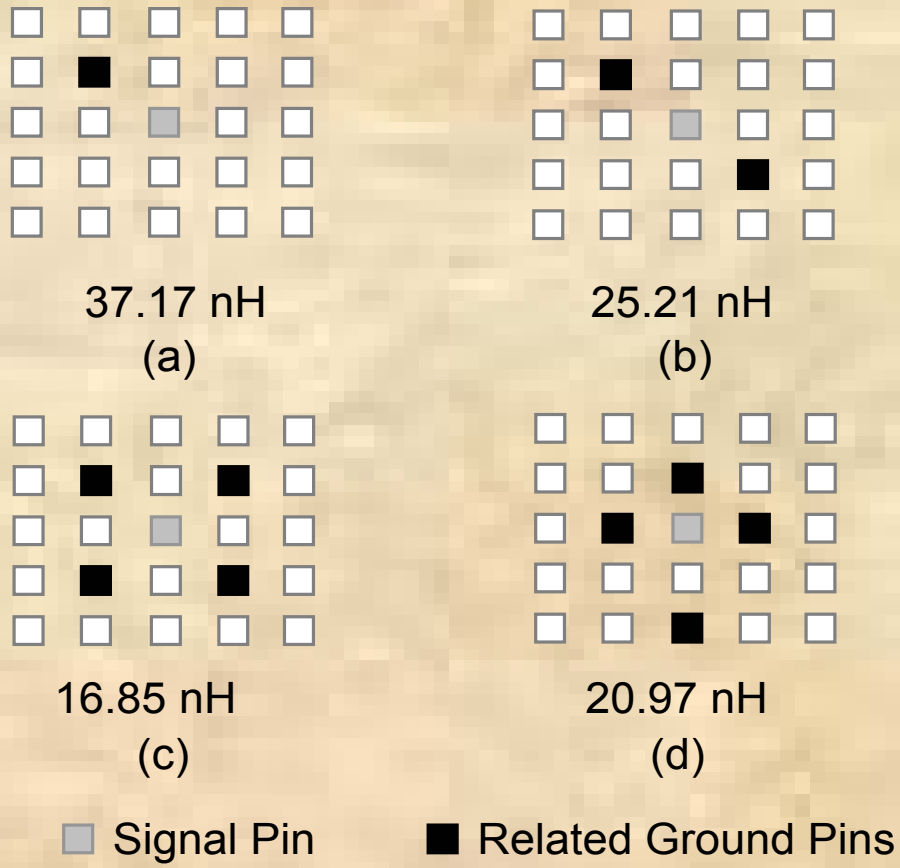
Antenna Structures

Dipole antenna

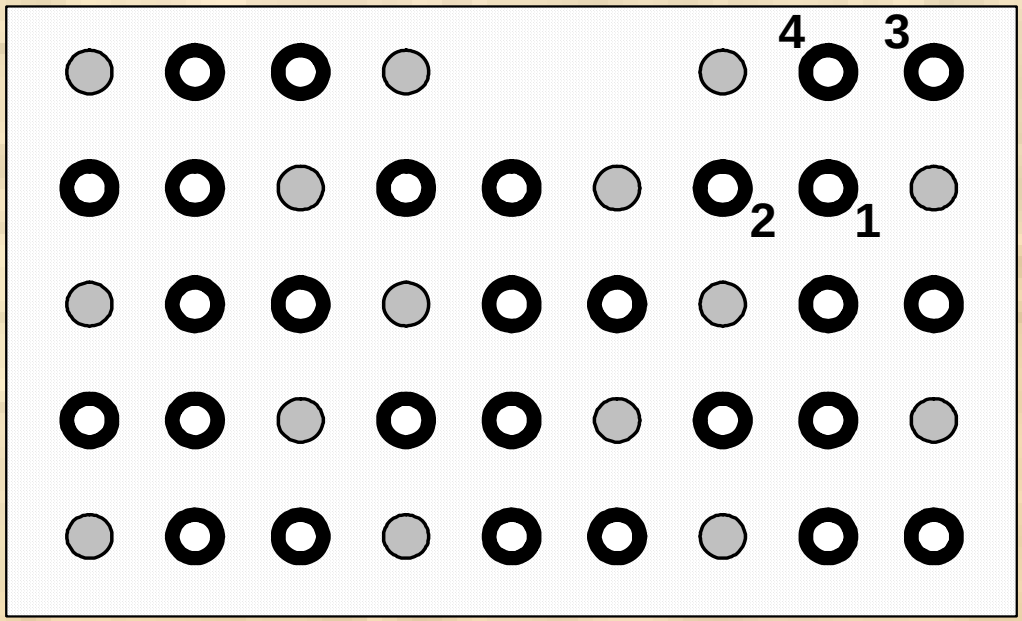
Non-Dipole antenna



Pin Assignment Controls Inductance for CM signals



Different pins within Same Pair may have Different Loop Inductance for CM



pin 1 -- 26.6nH

pin 2 -- 23.6nH

pin 3 -- 31.8nH

pin 4 -- 28.8nH

PCB Layout

Thought Process

- Intentional Signals
  - Clock
  - Buss
  - I/O
  - Video
- Unintentional Signals
  - Common Mode Currents
  - Cross Talk Coupling
  - Power Plane Bounce
  - Above Board Structures

Potential Problems

- Intentional Signals
  - Loop Mode
  - Common Mode
- Unintentional Signals
  - Common Mode
  - Crosstalk Coupling
  - Power Plane Bounce
  - Above Board Structures

So….. What can we do up front??

Design on ***PURPOSE***

not by Magic!!

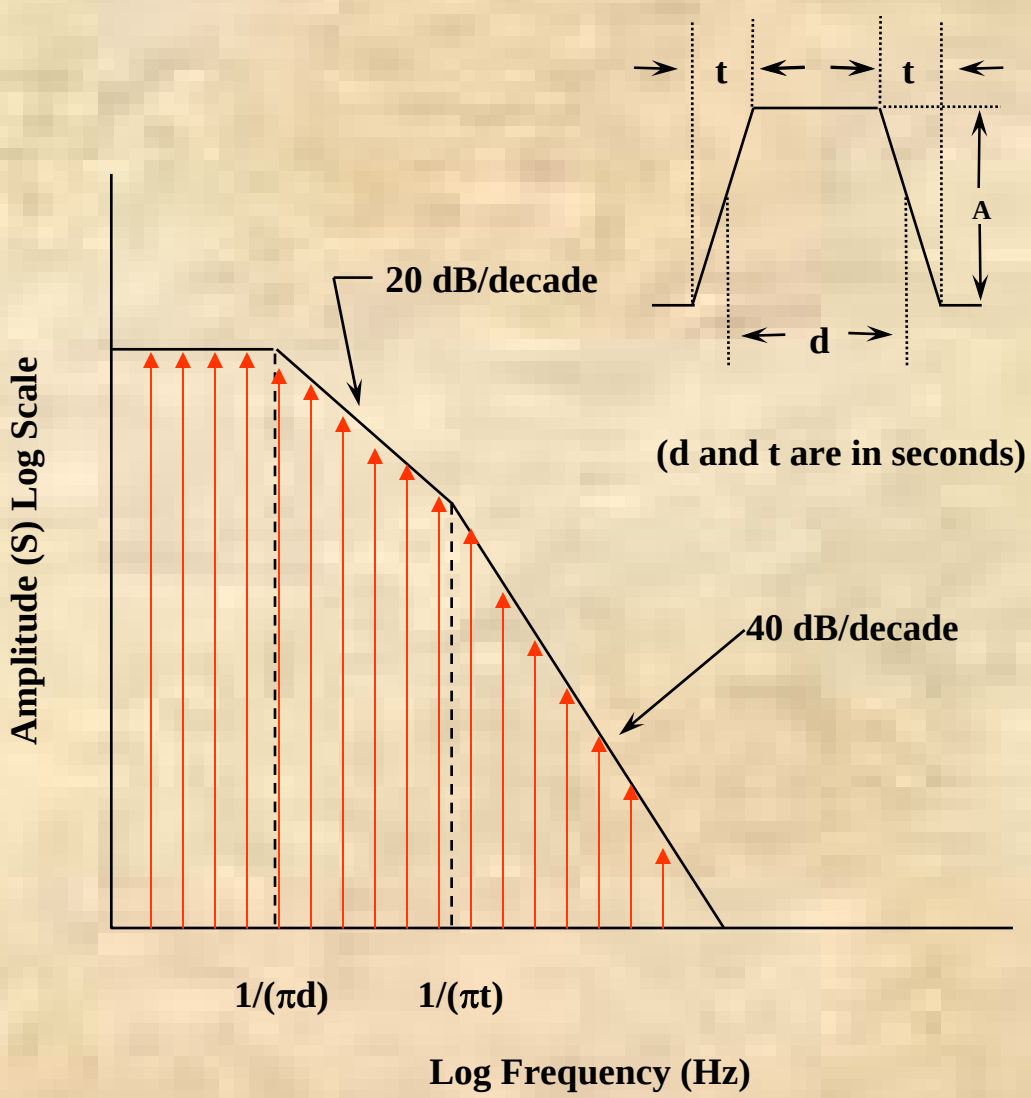
Intentional Signal Emissions

- Loop Mode
  - *Intentional* signal current travels down trace to receiver
  - Assume return current flows directly under trace in reference plane
  - Microstrip creates small loop antenna

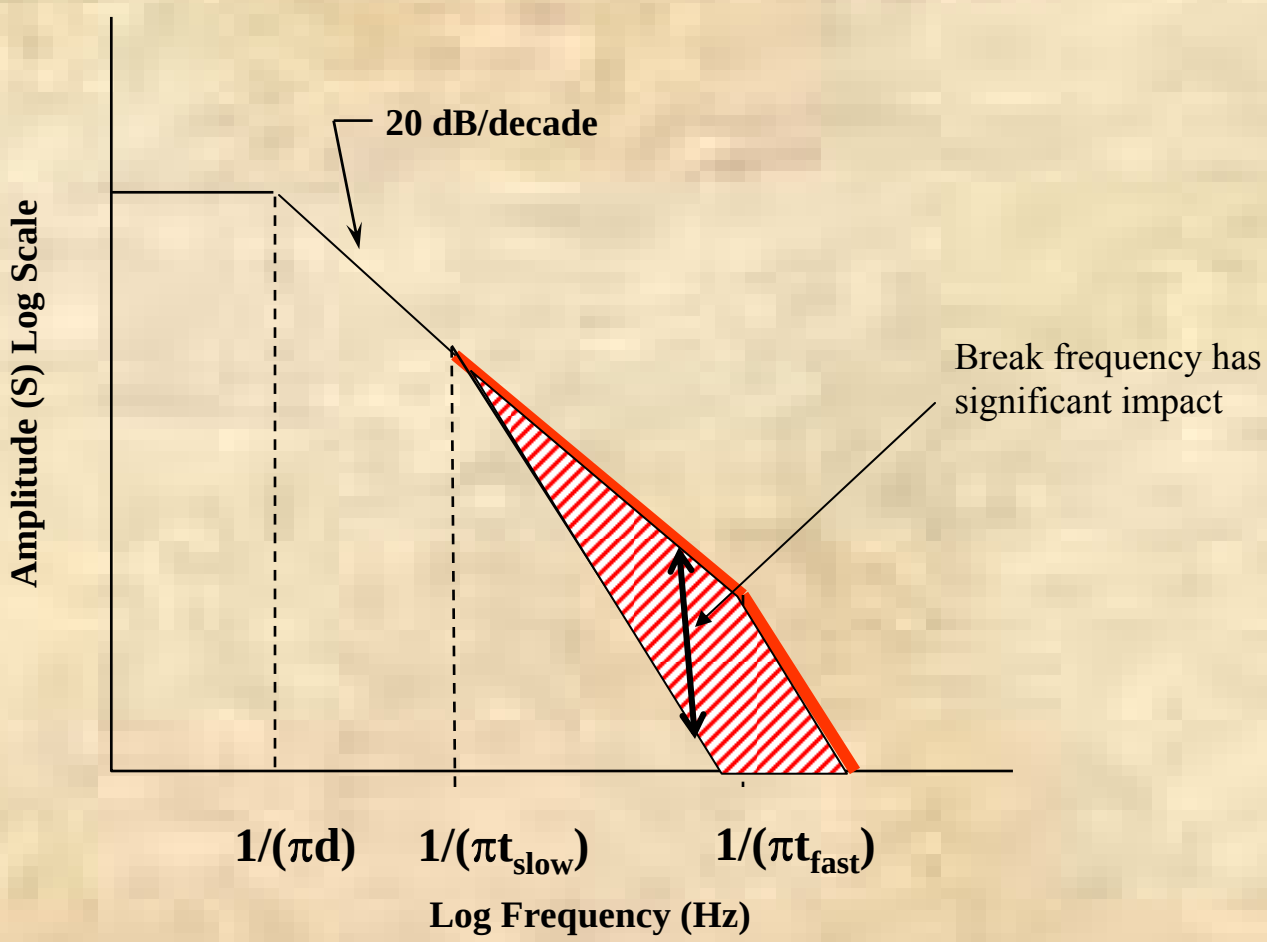
What is the *Intentional* Signal?

- bit rate
- rise time
- not enough information!

Rule of Thumb for Spectral Envelope

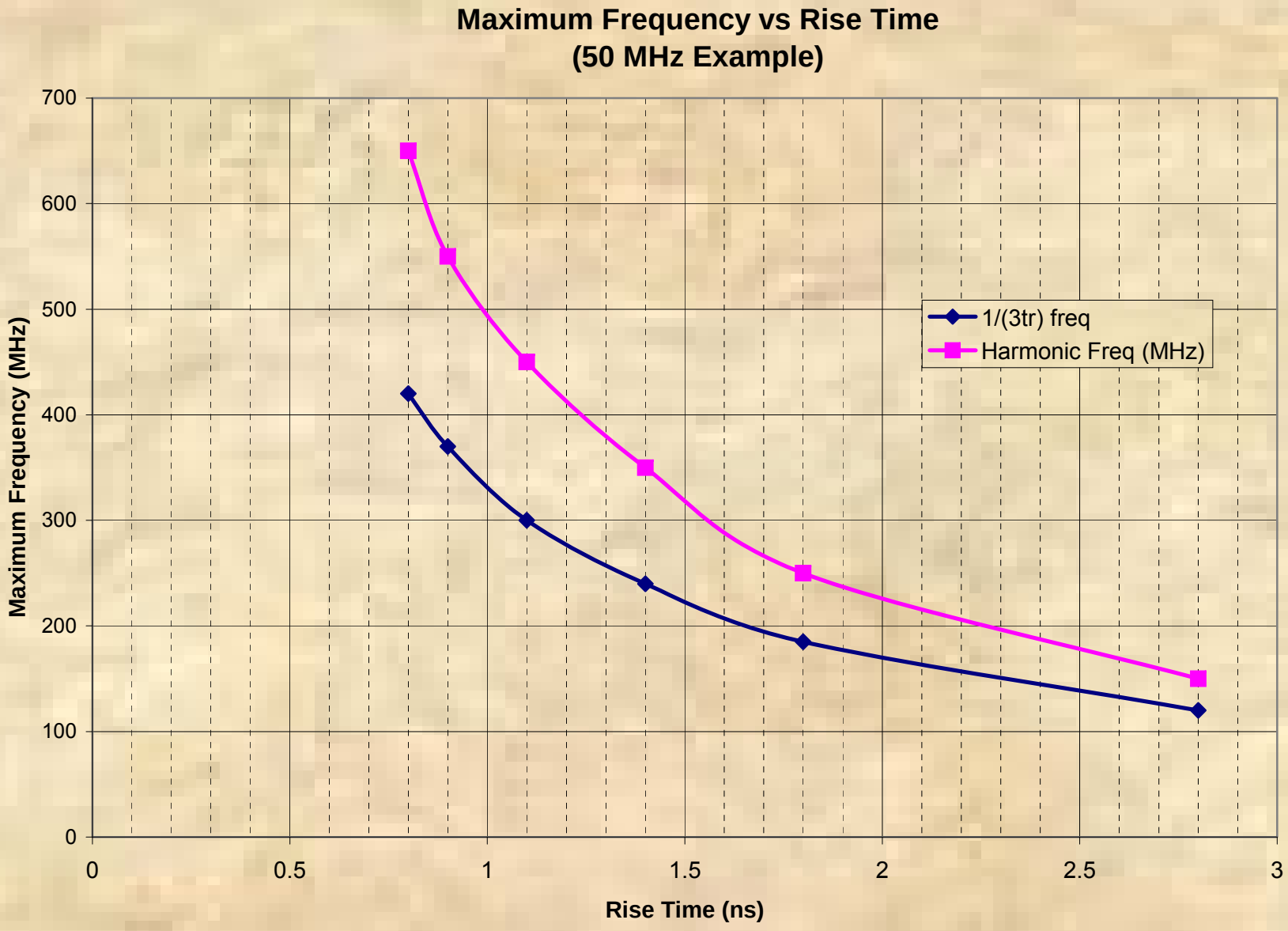


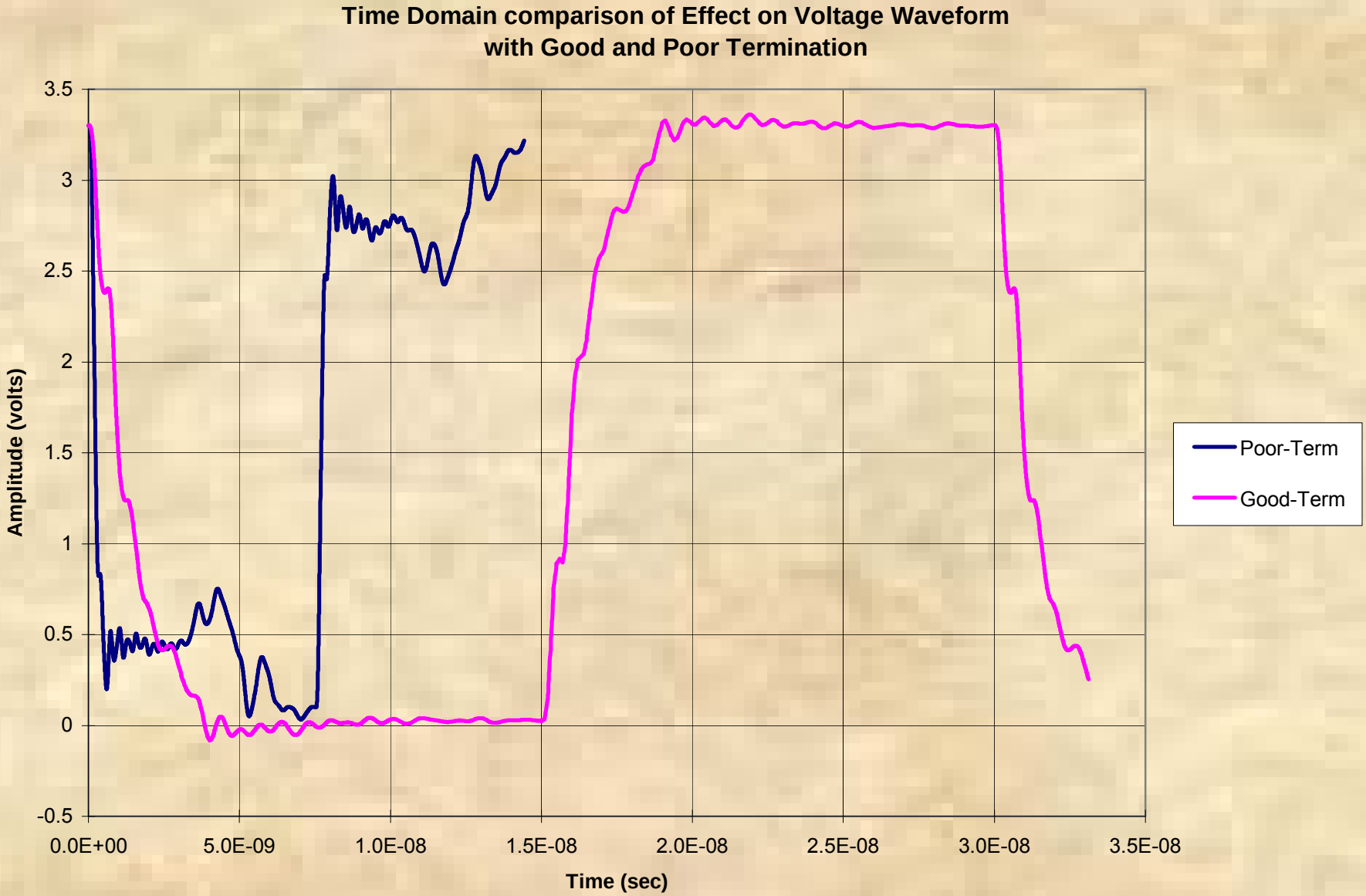
Faster Rise Time gives higher Frequency Harmonics!



Real Intentional Signal

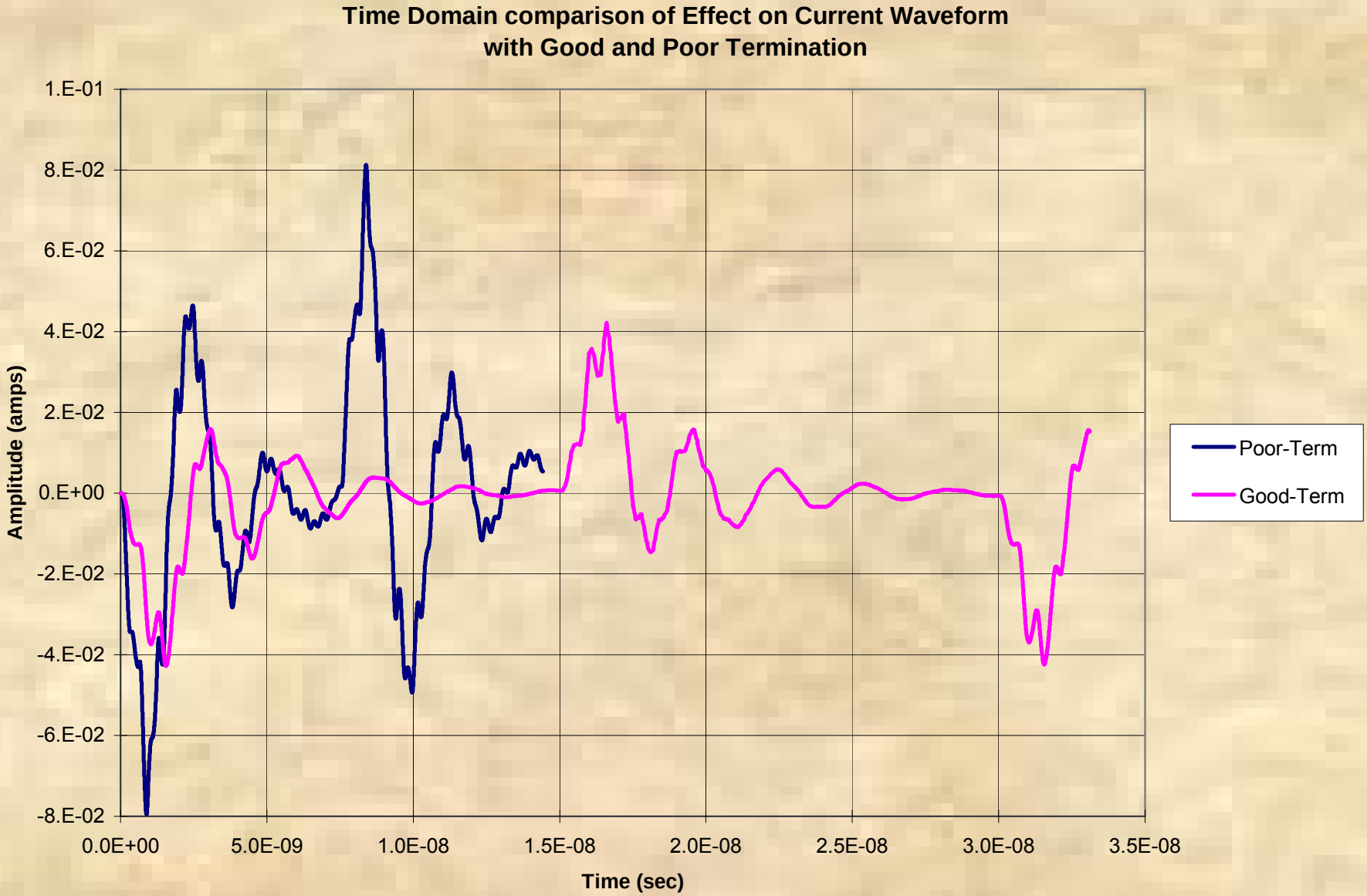
- Note that F_{max}= .35/risetime is not high enough!
- Previous guidelines is only a starting point
  - Real world is much different
- Significant over/under shoot!
- example

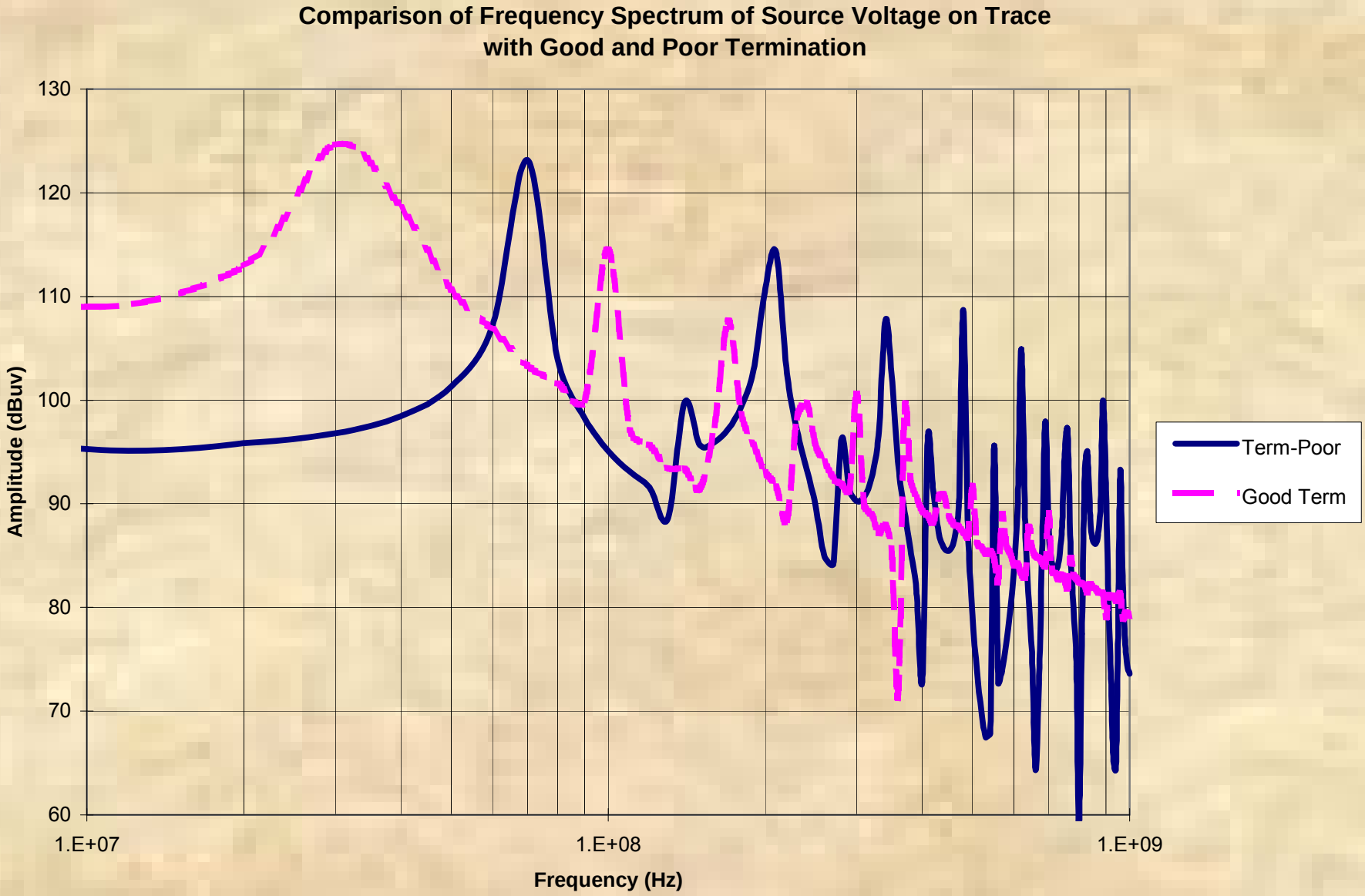

Maximum Frequency vs Rise Time
(50 MHz Example)
Maximum Frequency (MHz)
700
600
500
400
300
200
100
0
0
0.5
1
1.5
2
2.5
3
Rise Time (ns)
1/(3tr) freq
Harmonic Freq (MHz)

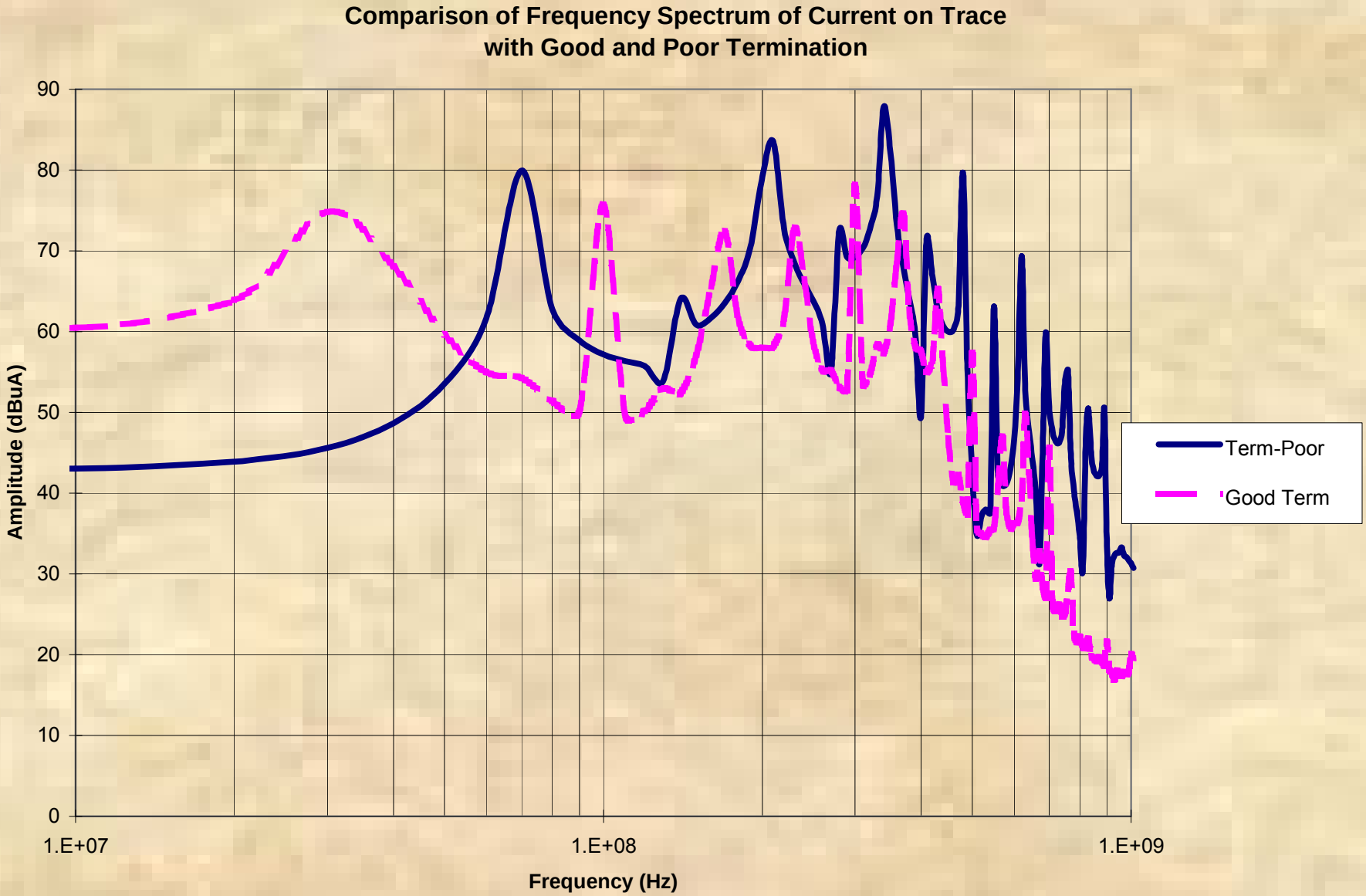

Time Domain comparison of Effect on Voltage Waveform
with Good and Poor Termination
Amplitude (volts)
3.5
3
2.5
2
1.5
1
0.5
0
-0.5
0.0E+00
5.0E-09
1.0E-08
1.5E-08
2.0E-08
2.5E-08
3.0E-08
3.5E-08
Time (sec)
Poor-Term
Good-Term

Current Radiates

- Voltage signal important for SI and Functionality
- NOT Important for emissions!
- *Current radiates, not voltage!!!*


Time Domain comparison of Effect on Current Waveform
with Good and Poor Termination
1.E-01
8.E-02
6.E-02
4.E-02
2.E-02
0.E+00
-2.E-02
-4.E-02
-6.E-02
-8.E-02
Amplitude (amps)
0.0E+00
5.0E-09
1.0E-08
1.5E-08
2.0E-08
2.5E-08
3.0E-08
3.5E-08
Time (sec)
Poor-Term
Good-Term


Comparison of Frequency Spectrum of Source Voltage on Trace with Good and Poor Termination
Amplitude (dBuv)
130
120
110
100
90
80
70
60
1.E+07
1.E+08
1.E+09
Frequency (Hz)
Term-Poor
Good Term


Comparison of Frequency Spectrum of Current on Trace
with Good and Poor Termination
Amplitude (dBuA)
90
80
70
60
50
40
30
20
10
0
1.E+07
1.E+08
1.E+09
Frequency (Hz)
Term-Poor
Good Term

- Risetime often controlled by Signal Integrity constraints -- can't be slowed down
- Other 'noise' is caused by imperfect termination
- More details on this later

Radiation from Traces

- Who cares about the far field?
  - using shielded boxes
  - even in unshielded products, most emissions are from cables
- Near field can excite shielded box resonances
  - resonant frequency can be anything
  - changes with placement of inside stuff

How can we find the near field 2” above a board?

Board with 10” microstrip

Hertzian Dipole Approach

$$E_\theta = \frac{IL\sin\theta}{4\pi\varepsilon_0}\left(\frac{j\omega}{c^2 r} + \frac{1}{cr^2} + \frac{1}{j\omega r^3}\right)$$

Break trace into small segments

Hertzian Dipole Approach

- Previous equation reduces to
  - Electric Field = ***Current*** * ***Length*** * Constant

Near Radiated Fields above Board

- For a single clock net
- Near Electric Field is Linear with Current
  - 20 dB difference in Current means 20 dB difference in Electric Field!
  - Termination makes a Big Difference!

Intentional Signal Analysis

- Most EMC problems come from common-mode currents
- All common mode currents are caused by intentional signals
- Signal Integrity tools now allow analysis of current spectrum
- Reduce high frequency harmonics on the current to lower EMC common mode currents!

Why fight an emission problem which is due to a current that is not required?!

- A little extra analysis
- Use tools already available
- cost of different value resistors is equal
  - Therefore, reducing emissions by termination control is ***FREE*** !!!

Effect of Exposed Length reduced to 3”

- Using Same Spectrum of Current
- Near Electric field is linear with trace length
  - Reducing exposed length from 12” to 3” reduces electric field by factor of 4 (12 dB)!

Potential Problems

- Intentional Signals
  - Loop Mode
  - Common Mode
- Unintentional Signals
  - Common Mode
  - Crosstalk Coupling
  - Power Plane Bounce
  - Above Board Structures

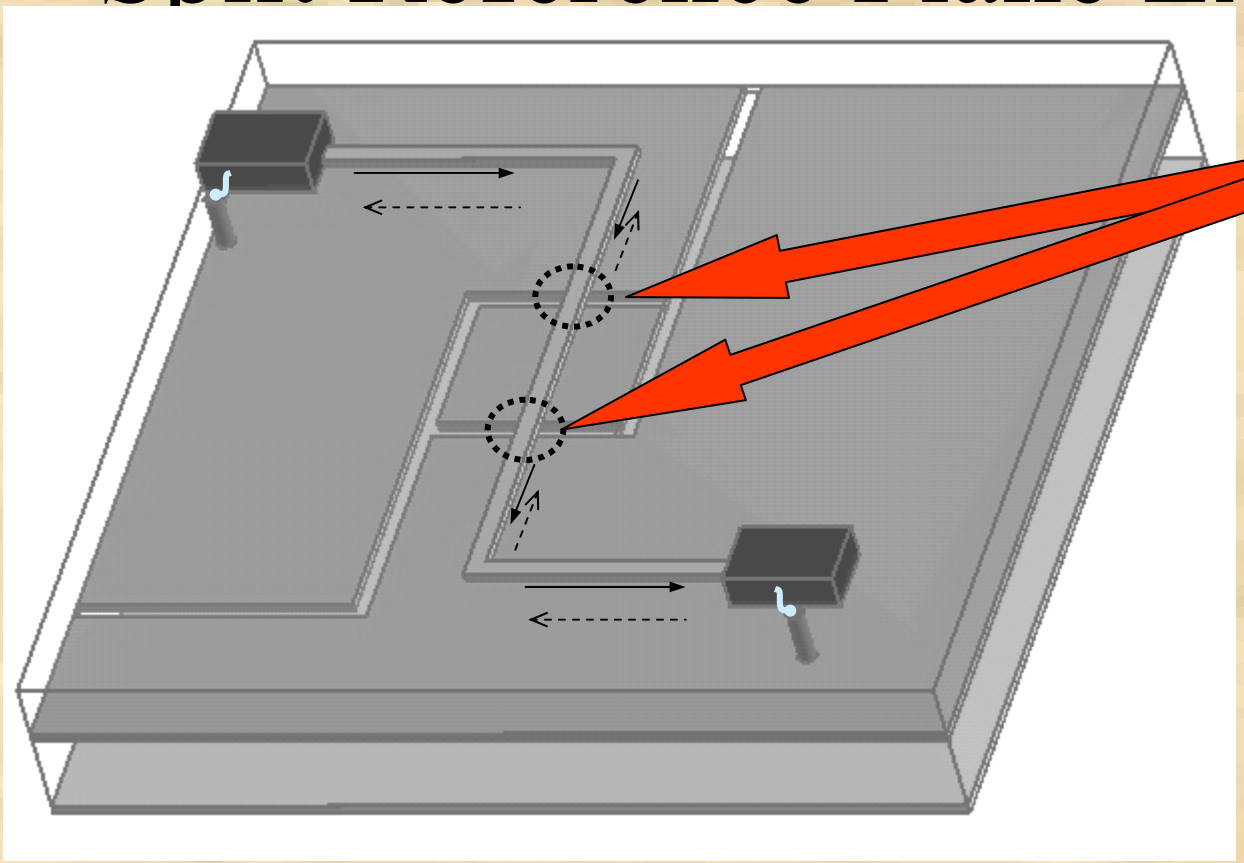
When Reference Plane not perfect

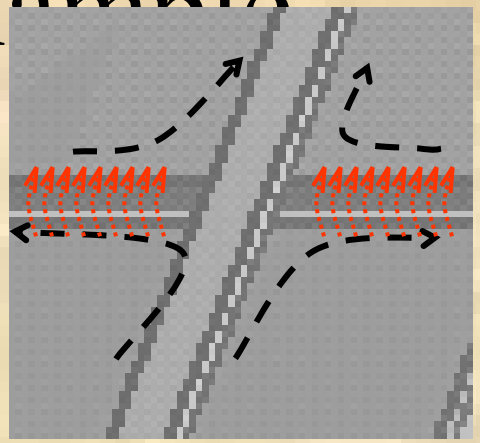
- Splits in power plane?
- Traces across split

Splits in Reference Plane

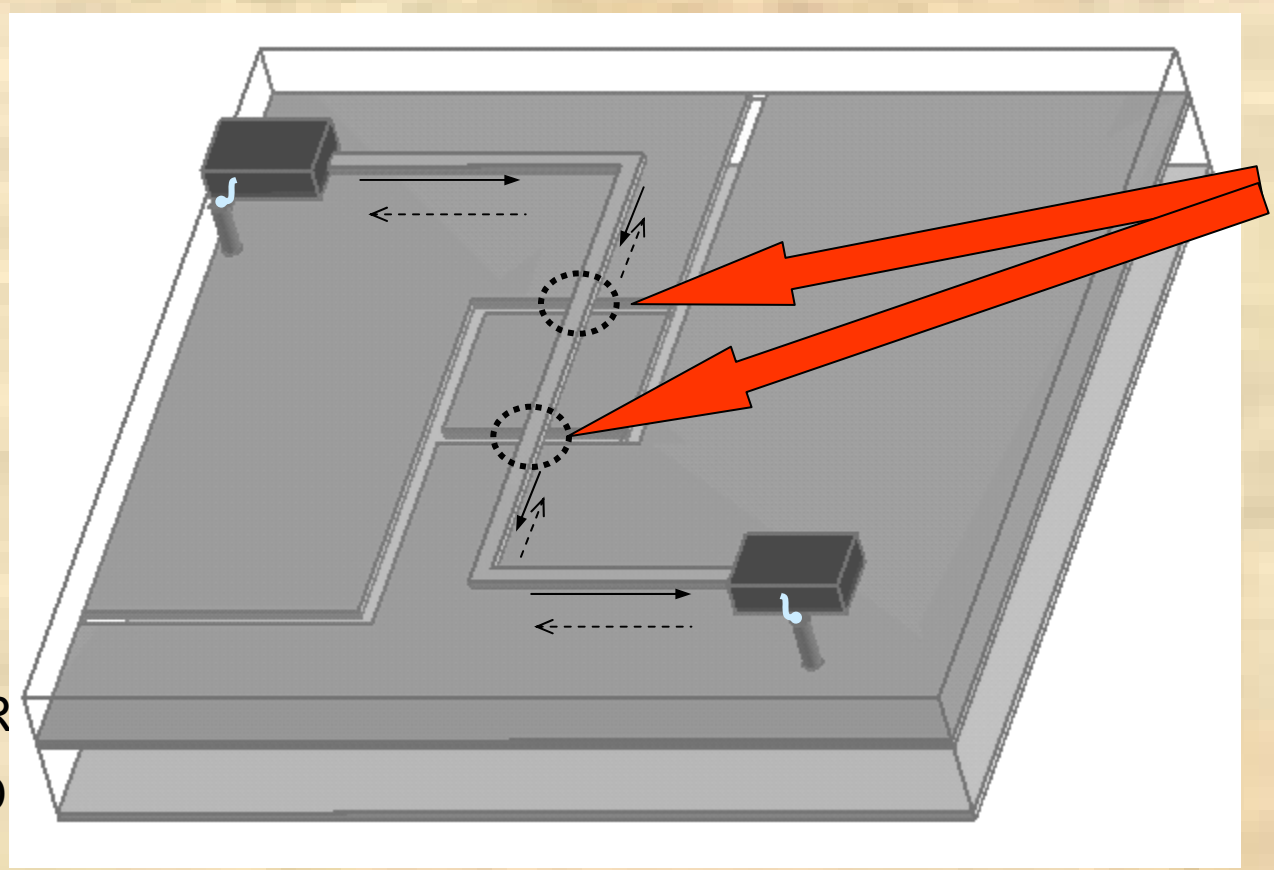
- Power planes often have splits
- Return current path interrupted
- Consider spectrum of clock signal
- Consider stitching capacitor impedance
- High frequency harmonics not returned directly

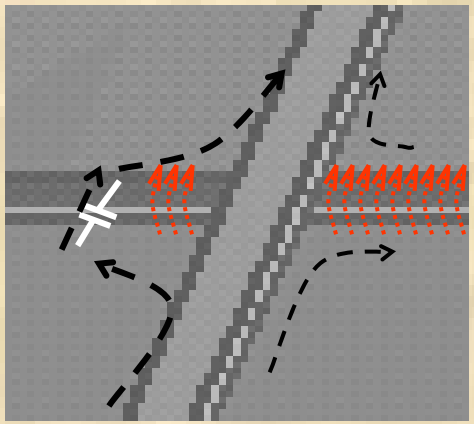
Split Reference Plane Example





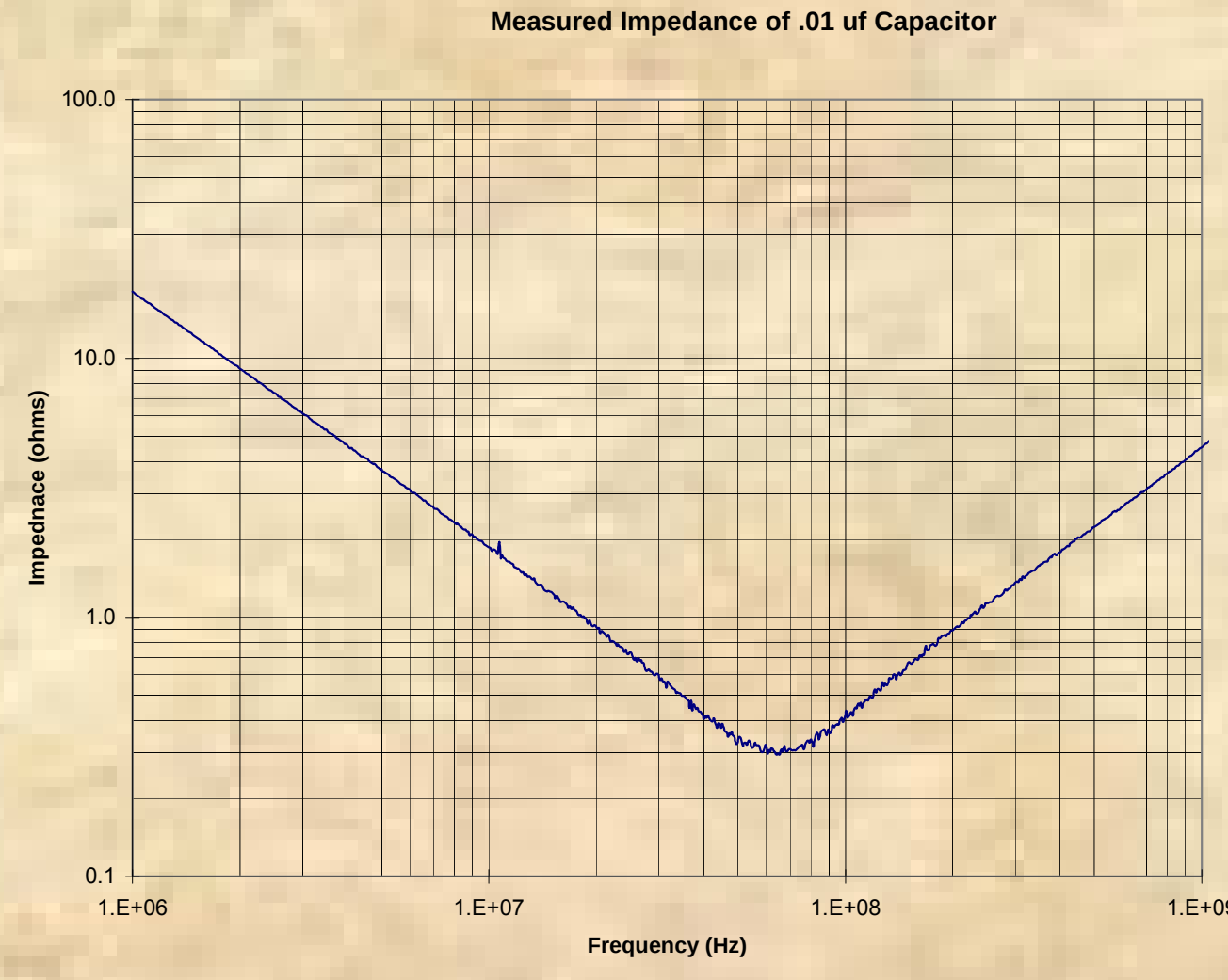
Split Reference Plane Example With Stitching Capacitors

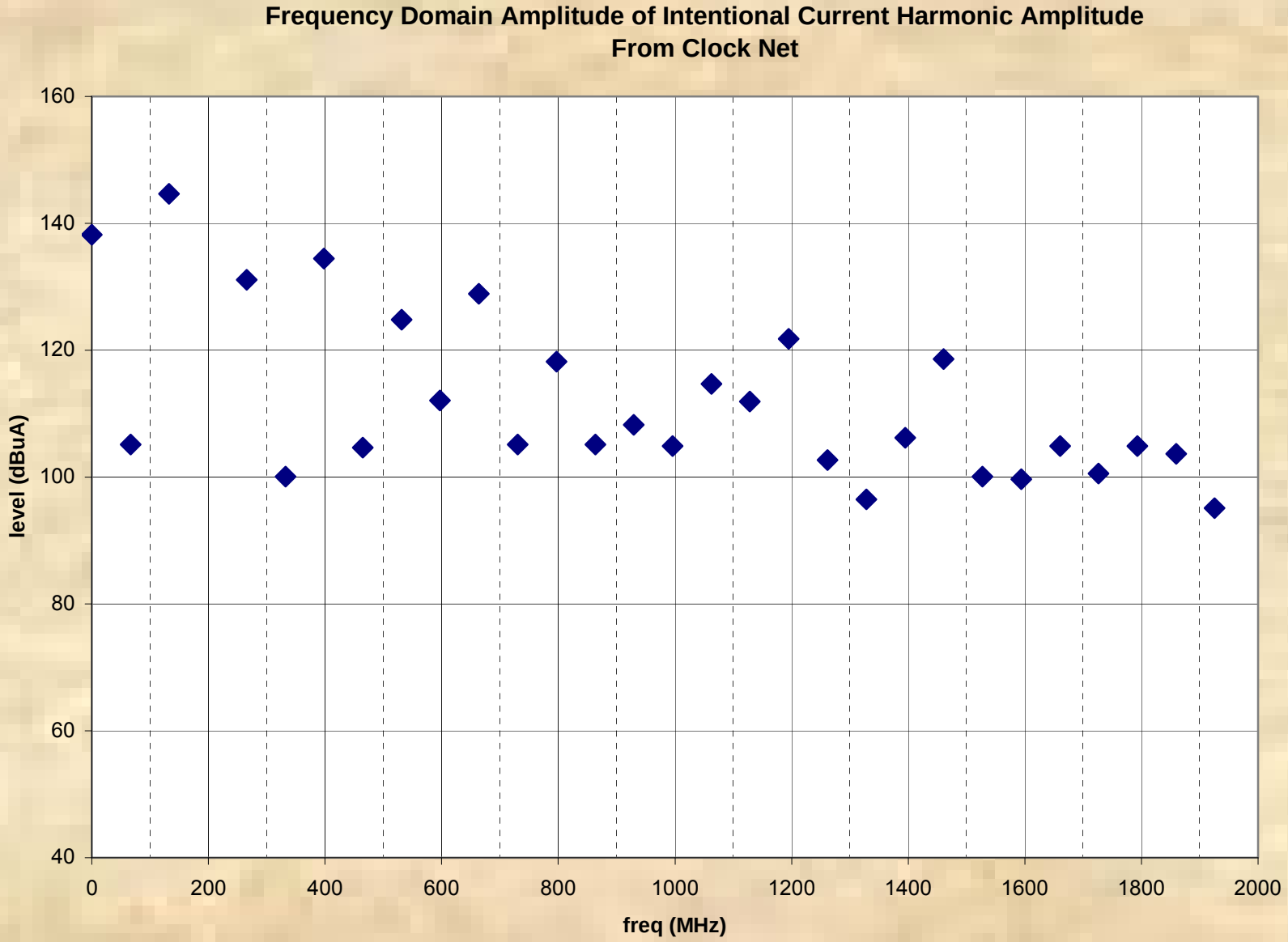




Stitching Capacitors Allow Return current to Cross Splits ???

Capacitor Impedance

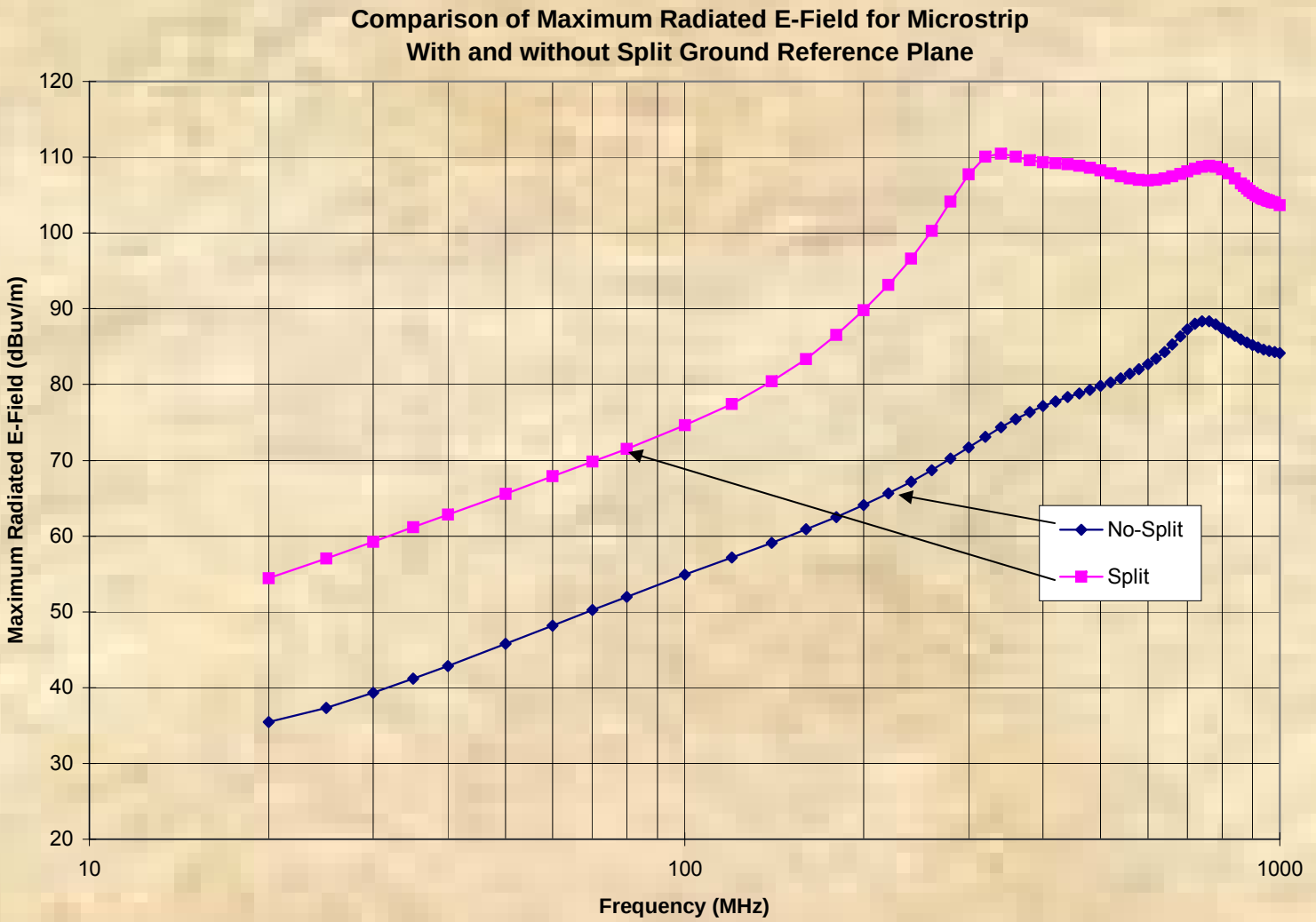



Frequency Domain Amplitude of Intentional Current Harmonic Amplitude
From Clock Net
level (dBuA)
160
140
120
100
80
60
40
0
200
400
600
800
1000
1200
1400
1600
1800
2000
freq (MHz)

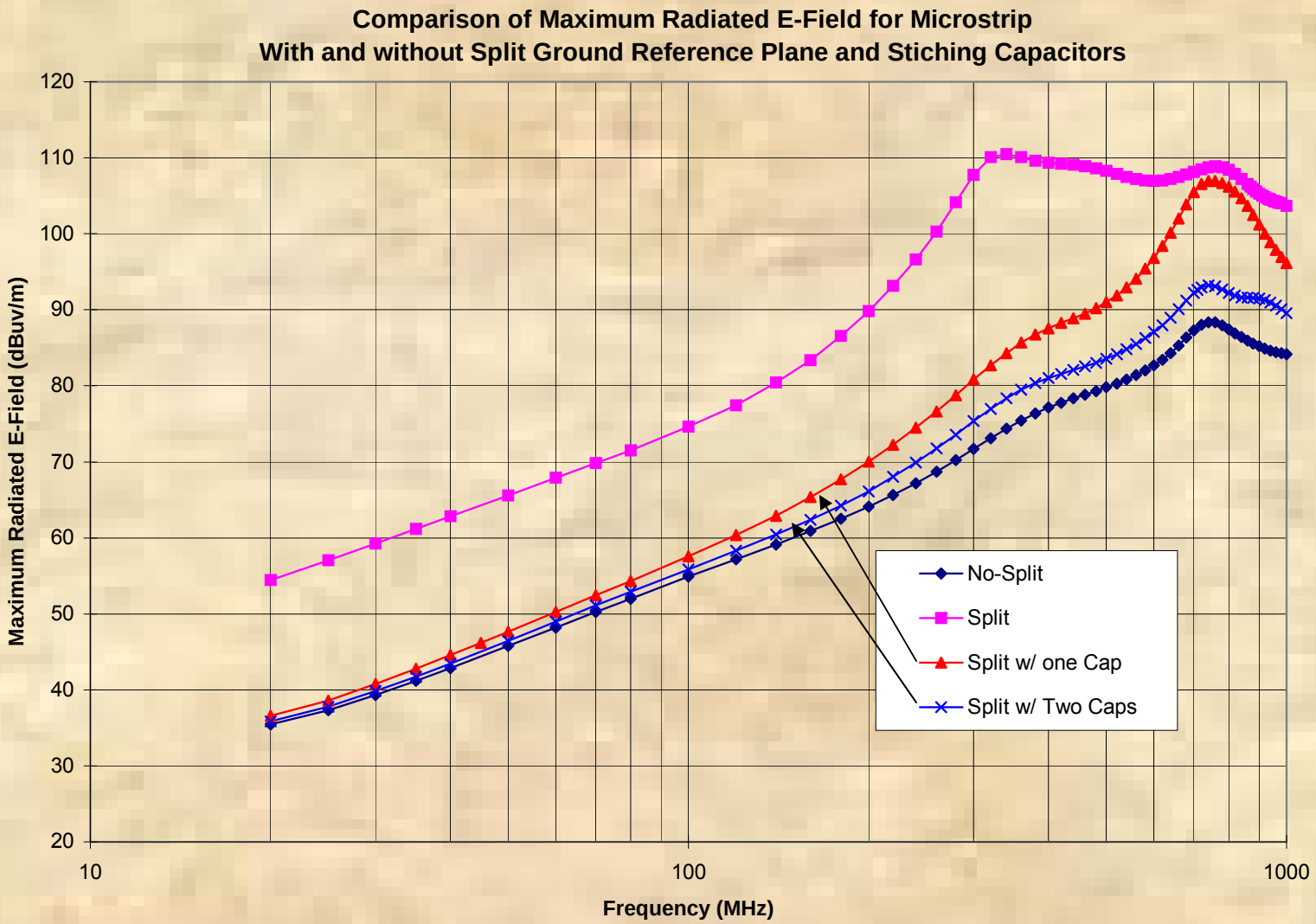
Are Stitching Capacitors Effective ???

- YES, at low frequencies
- No, at high frequencies
- Need to limit the high frequency current spectrum
- Need to avoid split crossings with ALL critical signals

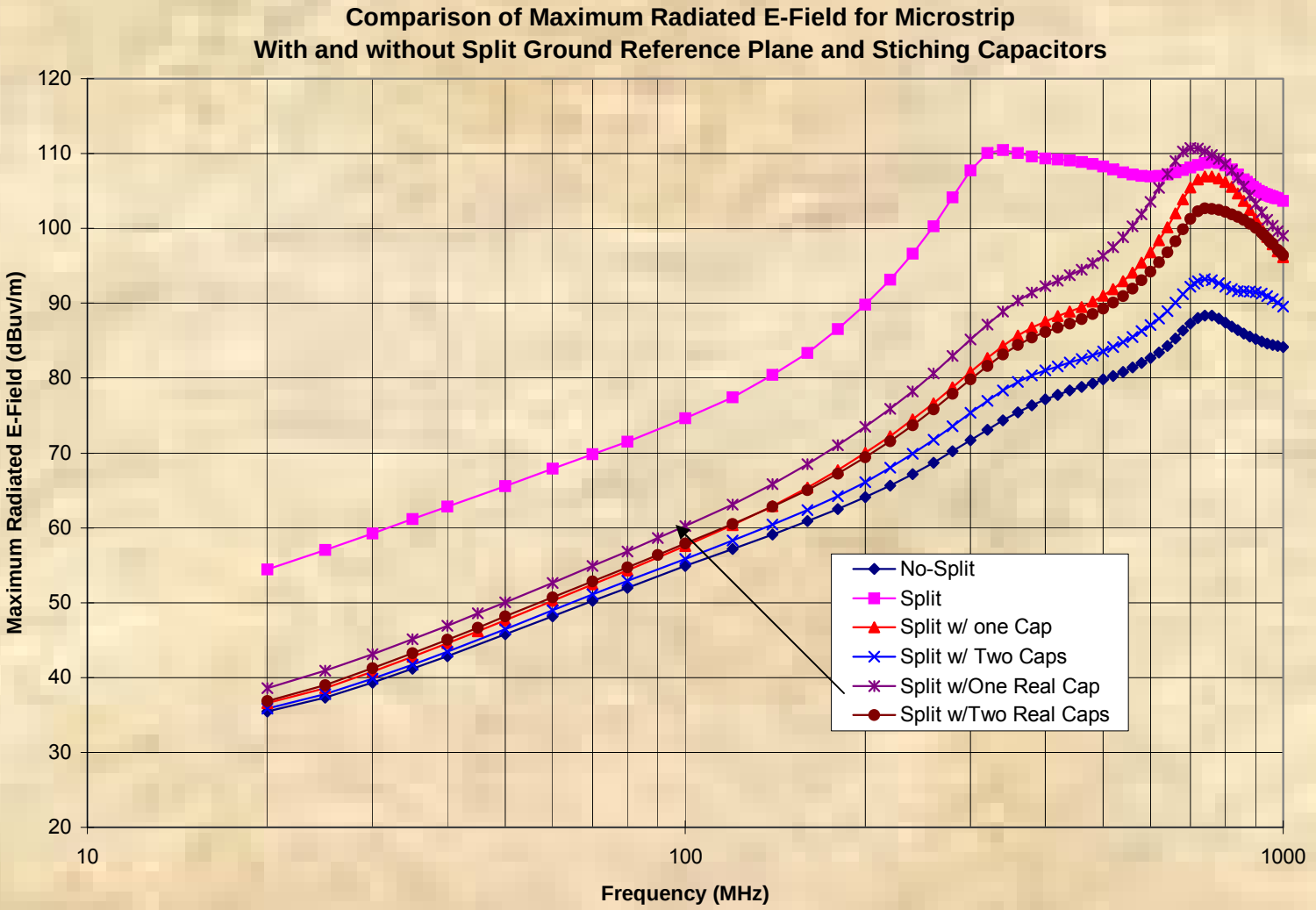
Near Field Radiation from Microstrip on Board with Split in Reference Plane



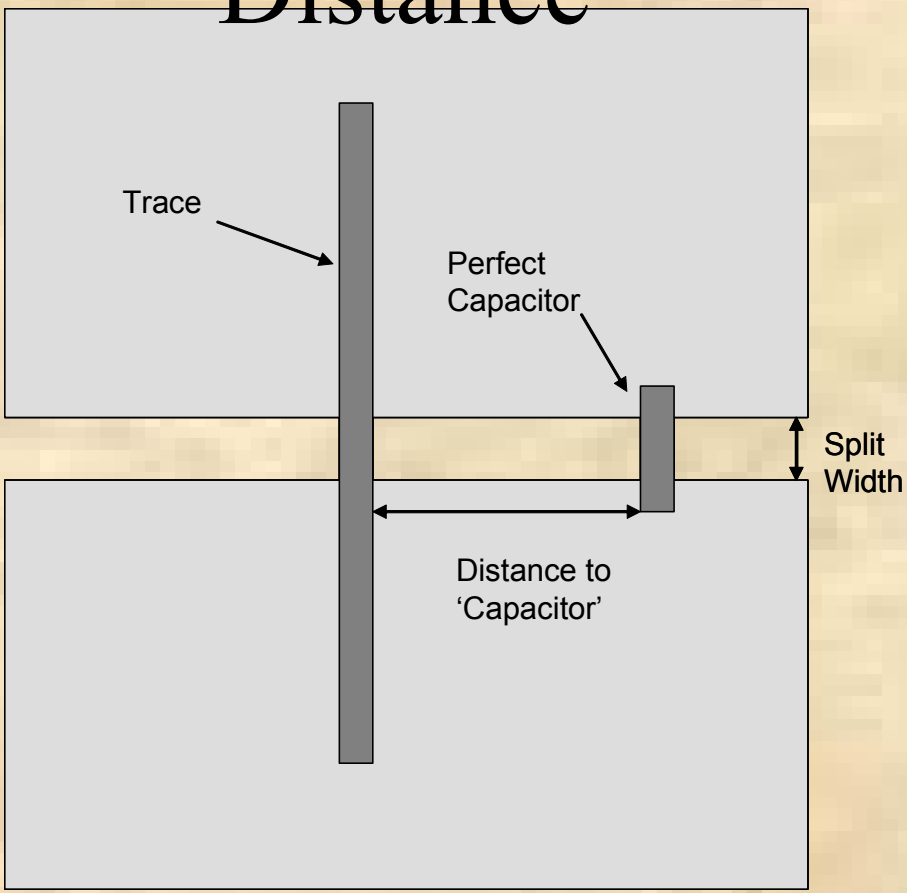
With "Perfect" Stitching Capacitors Across Split



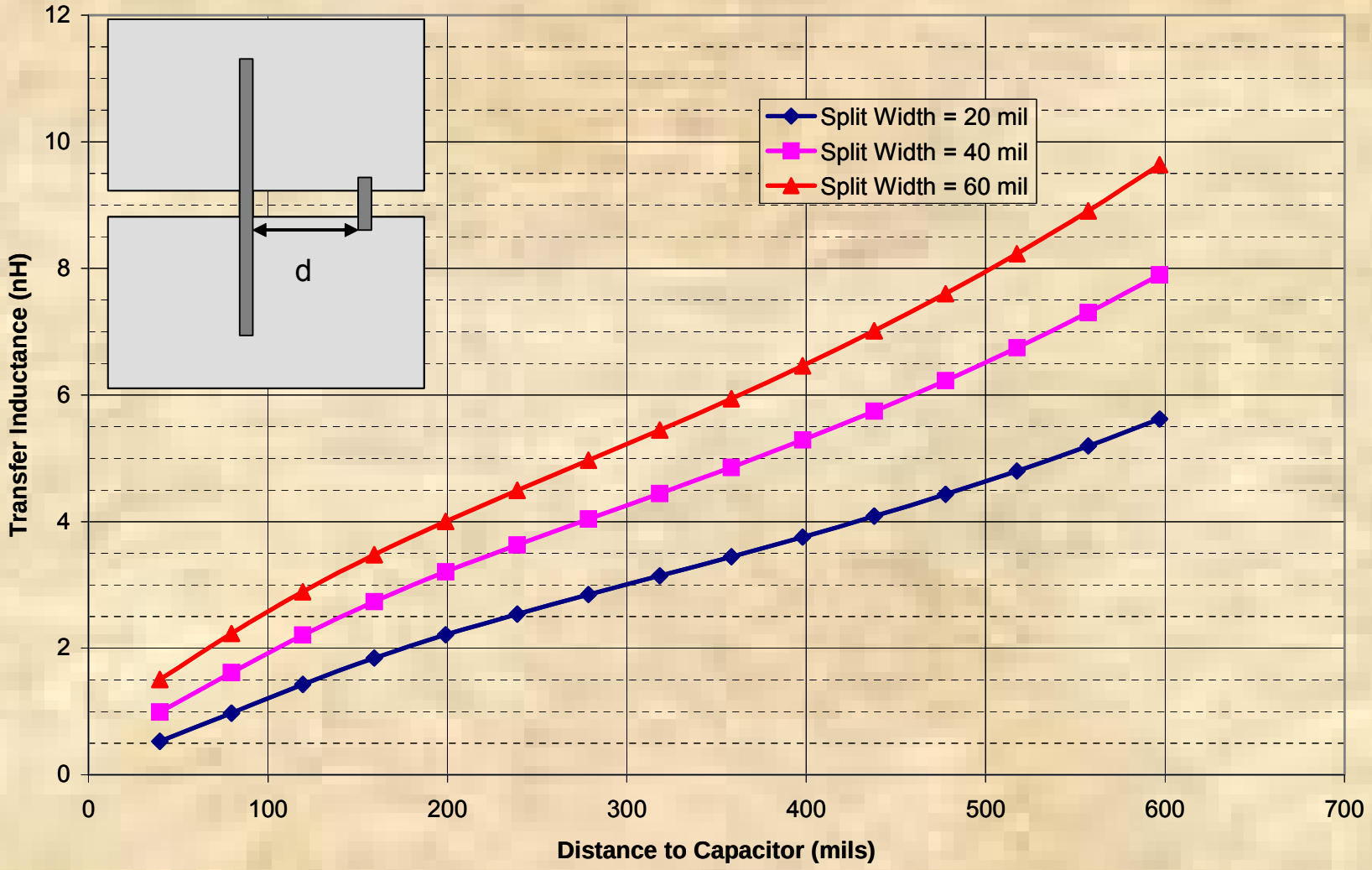
Stitching Caps with Inductance and Via Inductance

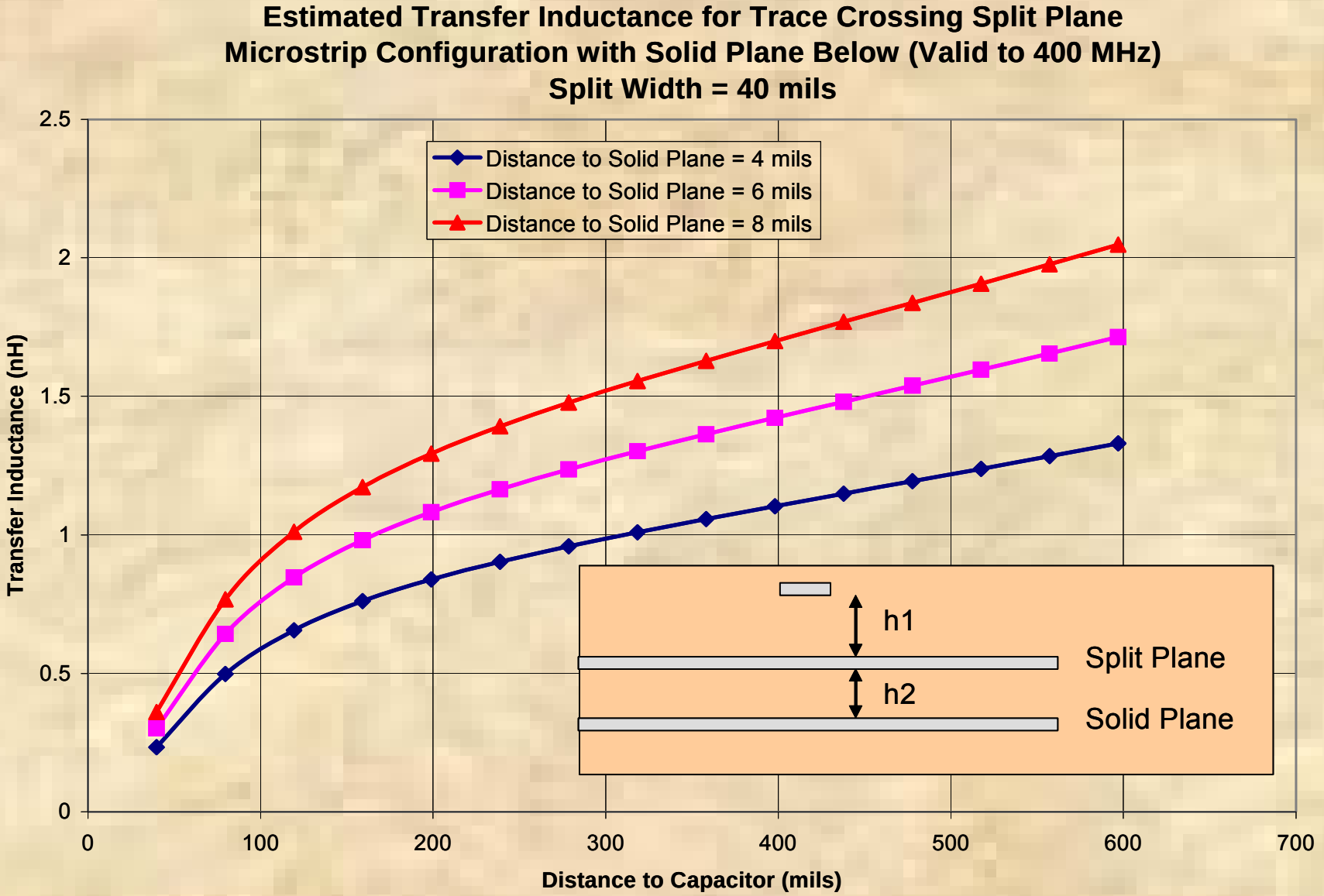


Effect of Stitching Capacitor Distance

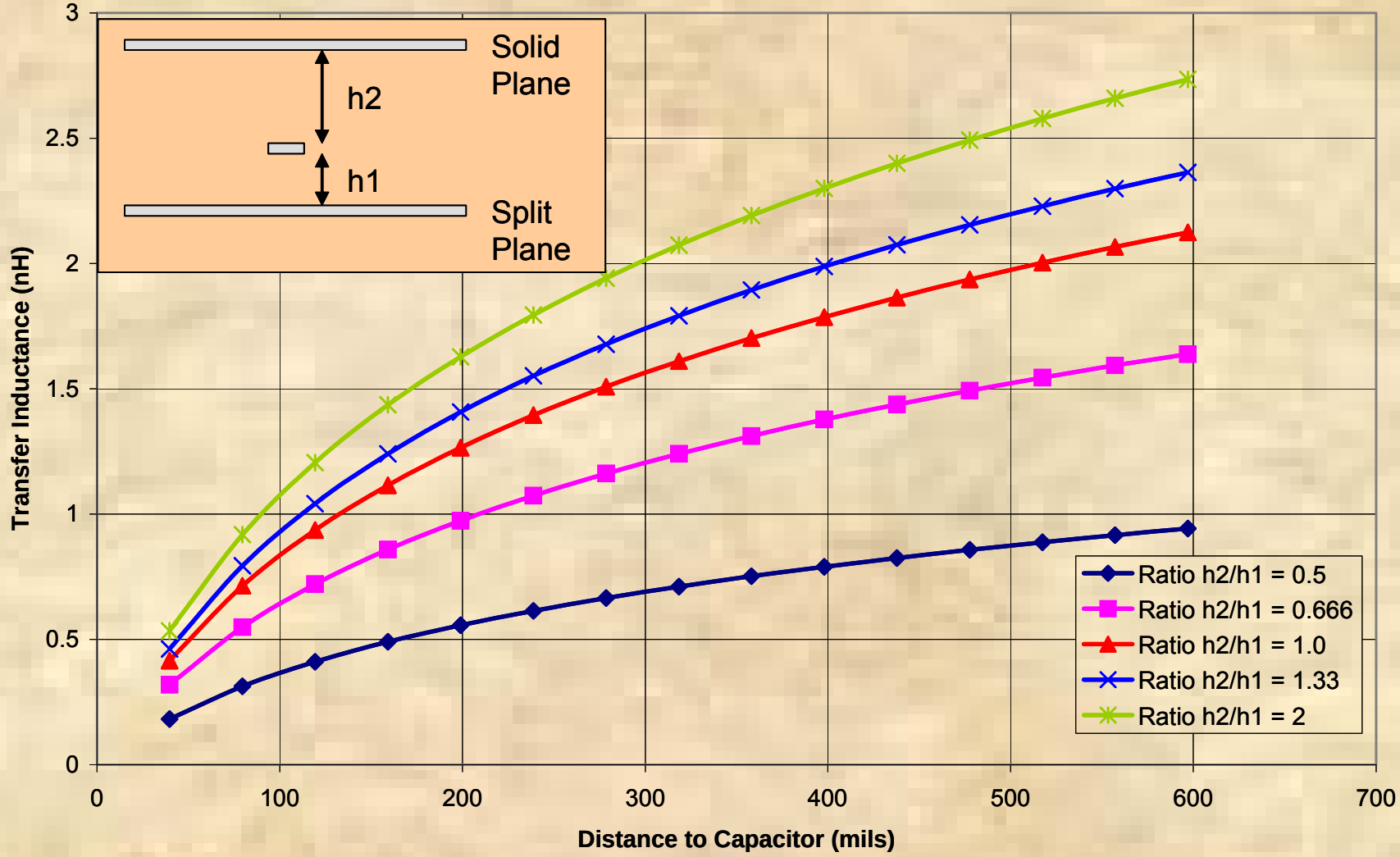


Estimated Transfer Inductance for Trace Crossing Split Plane Microstrip Configuration (Valid to 2 GHz)

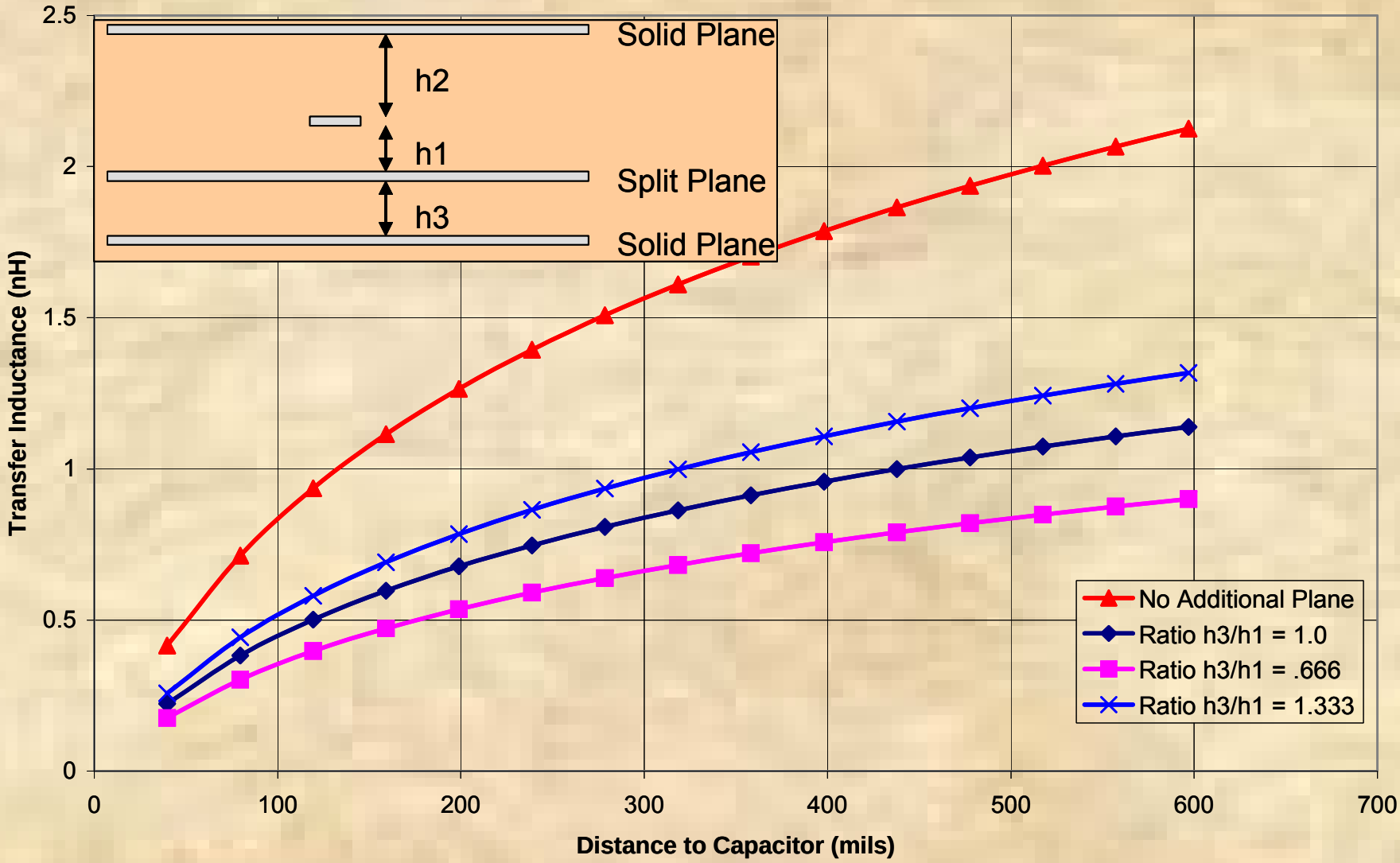



Estimated Transfer Inductance for Trace Crossing Split Plane
Microstrip Configuration with Solid Plane Below (Valid to 400 MHz)
Split Width = 40 mils
Distance to Solid Plane = 4 mils
Distance to Solid Plane = 6 mils
Distance to Solid Plane = 8 mils
Transfer Inductance (nH)
Distance to Capacitor (mils)
0
0.5
1
1.5
2
2.5
0
100
200
300
400
500
600
700
h1
h2
Split Plane
Solid Plane

Estimated Transfer Inductance for Trace Crossing Split Plane
Stripline Configuration (Valid to 600 MHz)
Split Width = 40 mils (h2=Distance to Solid Plane, h1 = Distance to Split Plane)



Estimated Transfer Inductance for Trace Crossing Split Plane
Symetrical Stripline Configuration (Valid to 600 MHz)
Split Width = 40 mils (h3=Distance to Solid Plane, h1 = Distance to Split Plane)



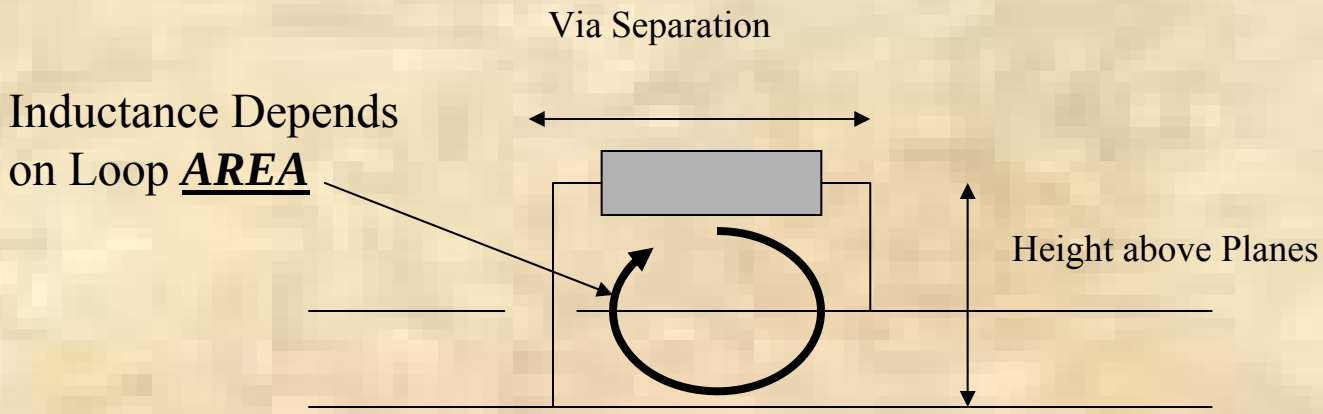
Split Plane videos

- Stitching Cap close to crossing
- Stitching cap far from crossing

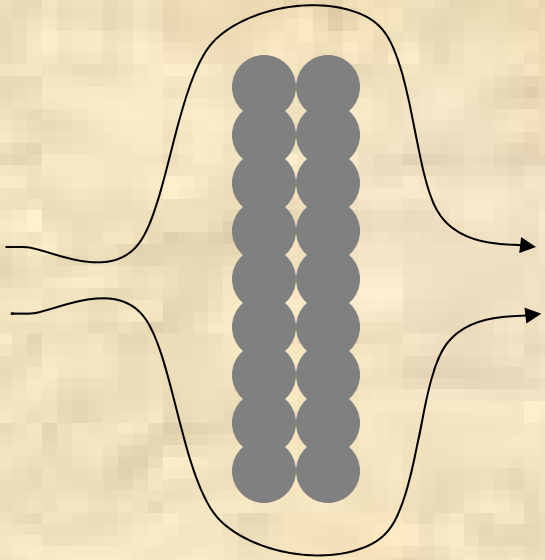
Stitching Capacitor Mounting

Power-to-Power

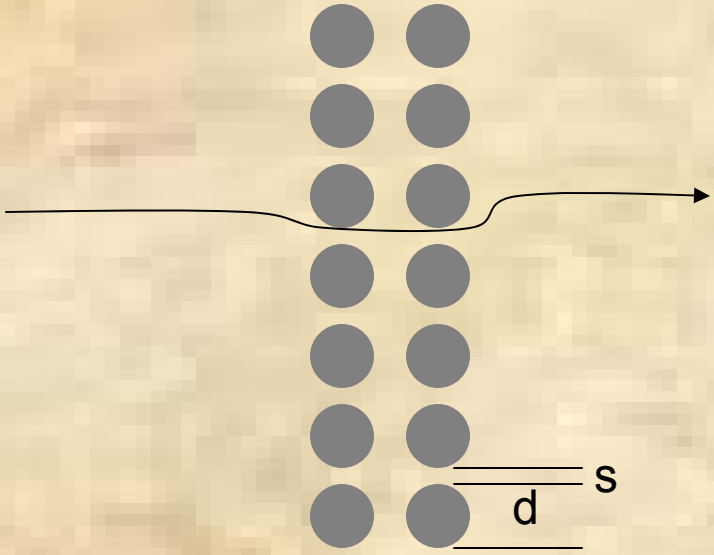
- **Stitching Capacitor Performance at high frequencies depends on connection inductance!**



Pin Field Via Keepouts??



Return Current must go around entire keep out area --- just as bad as a slot



Return current path deviation minimal

Recommend s/d > 1/3

Are Stitching Capacitors Effective ???

- YES, at low frequencies
- No, at high frequencies
- Need to limit the high frequency current spectrum
- Need to avoid split crossings with ALL critical signals

- ***SAME for So-called 'differential' signals!!***

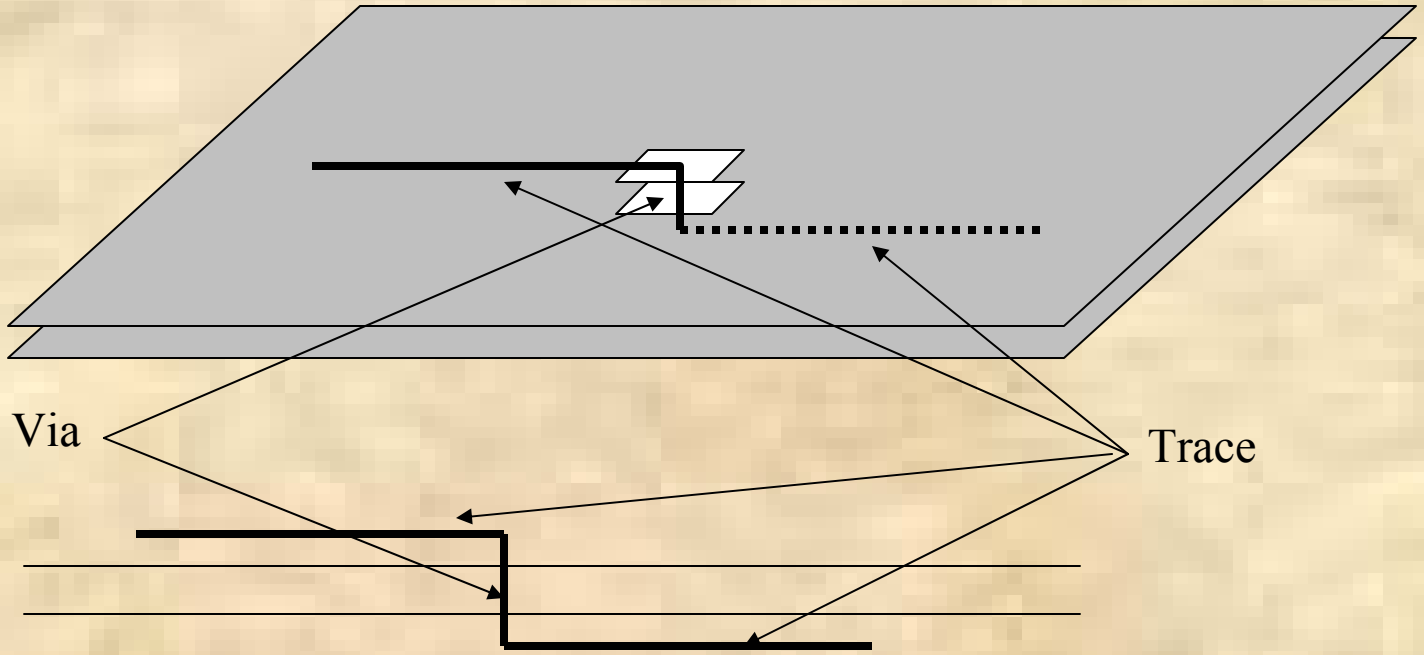
Referencing Nets

(Where does the Return Current Flow??)

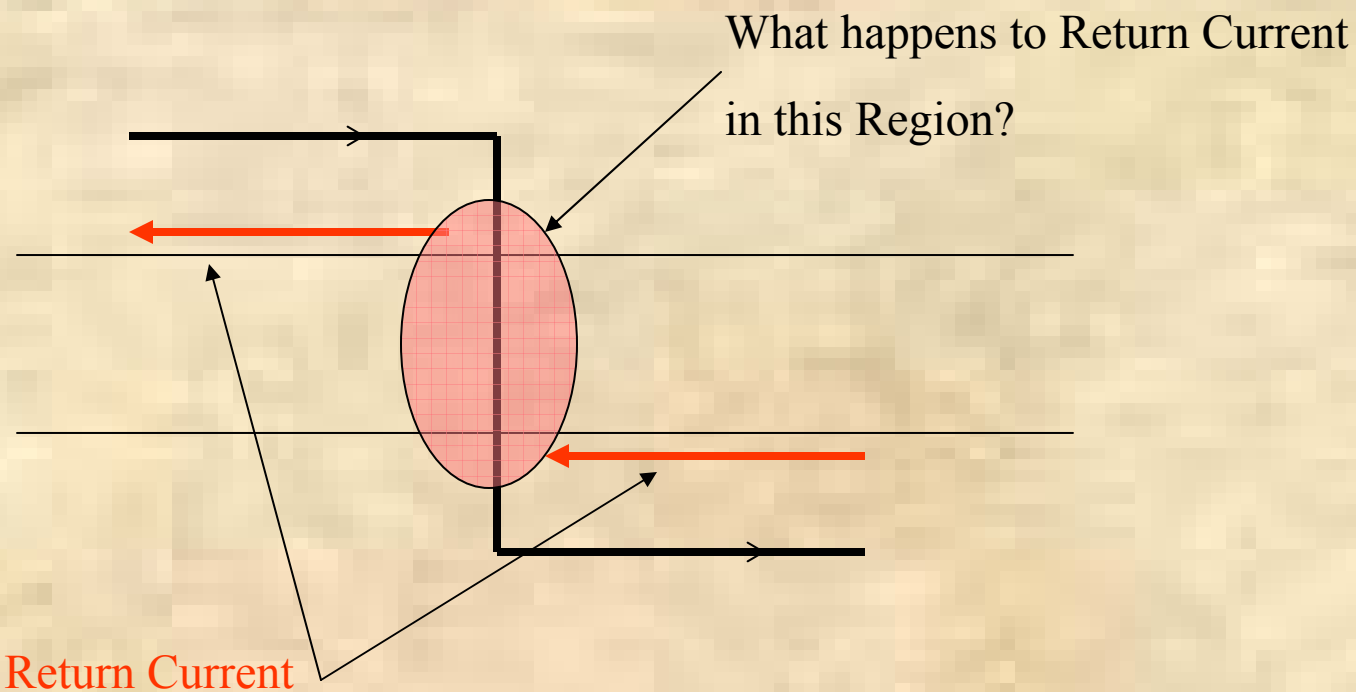
Referencing Nets
(Where does the Return Current Flow??)

- √ Microstrip/Stripline over unbroken reference plane
- √ Microstrip/Stripline across split in reference plane
- Microstrip/Stripline through via (change reference planes)
- Mother/Daughter card

Microstrip/Stripline through via (change reference planes)



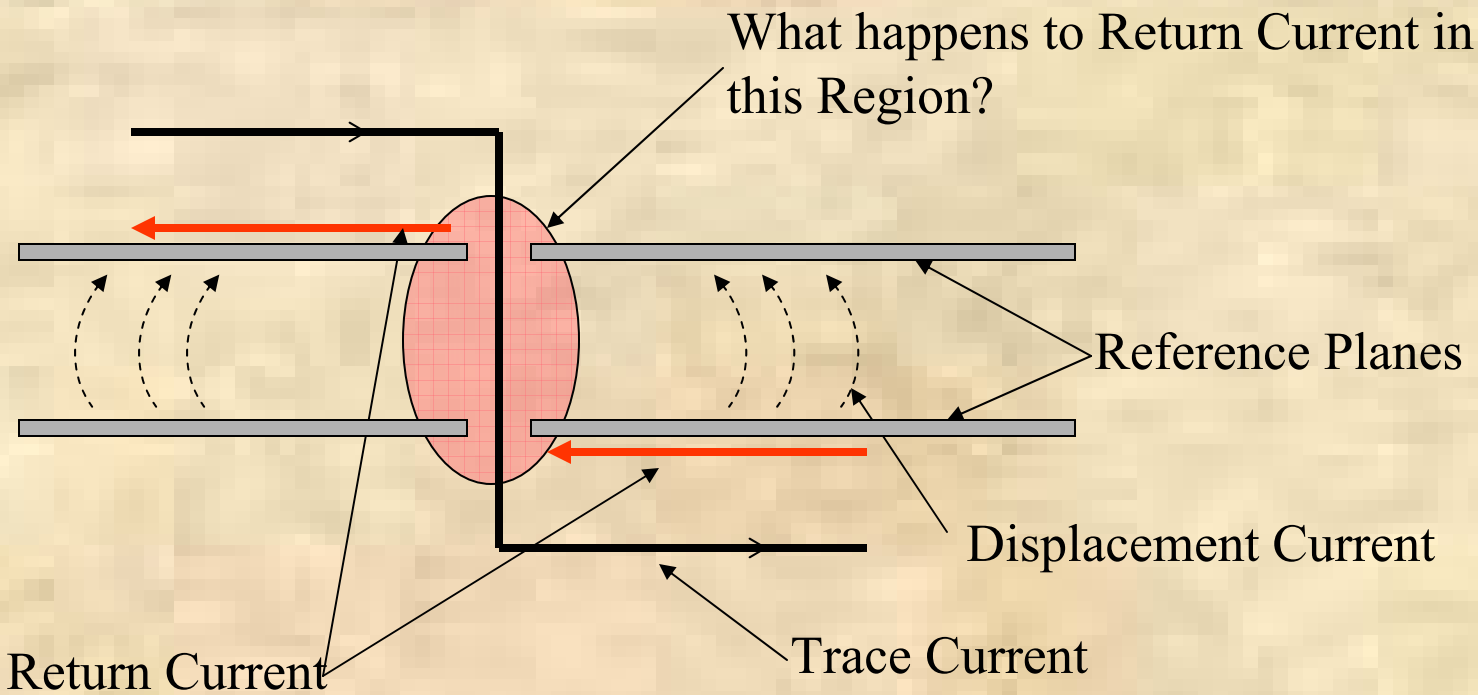
How can the Return Current Flow When Signal Line Goes Through Via??

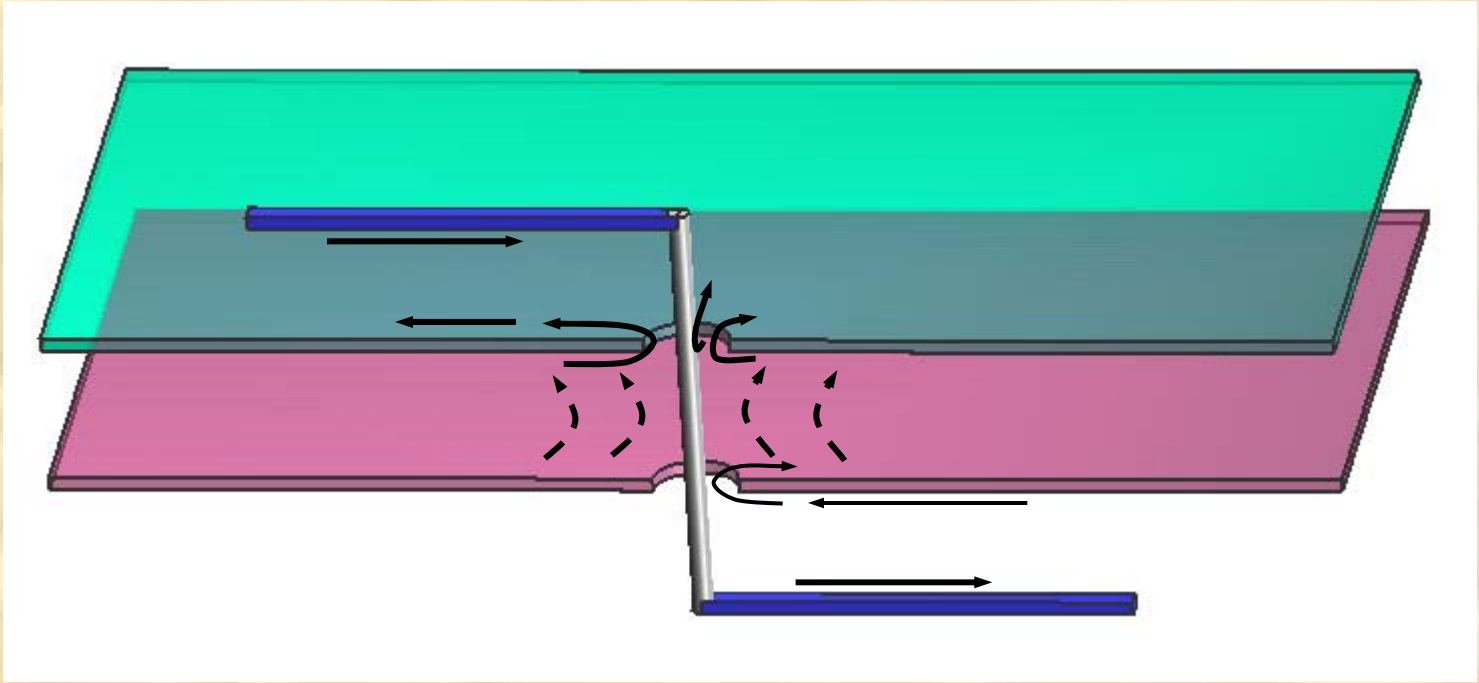


How can the Return Current Flow When Signal Line Goes Through Via??

- Current can NOT go from one side of the plane to the other through the plane
  - skin depth
- Current must go around plane at via hole, through decoupling capacitor, around second plane at the second via hole!
- Displacement current spread

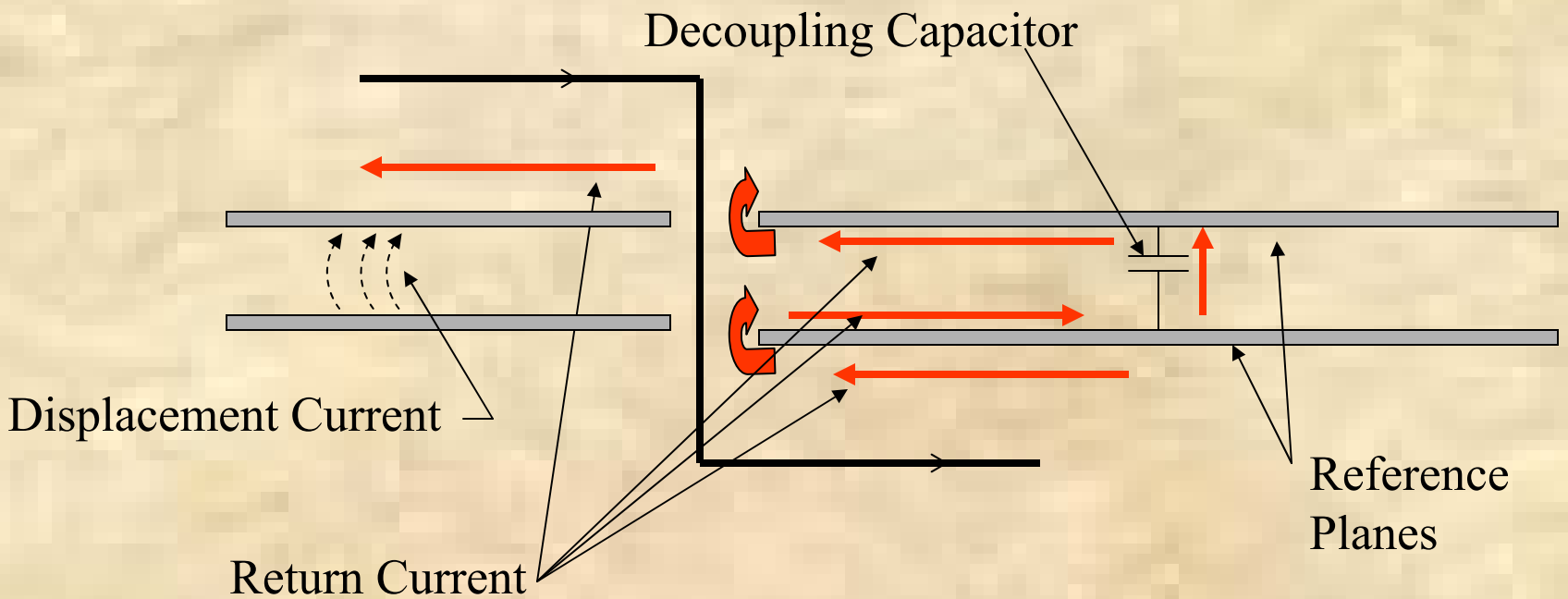
Return Current Across Reference Plane Change




GND
PWR

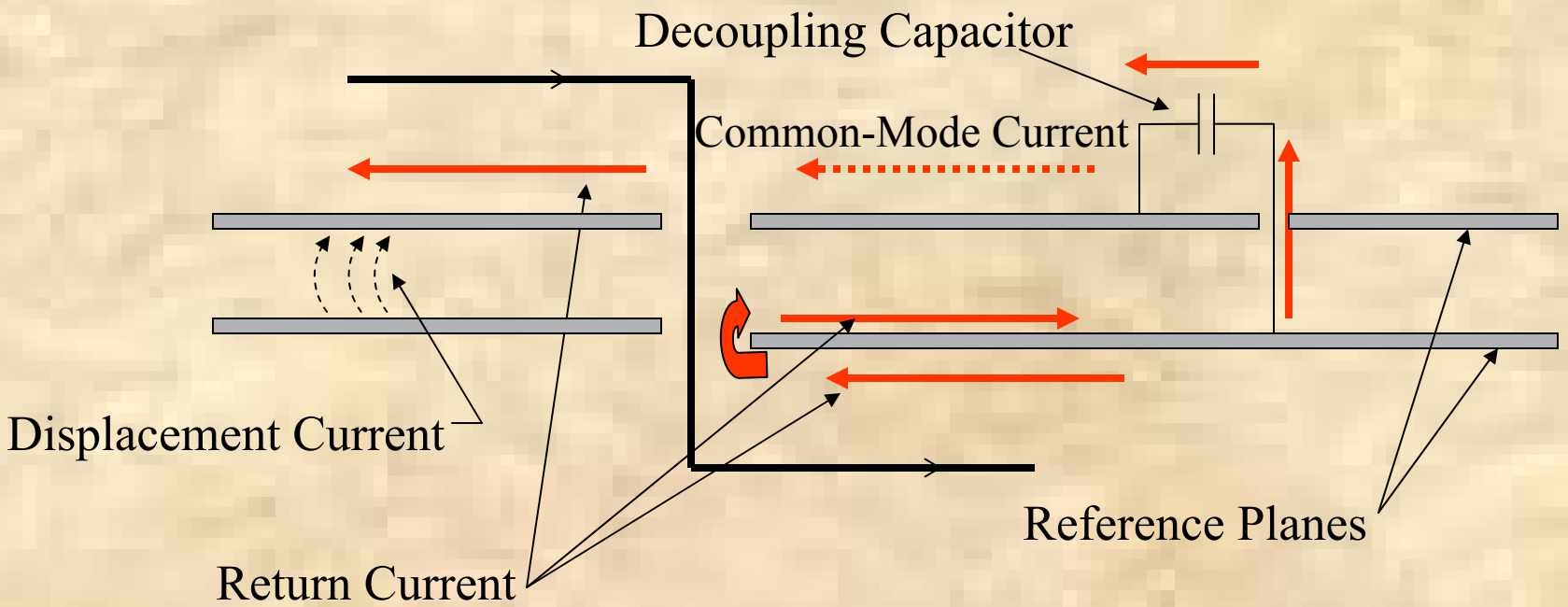
Return Current Across Reference Plane Change

With Decoupling Capacitor



Return Current Across Reference Plane Change

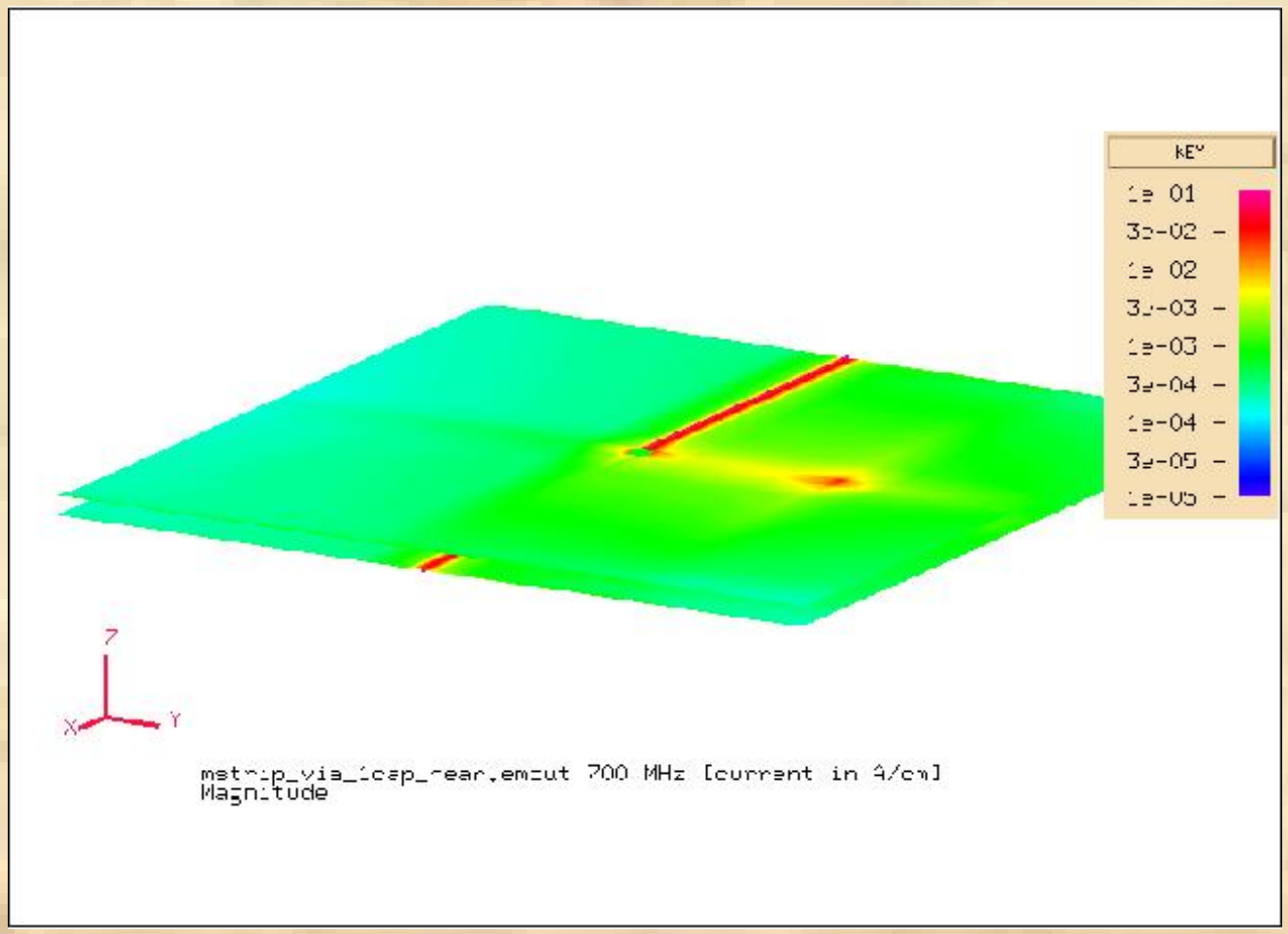
With Decoupling Capacitor (on Top)



Location of Decoupling Capacitors (Relative to Via) is Important!

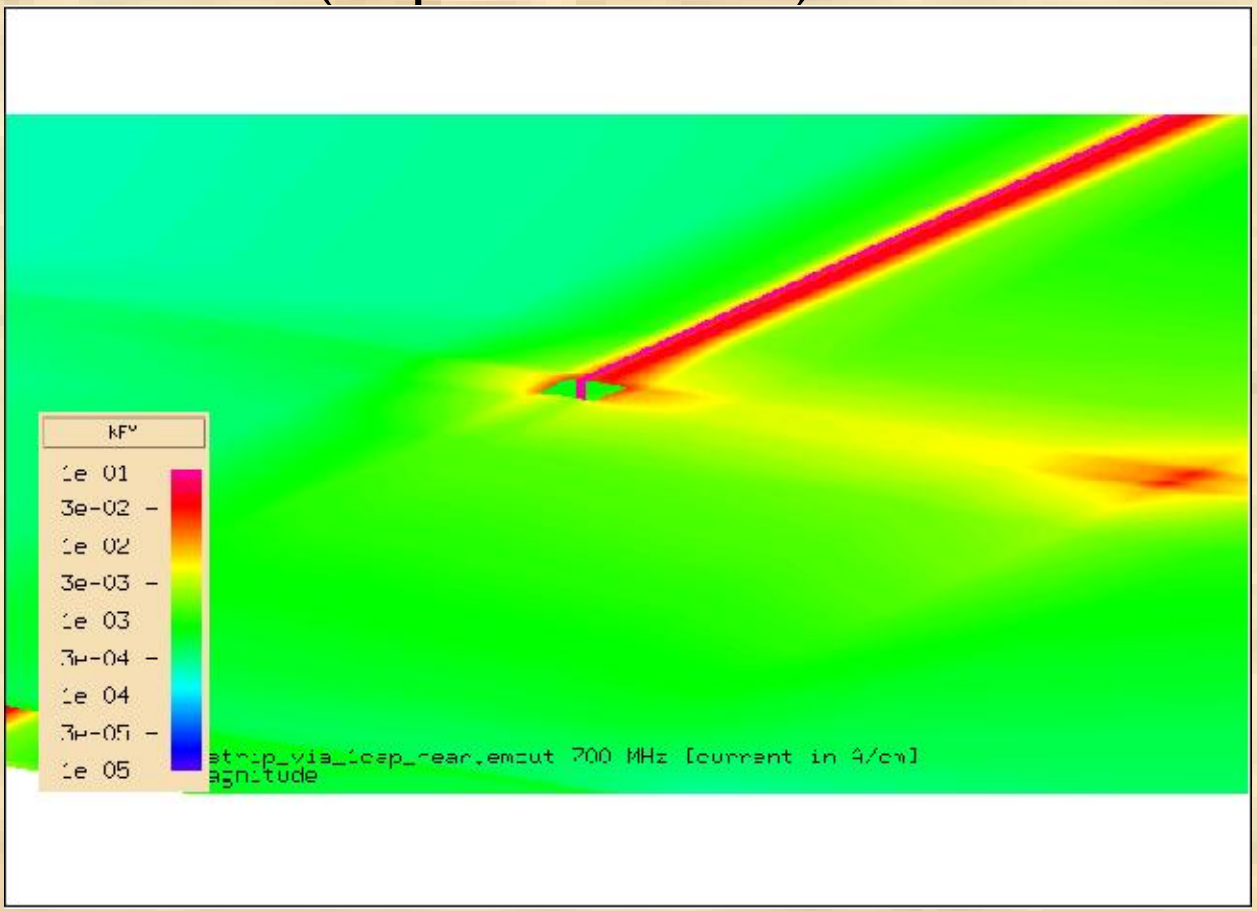
- One Decoupling Capacitor at 0.5”
- Two Decoupling Capacitors at 0.5”
- Two Decoupling Capacitors at 0.25”

RF Current @ 700 MHz with One Capacitor 0.5” from Via

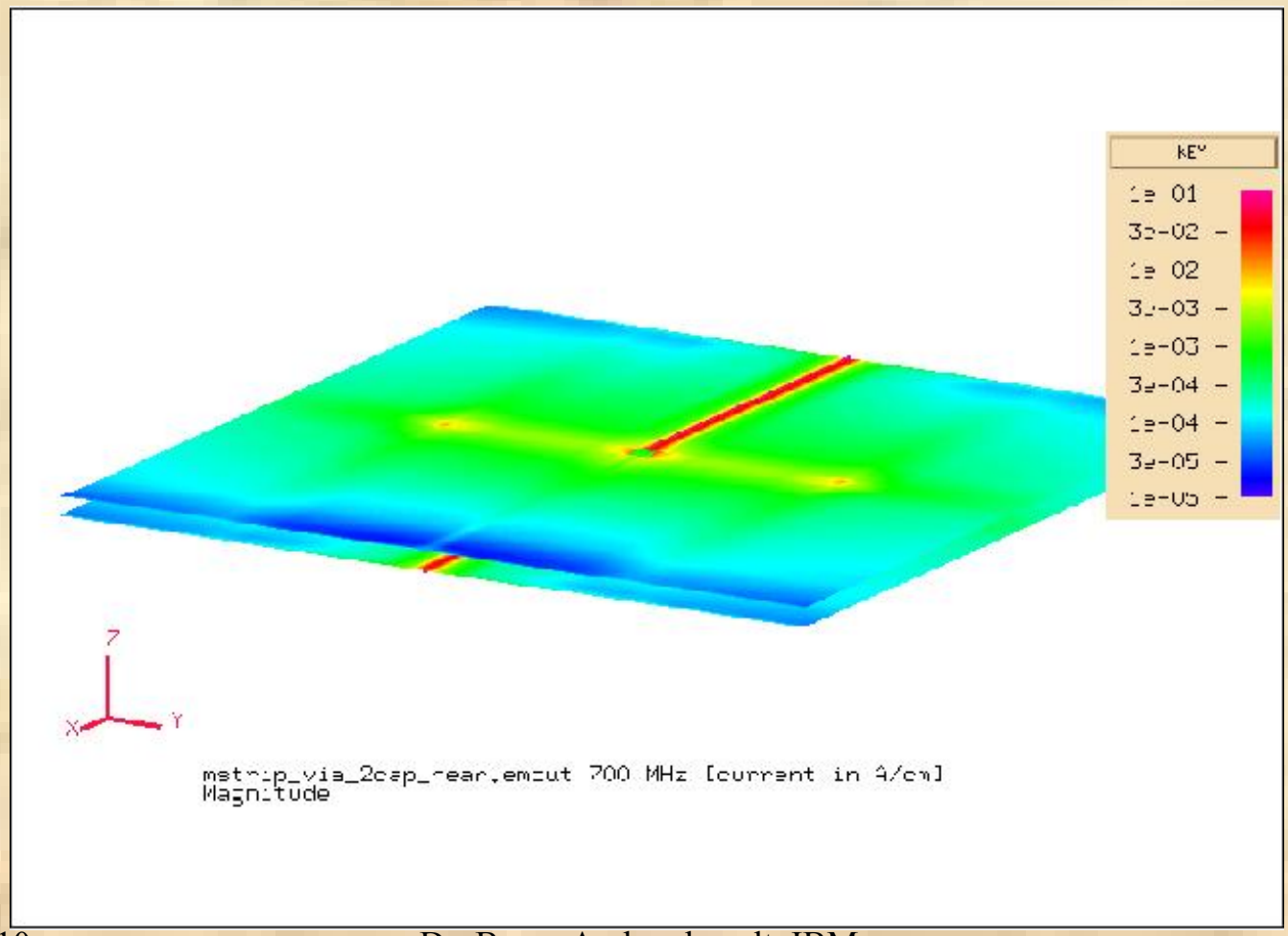


RF Current @ 700 MHz with One Capacitor 0.5” from Via

(expanded view)

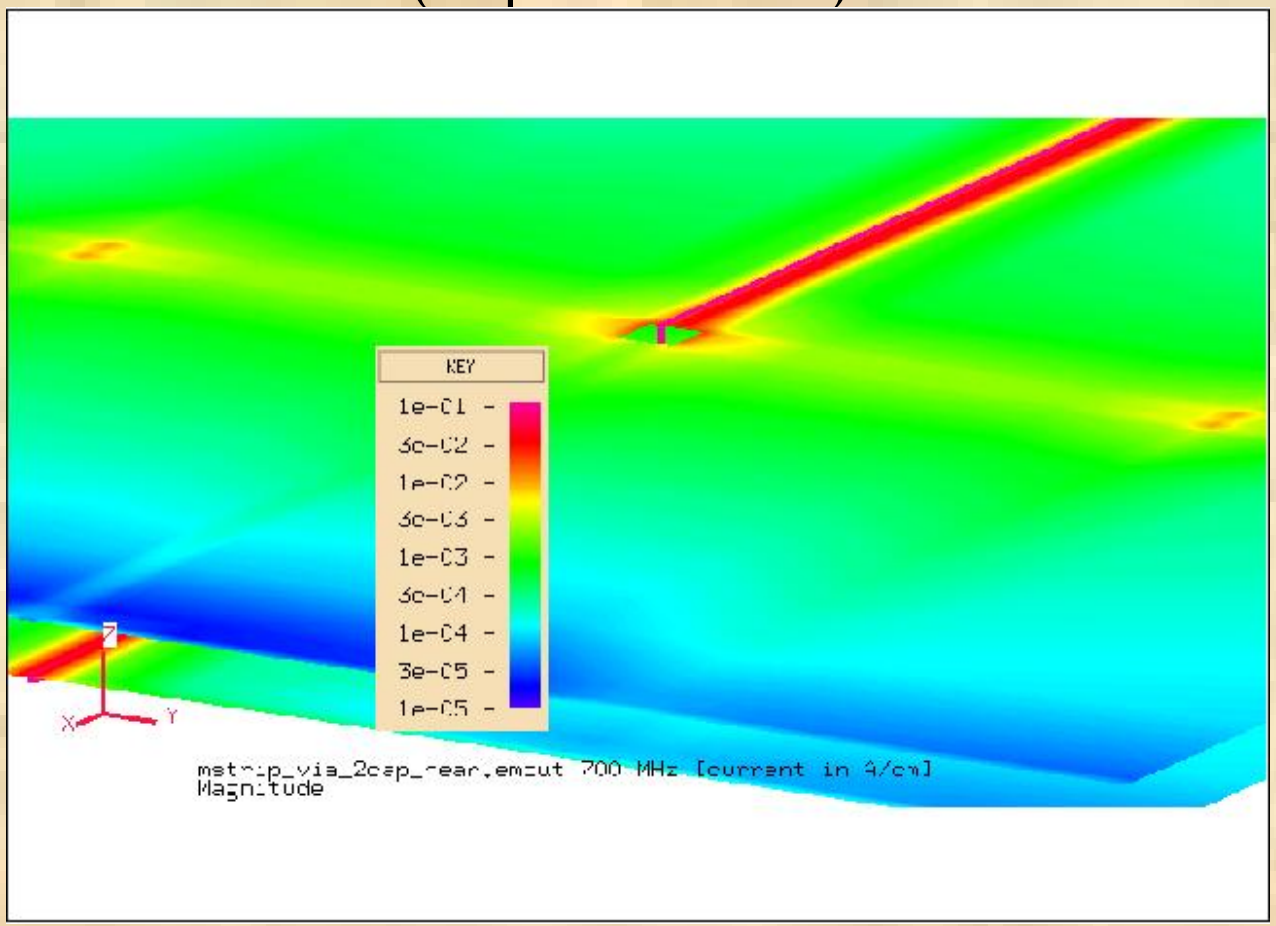


RF Current @ 700 MHz with Two Capacitors 0.5” from Via

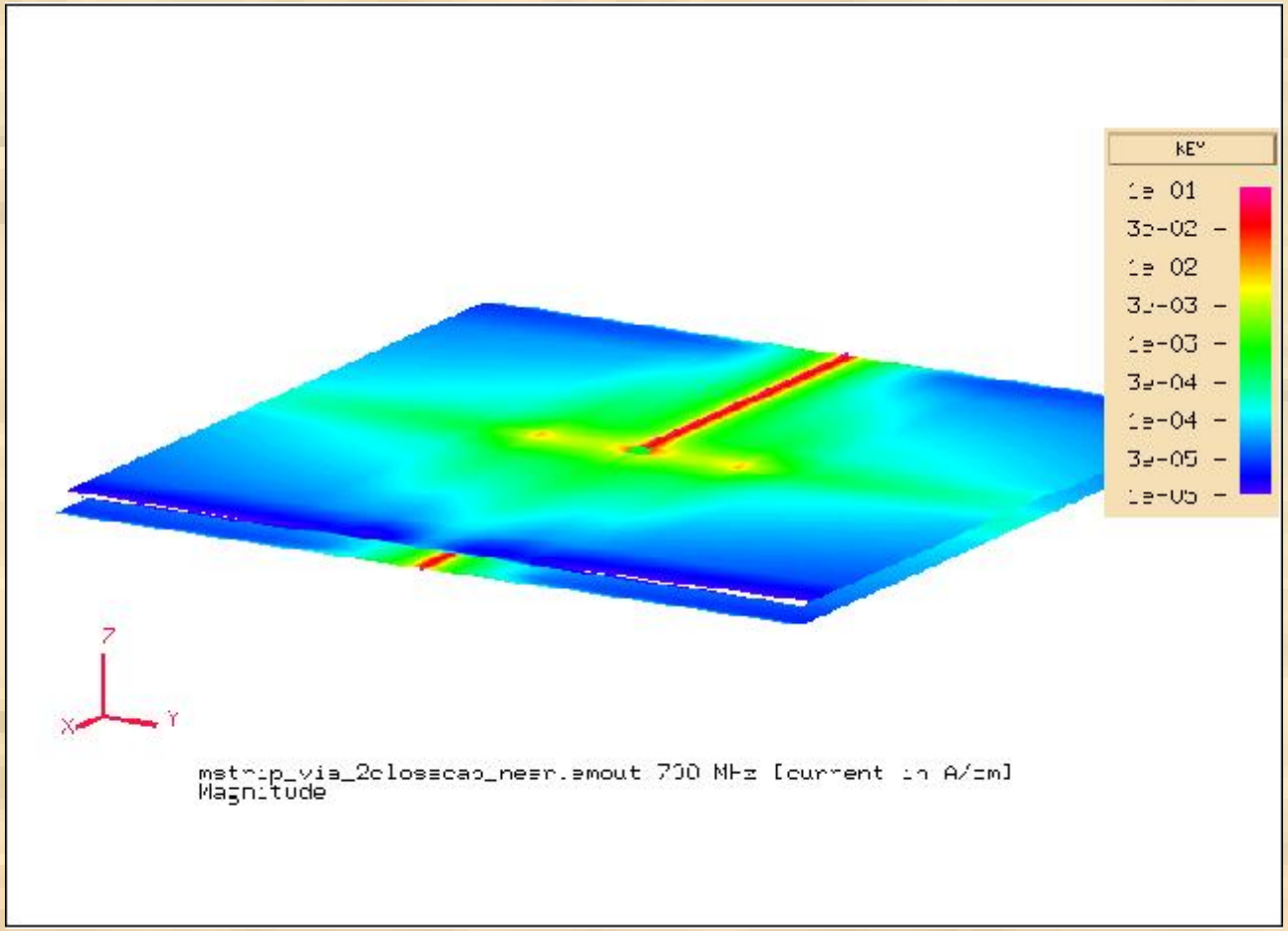


RF Current @ 700 MHz with One Capacitor 0.5” from Via

(Expanded view)

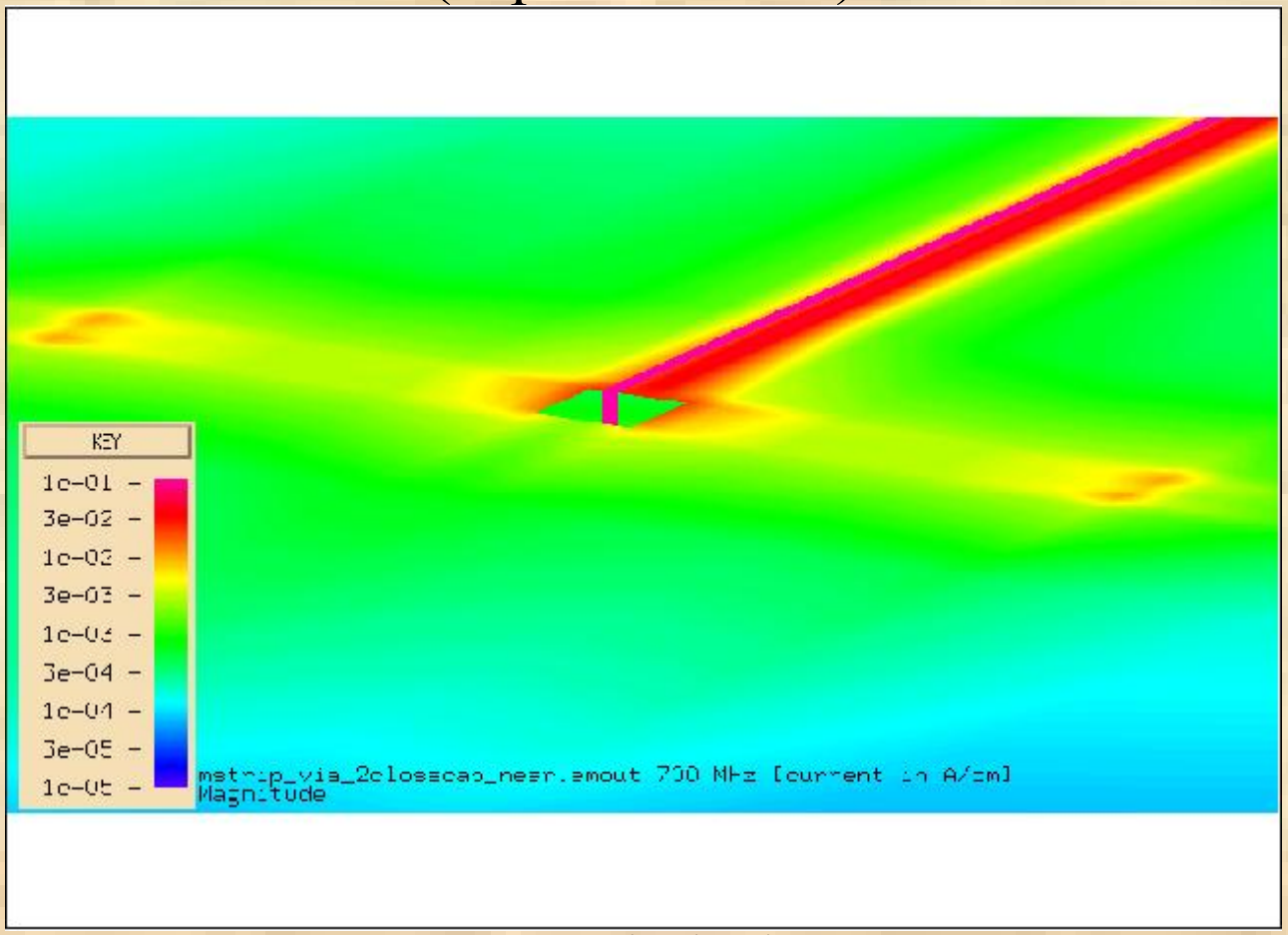


RF Current @ 700 MHz with Two Capacitors 0.25” from Via

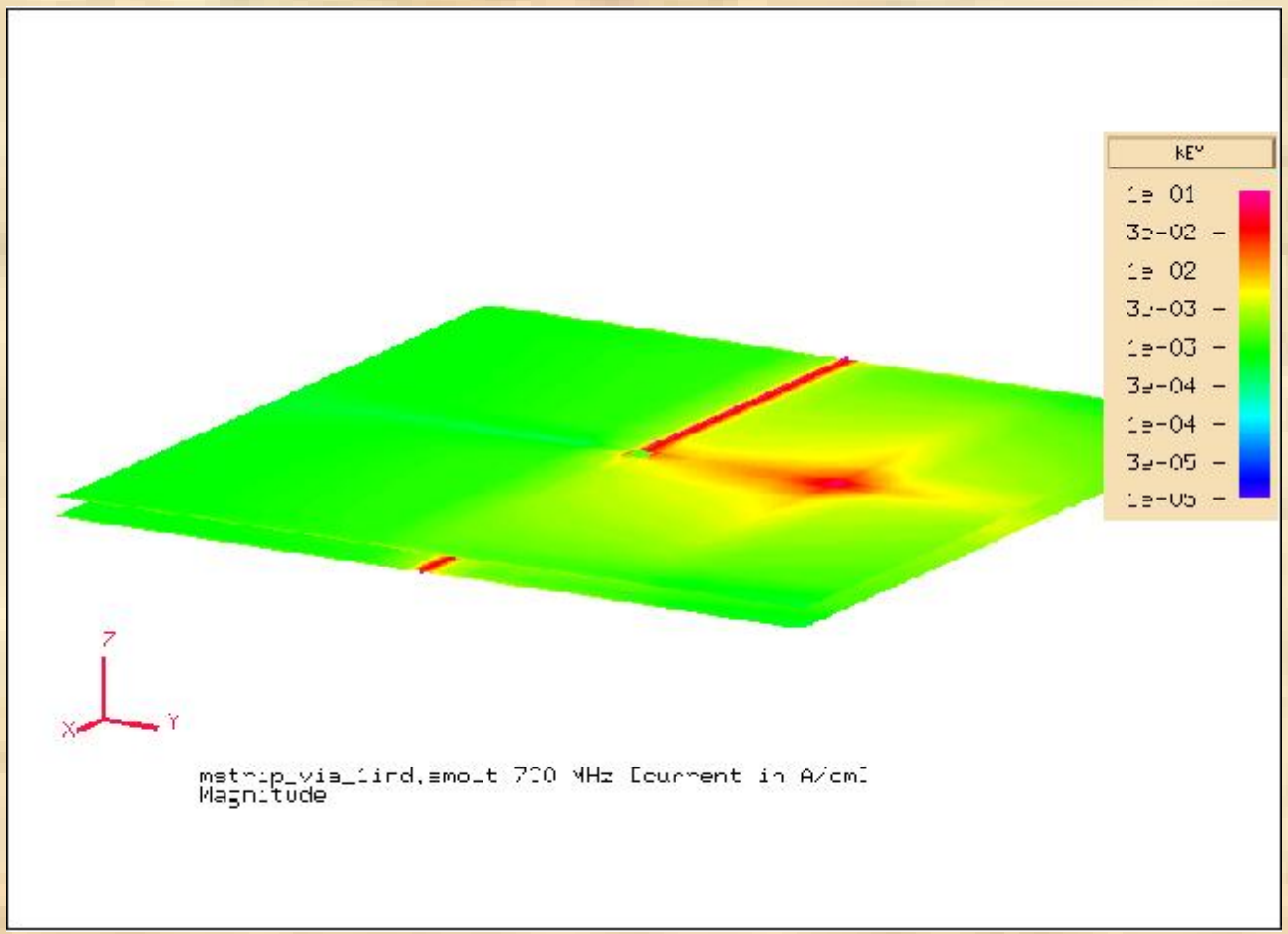


RF Current @ 700 MHz with Two Capacitors 0.25” from Via

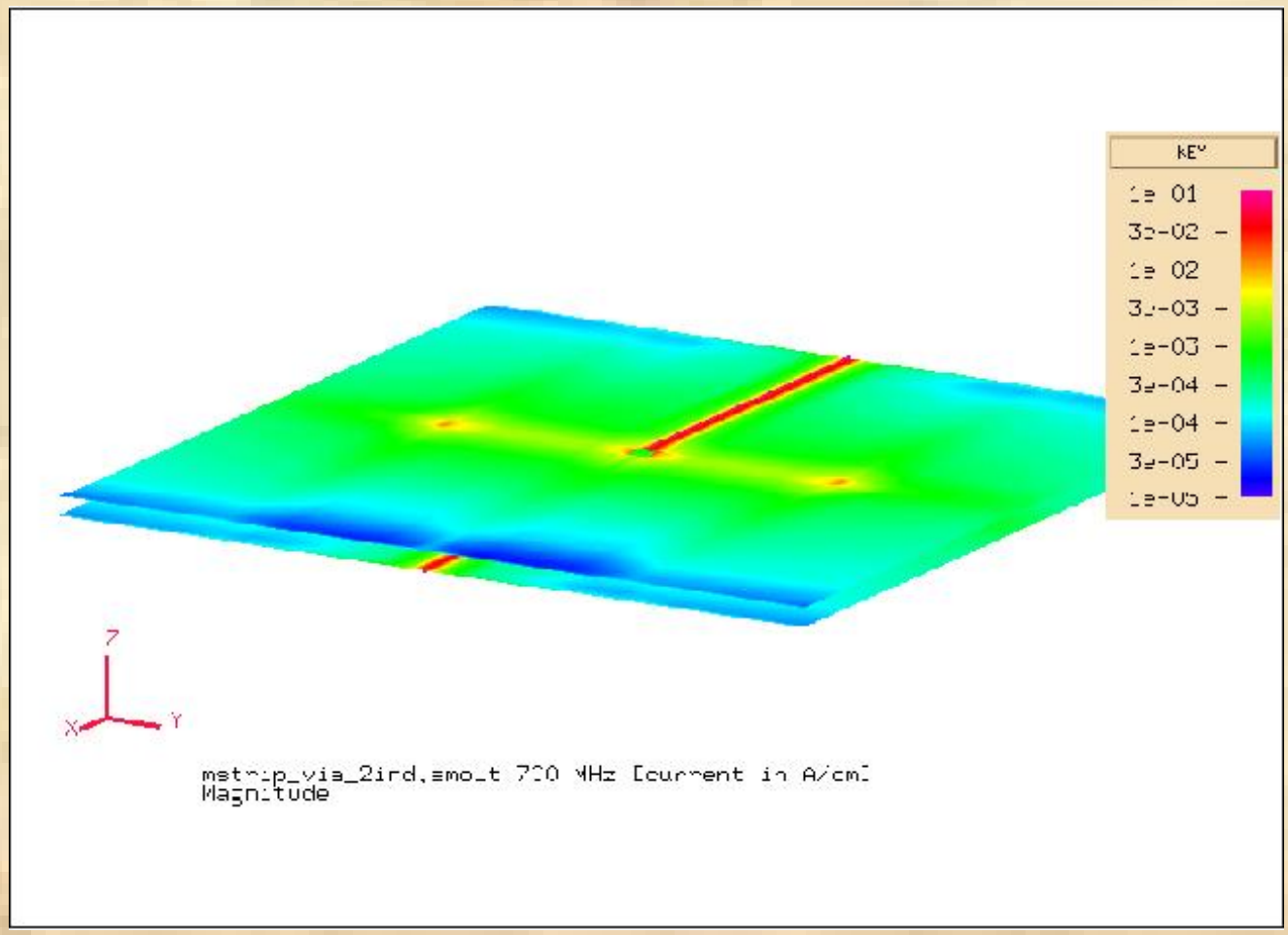
(expanded view)



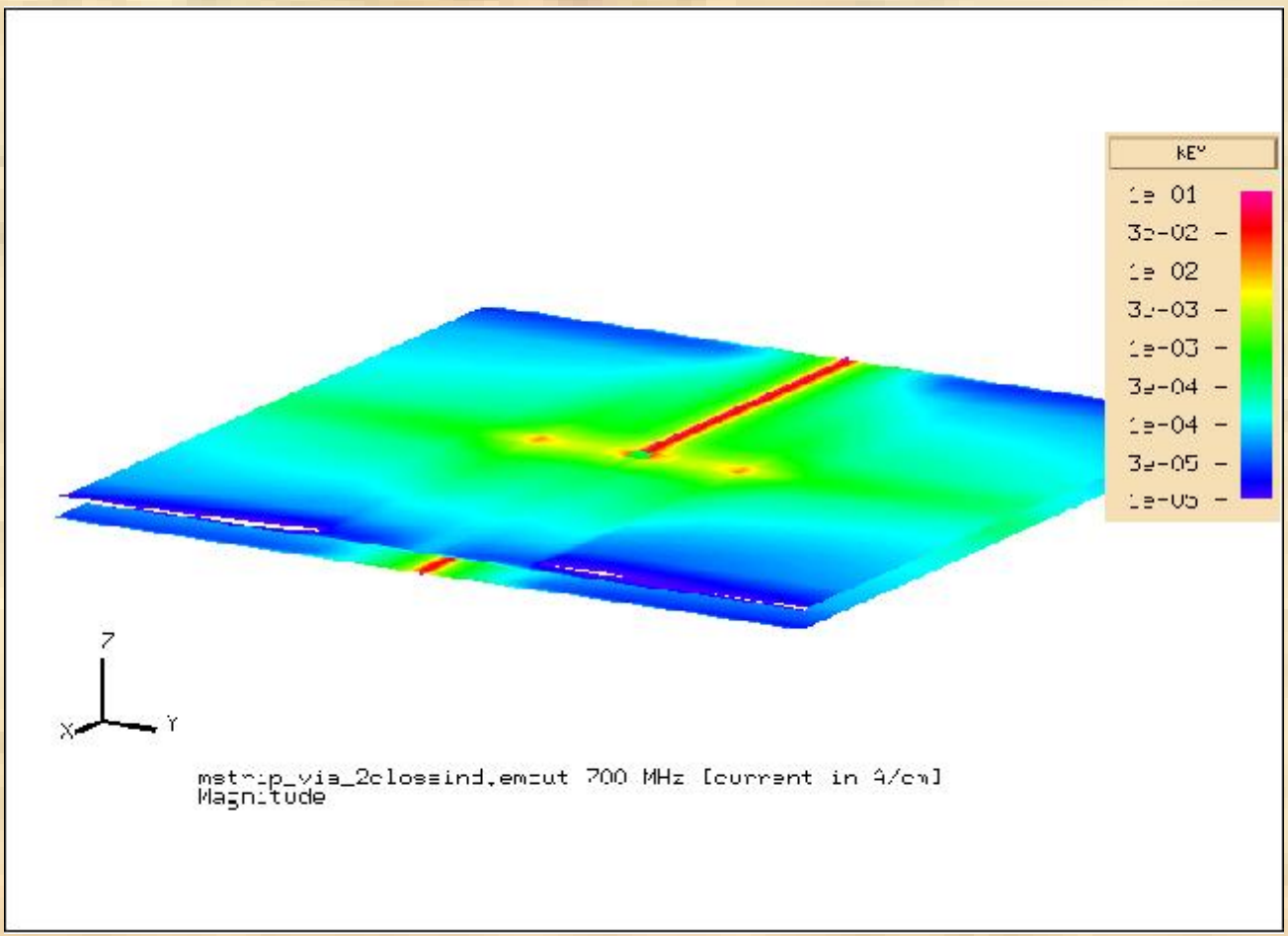
RF Current @ 700 MHz with One REAL Capacitor 0.5” from Via



RF Current @ 700 MHz with Two REAL Capacitors 0.5” from Via

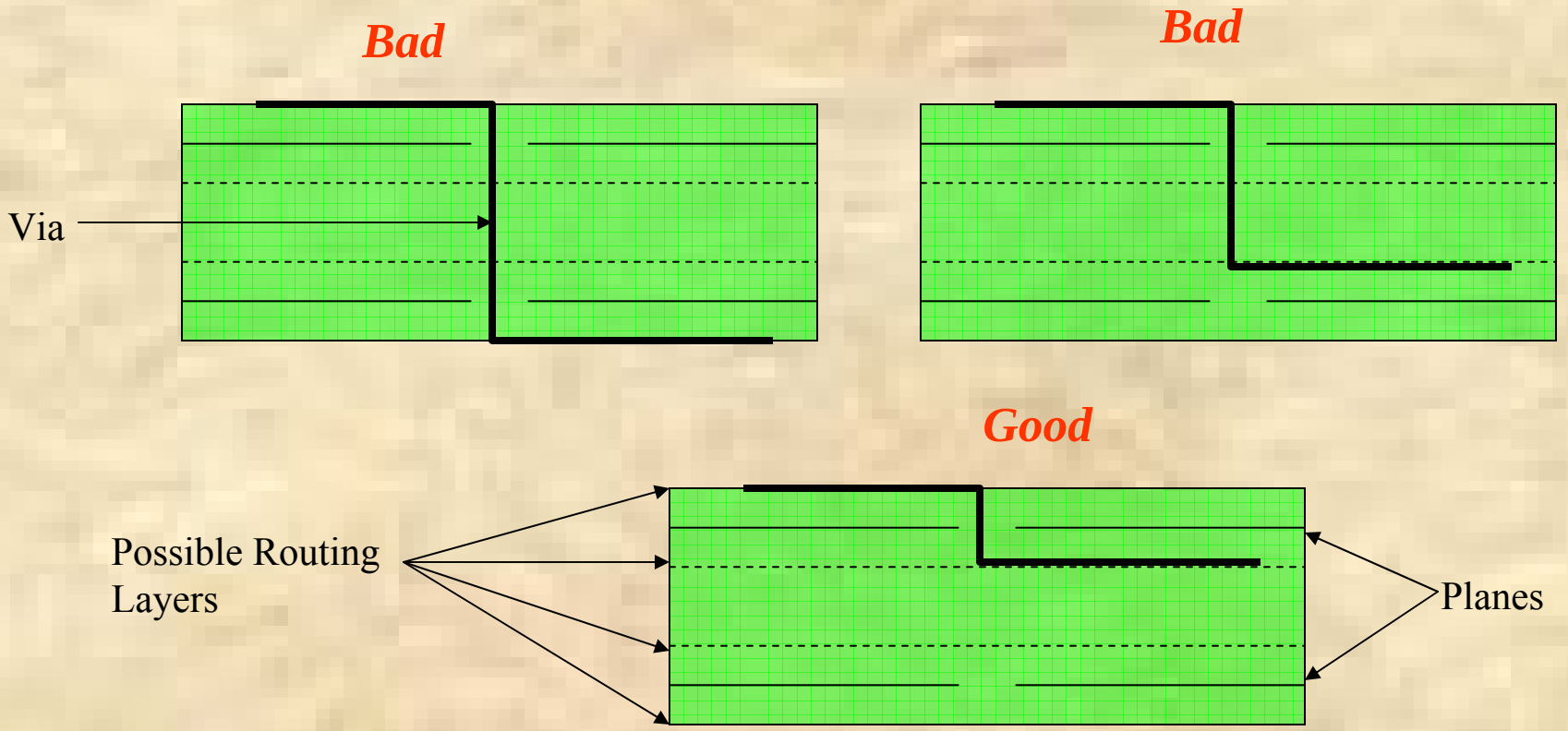


RF Current @ 700 MHz with Two REAL Capacitors 0.25” from Via

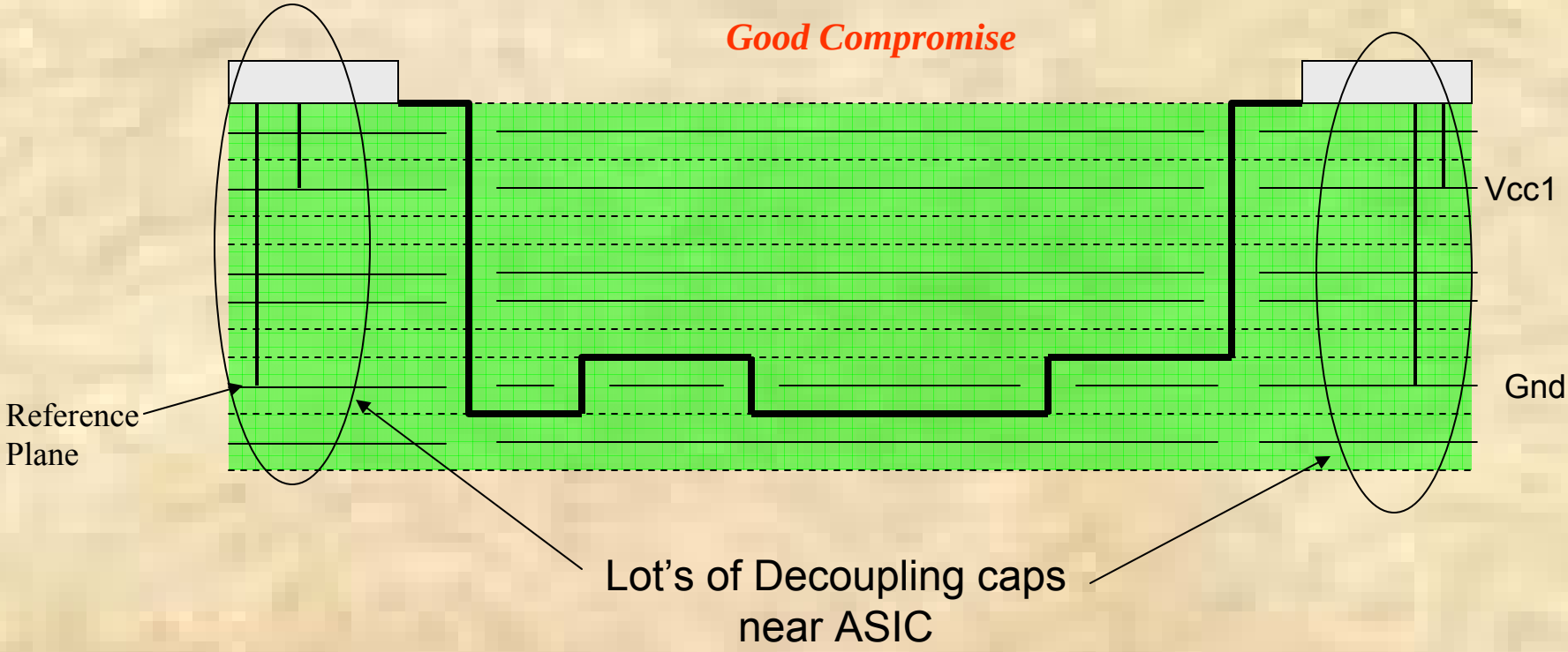


Critical Net Via Options

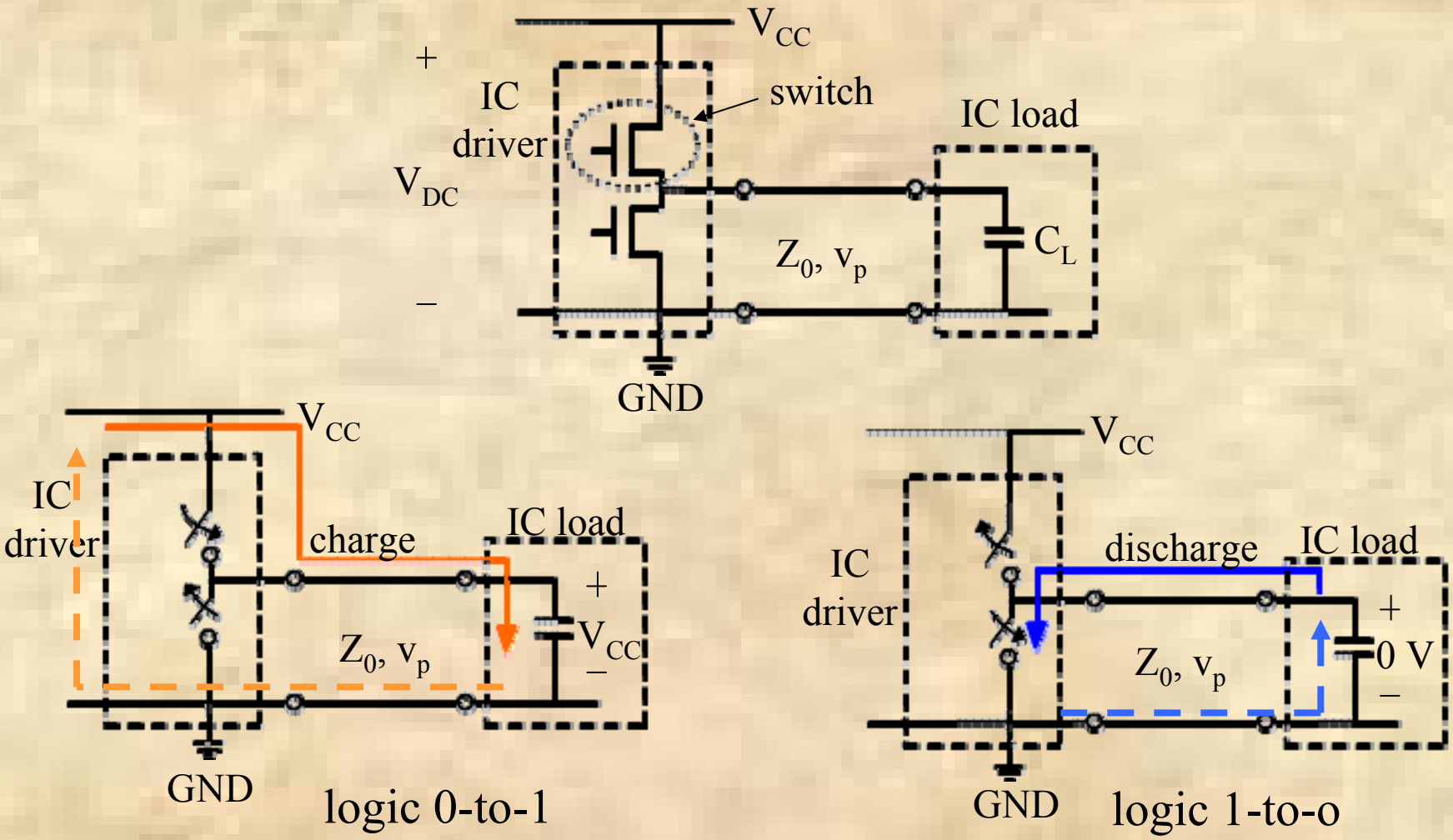
6-layer Board



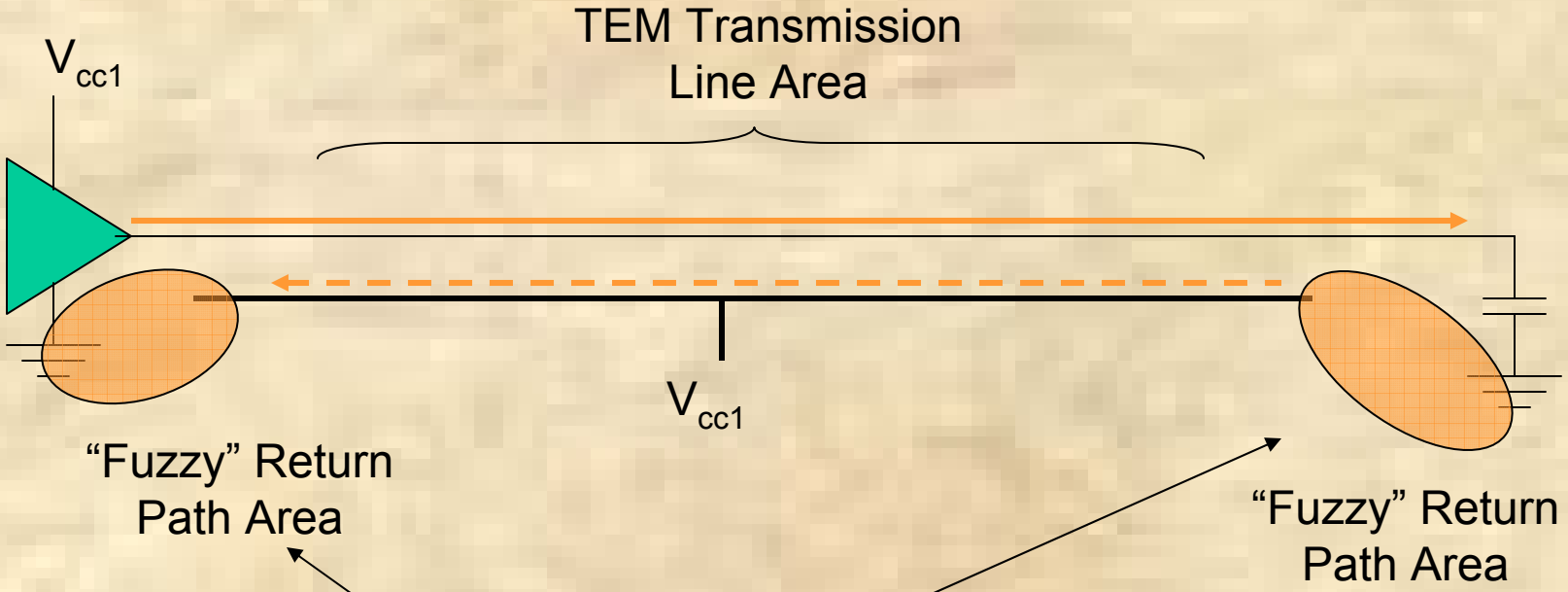
Compromise Routing Option for Many Layer Boards



Typical Driver/Receiver Currents



Suppose The Trace is Routed Next to Power (not Gnd)

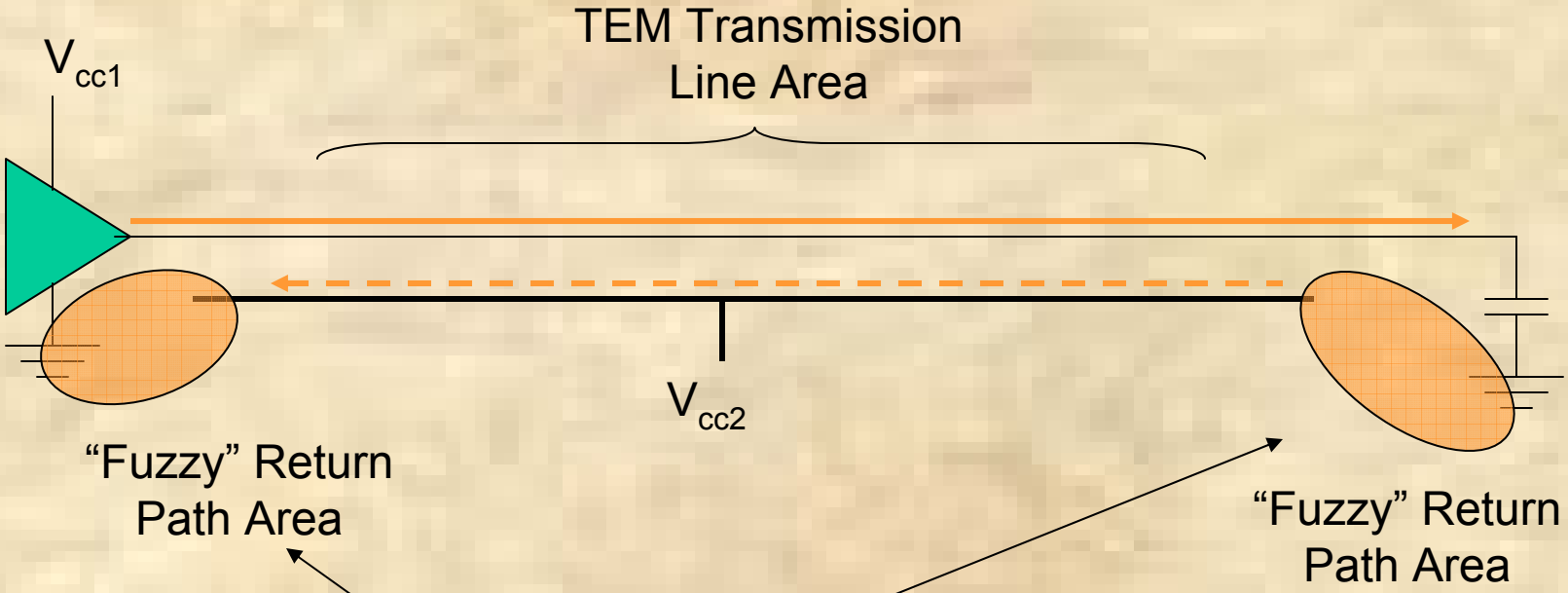


Return Path Options:

-- Decoupling Capacitors

-- Distributed Displacement Current

Suppose The Trace is Routed Next to a *DIFFERENT* Power (not Gnd)



Return Path Options:

-- Decoupling Capacitors ??? *May not be any nearby*!!

-- Distributed Displacement Current – *Increased current spread*!!!

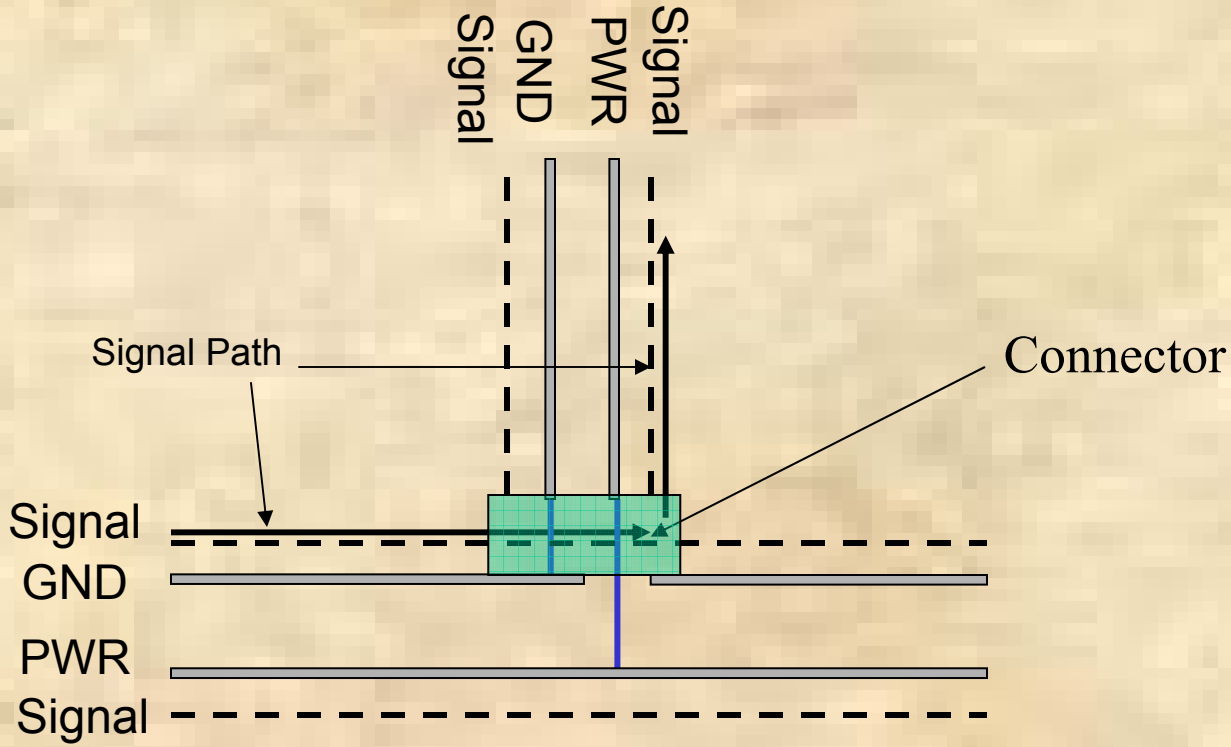
Via Summary

- ✓ Route critical signals on either side of ONE reference plane
- ✓ Drop critical signal net to selected layer close to driver/receiver
  - ✓ Many decoupling capacitors (or GND vias) to help return currents
- ✓ Do NOT change reference planes on critical nets unless ABSOLUTELY NECESSARY!!
- ✓ Make sure at least 2 decoupling capacitors within 0.25” of via (change reference planes) with critical signals

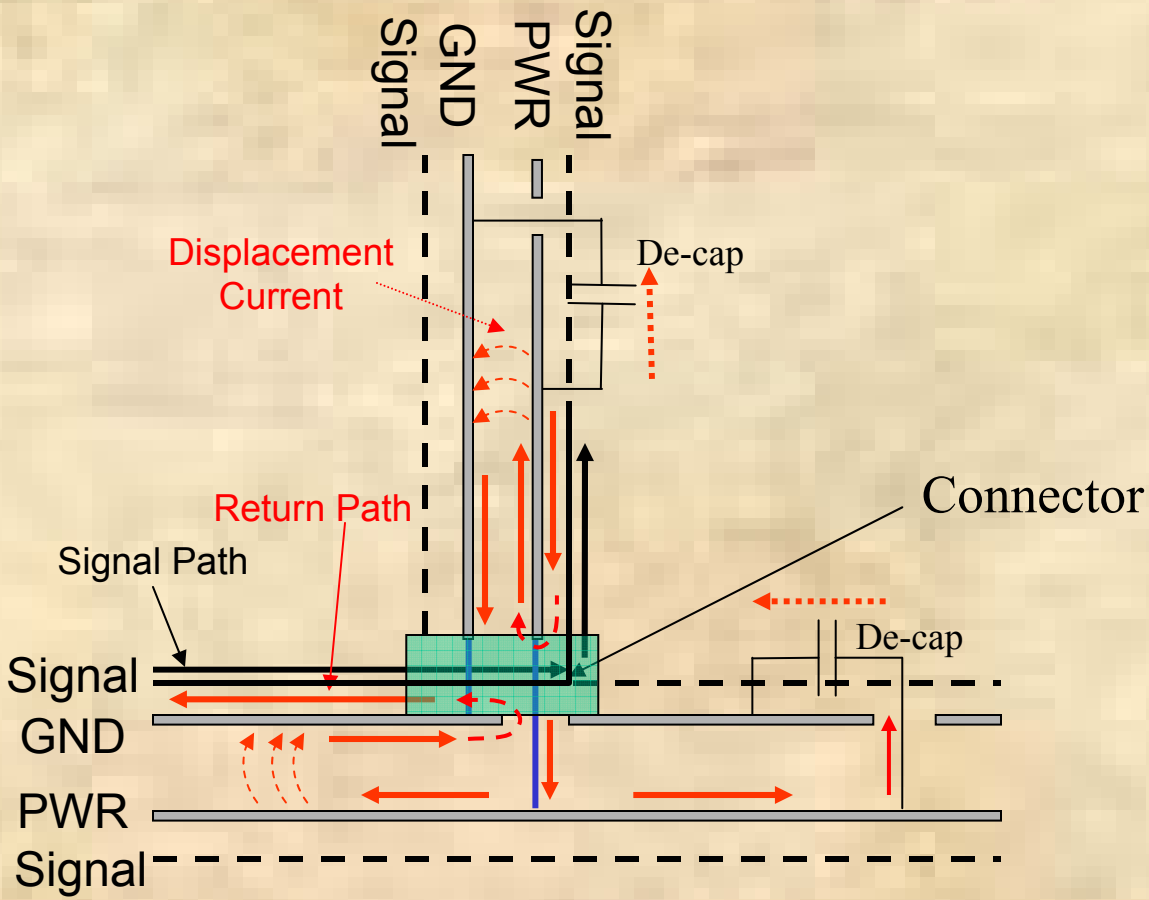
Mother/Daughter Board Connector Crossing

- Critical Signals must be referenced to same plane on both sides of the connector

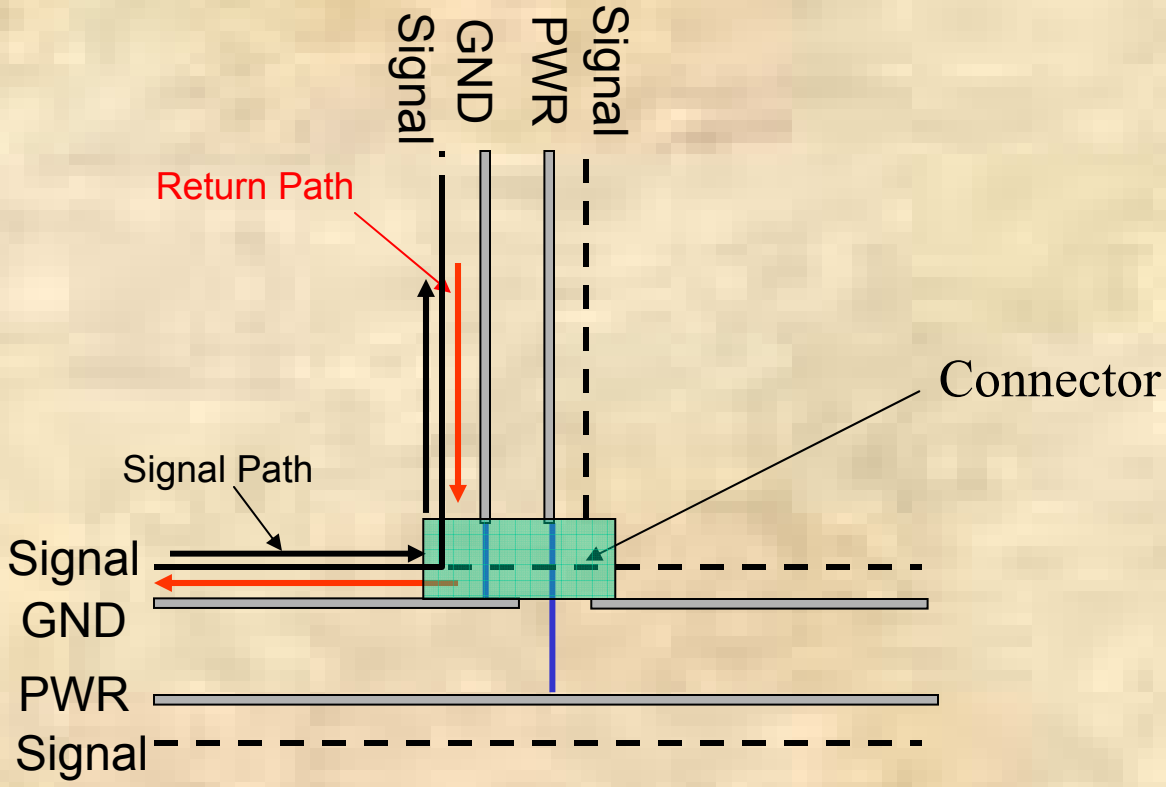
Mother/Daughter Board Connector Crossing



Return Current from Improper Referencing Across Connector



Return Current from Proper Referencing Across Connector



How Many "Ground" Pins Across Connector ???

- Nothing ***MAGICAL*** about "ground"
- Return current flow!
- Choose the number of power and "ground" pins based on the number of signal lines referenced to power or "ground" planes
- Insure signals are referenced against same planes on either side of connector

Think about Return Currents!!

- ✓Reference plane should be continuous under all critical traces
- ✓When Vias are necessary make sure there are two close decoupling capacitors
- ✓When crossing a connector to a second board, make sure the critical trace is referenced to the same reference plane as the primary board

To Prevent/Reduce Loop Mode Emissions

- ✓ Bury traces between planes whenever possible
  - ✓ No direct emissions from traces with no exposed length
- ✓ Keep Exposed lengths short
  - ✓ Shorter exposed traces radiate less
- ✓ Improve termination to reduce high frequency content
  - ✓ **If the high frequency currents are not created, they can not radiate!**

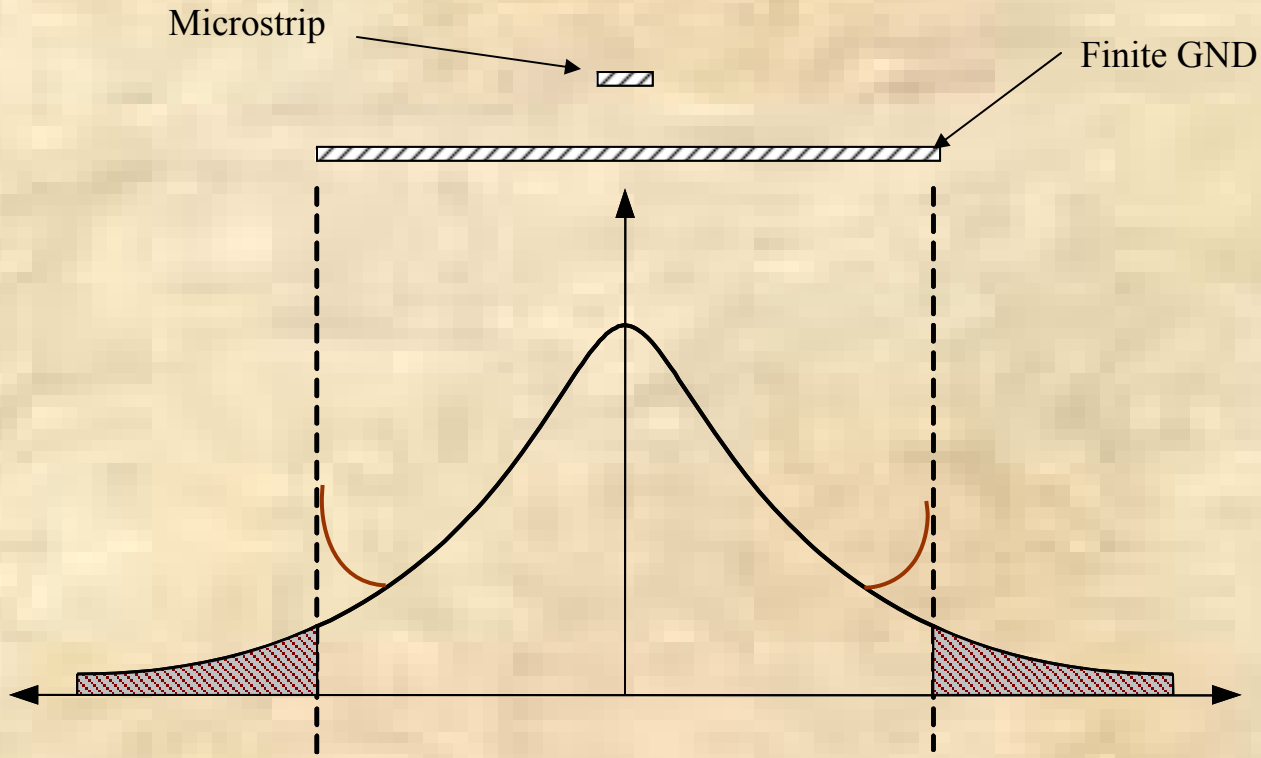
Potential Problems

- Intentional Signals
  - Loop Mode
  - Common Mode
- Unintentional Signals
  - Common Mode
  - Crosstalk Coupling
  - Power Plane Bounce
  - Above Board Structures

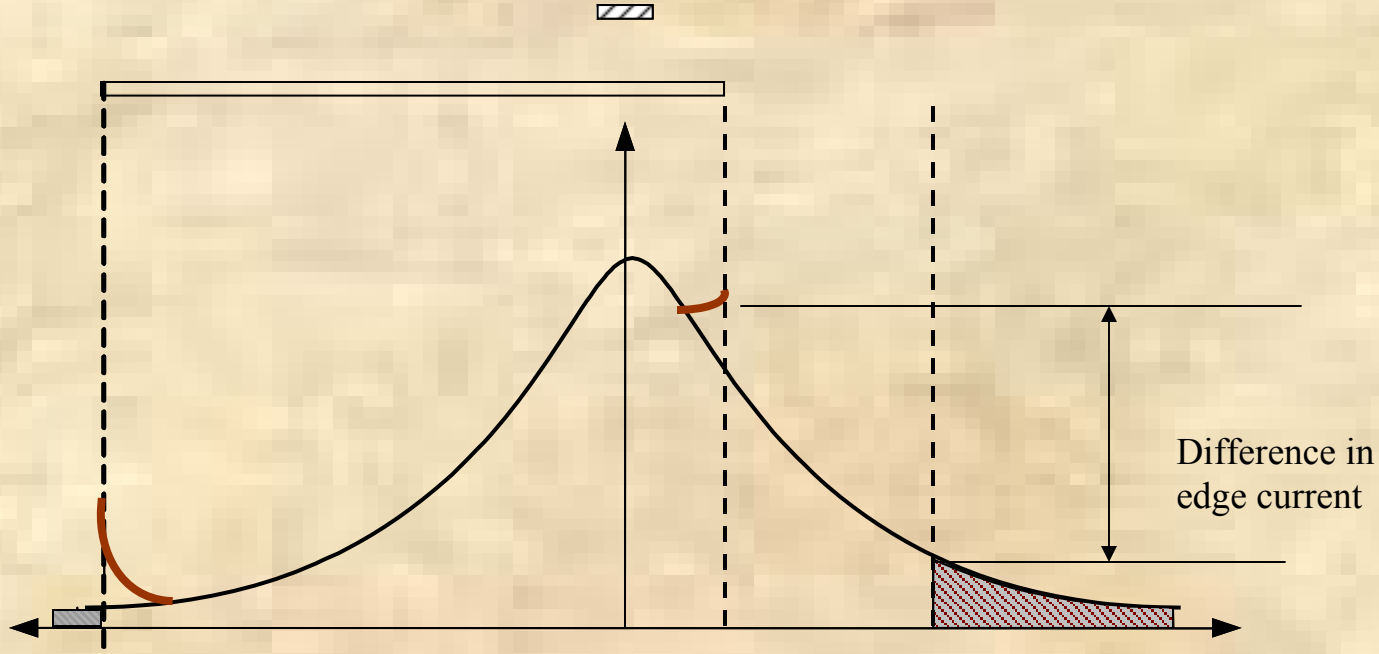
Intentional Signals -- Common Mode Emissions

- Return Currents do NOT flow only under microstrip
- Return current spreads out over entire plane to find path of least inductance
- When traces are near board edge, the return current is high along the edge

Current Spread in Ground-Reference Plane from Microstrip



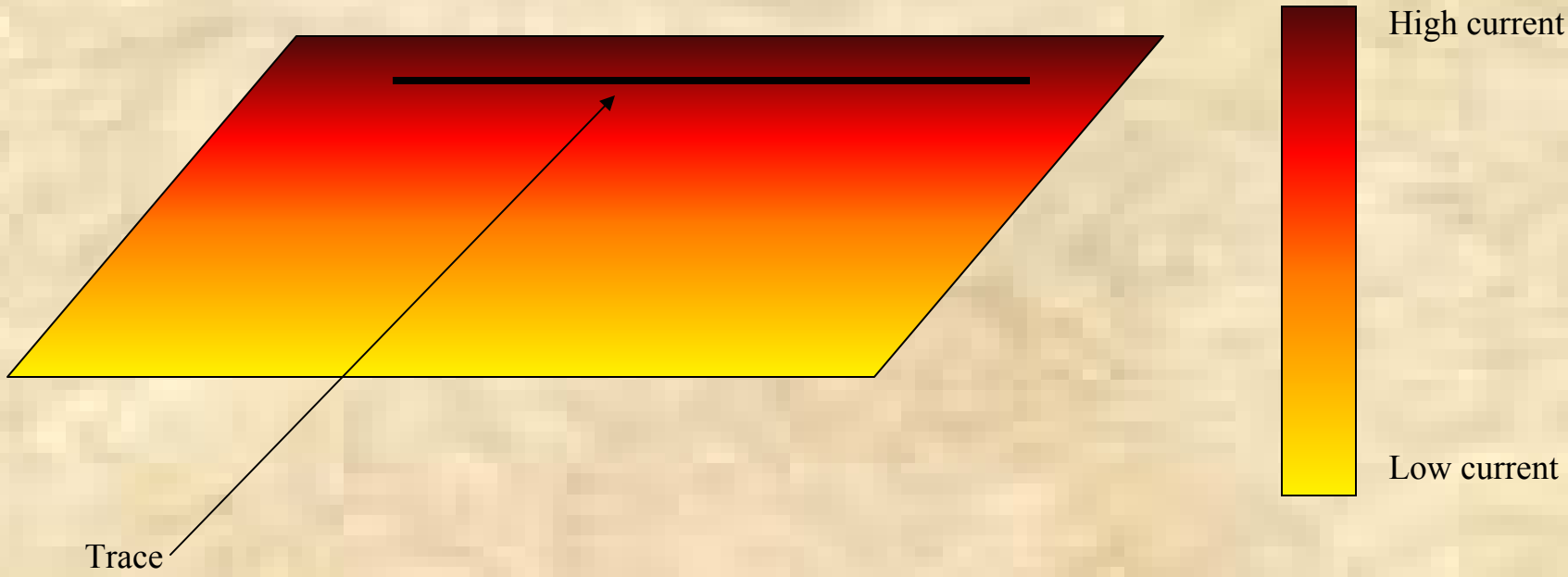
Current Spread in Ground-Reference Plane from Microstrip



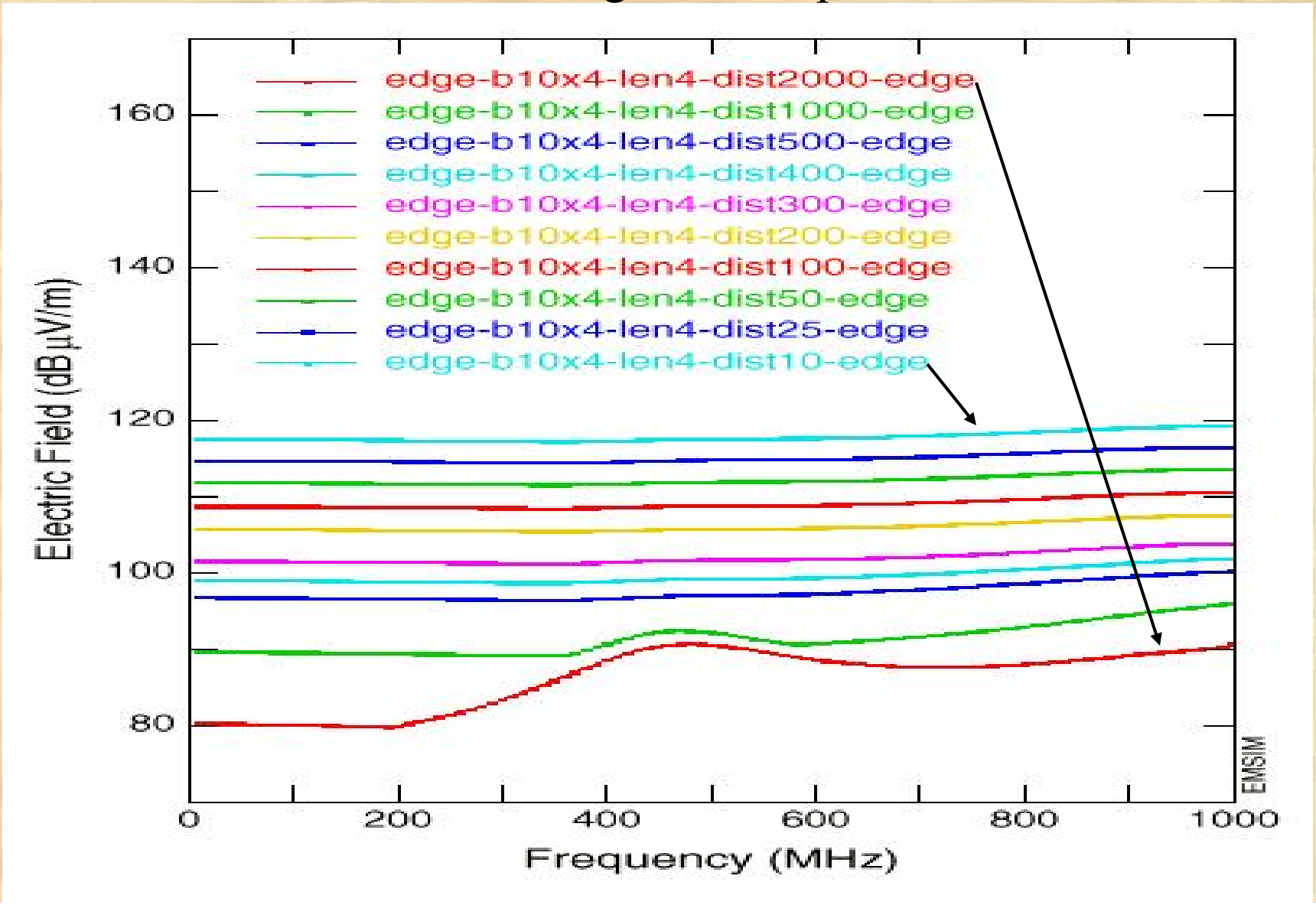
Where's the Radiation?

- Due to Current Build up Along the edge
  - Along Edge of board
  - Often near to enclosure seams, slots, airvents

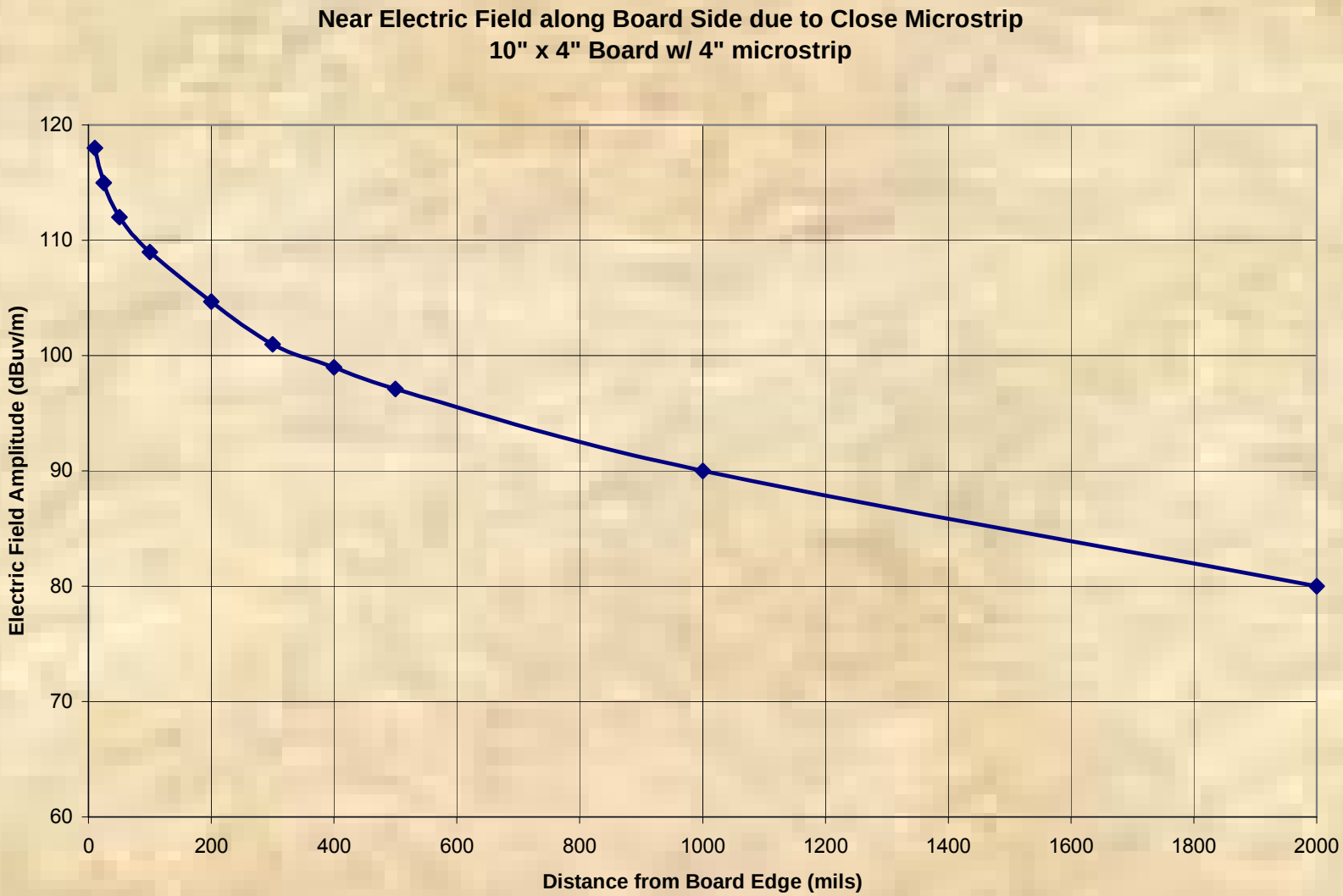
Return Current in Reference Plane with Trace Near Edge



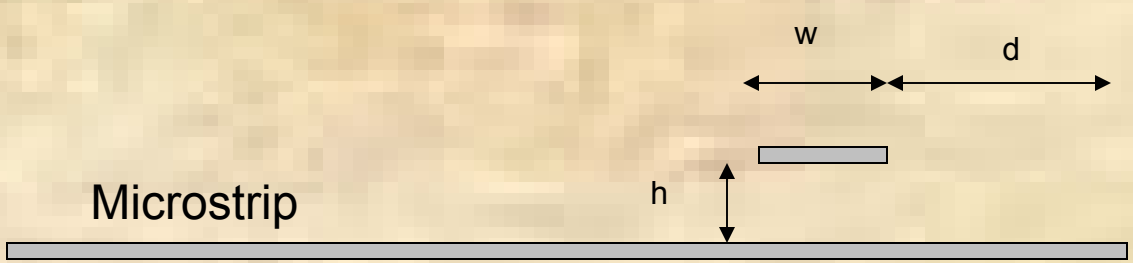
E-field along edge vs. distance from edge for 10”x4” board 4” long microstrip



Example Field vs. Distance



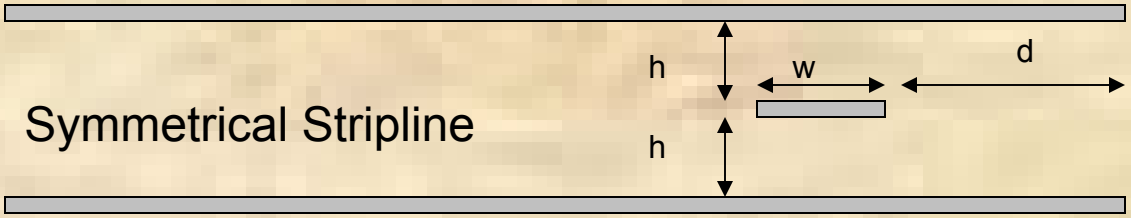
Current Along Edge of Reference Plane



$$I_{Edge} = \frac{I_{Signal}}{\pi}\left(\frac{\pi}{2} - \arctan\left(\frac{w_g - 2\left[\left(w_g / 2\right) - d\right]}{2h}\right)\right)$$

I_{signal} = the current amplitude (in linear scale) for each harmonic of the current waveform.
w_g = the width of the ground-refer4ence plane (set to 1000 always)
d = the distance from the trace to the edge of the ground-reference plane
h = the height between the trace and the ground-reference plane

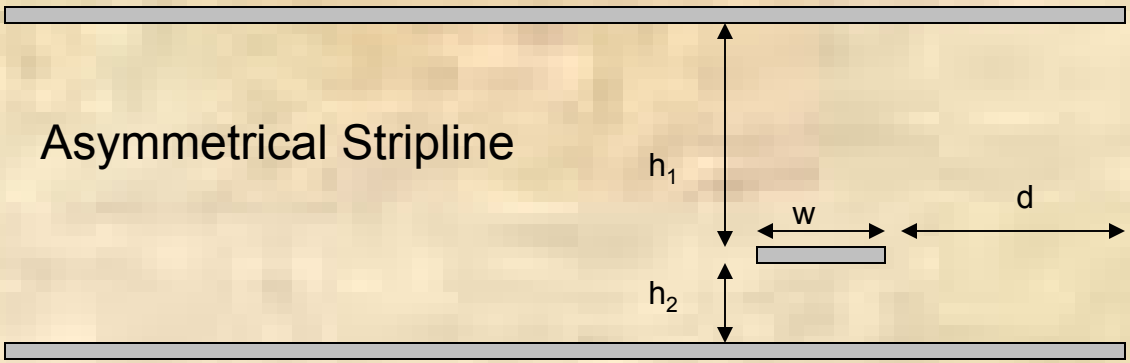
Current Along Edge of Reference Plane



$$I_{Edge} = \frac{I_{Signal}}{2\pi}\left(\frac{\pi}{2} - \arctan\left(\frac{w_g - 2\left[\left(w_g/2\right) - d\right]}{2h}\right)\right)$$

I_{signal} = the current amplitude (in linear scale) for each harmonic of the current waveform.
w_g = the width of the ground-refer4ence plane (set to 1000 always)
d = the distance from the trace to the edge of the ground-reference plane
h = the height between the trace and the ground-reference plane

Current Along Edge of Reference Plane



$$I_{Edge-Nearest} = \frac{I_{Signal}}{\pi}\left(\frac{h_2}{h_1}\right)\left(\frac{\pi}{2} - \arctan\left(\frac{w_g - 2\left[\left(w_g/2\right) - d\right]}{2h_2}\right)\right)$$

$$I_{Edge-Furthest} = \frac{I_{Signal}}{\pi}\left(\frac{h_1}{h_2}\right)\left(\frac{\pi}{2} - \arctan\left(\frac{w_g - 2\left[\left(w_g/2\right) - d\right]}{2h_1}\right)\right)$$

I_{signal} = the current amplitude (in linear scale) for each harmonic of the current waveform.
w_g = the width of the ground-refer4ence plane (set to 1000 always)
d = the distance from the trace to the edge of the ground-reference plane
h_1 *and* h_2 = the height between the trace and the ground-reference plane

To Prevent/Reduce Intentional Signal -- Common Mode Emissions

- ✓Keep traces away from board edge
  - Reduces Return current along edge of reference plane
- ✓Improve termination to reduce high frequency content
  - If the high frequency currents are not created, they can not radiate!

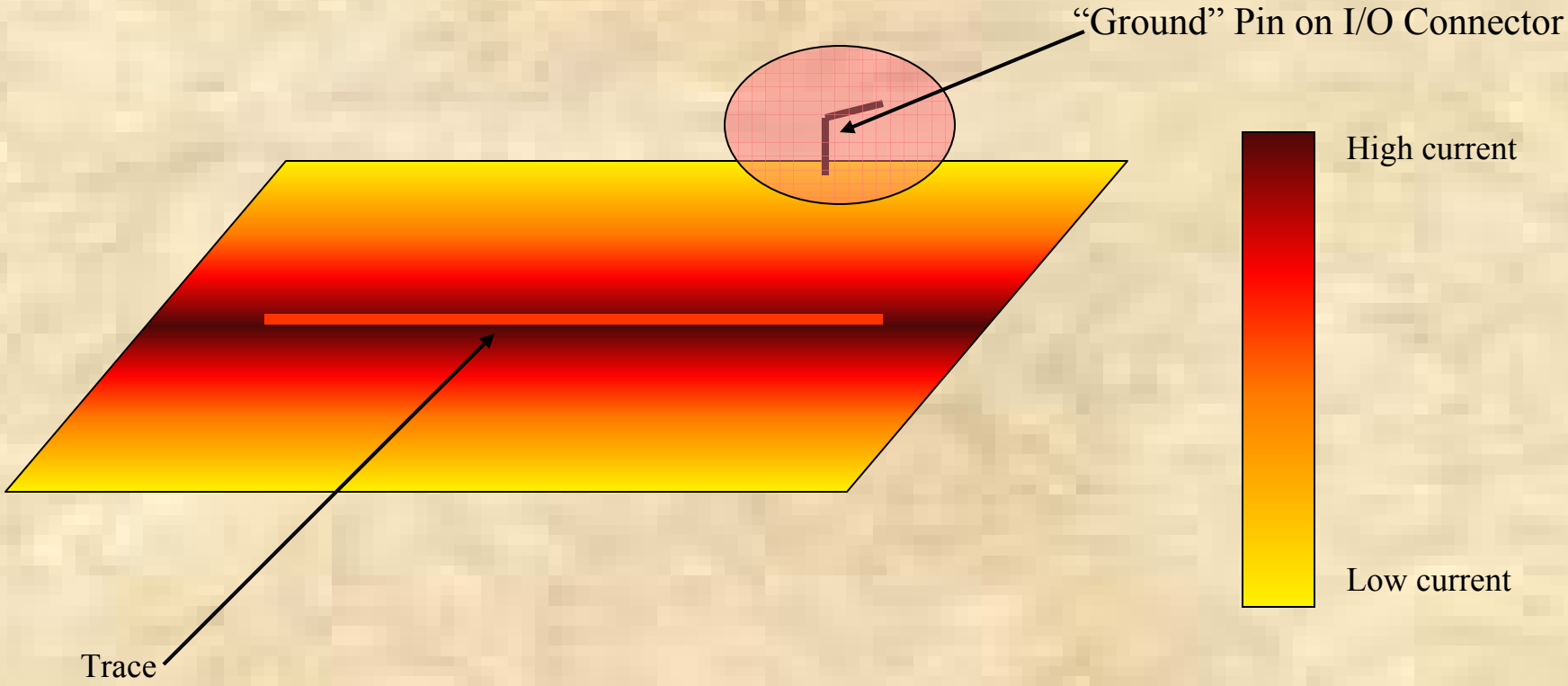
Potential Problems

- Intentional Signals
  - Loop Mode
  - Common Mode
- Unintentional Signals
  - Common Mode
  - Crosstalk Coupling
  - Power Plane Bounce
  - Above Board Structures

Unintentional Signal Emissions Common Mode

- Return current Spread
- I/O connector's pins directly connected to ground-reference plane
- results in high frequency common mode currents on external cables
- how can we stop those currents?

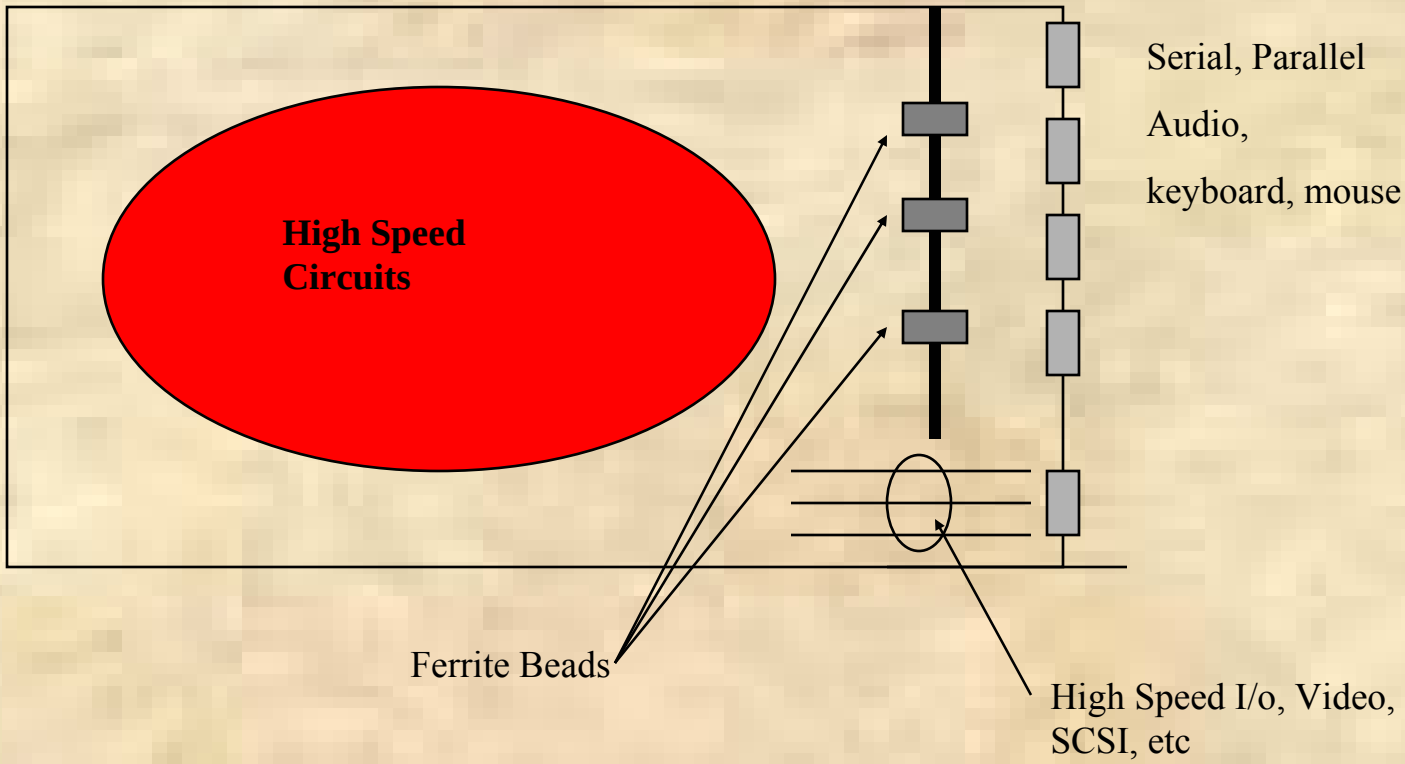
Return Current in Reference Plane with Trace Near Edge



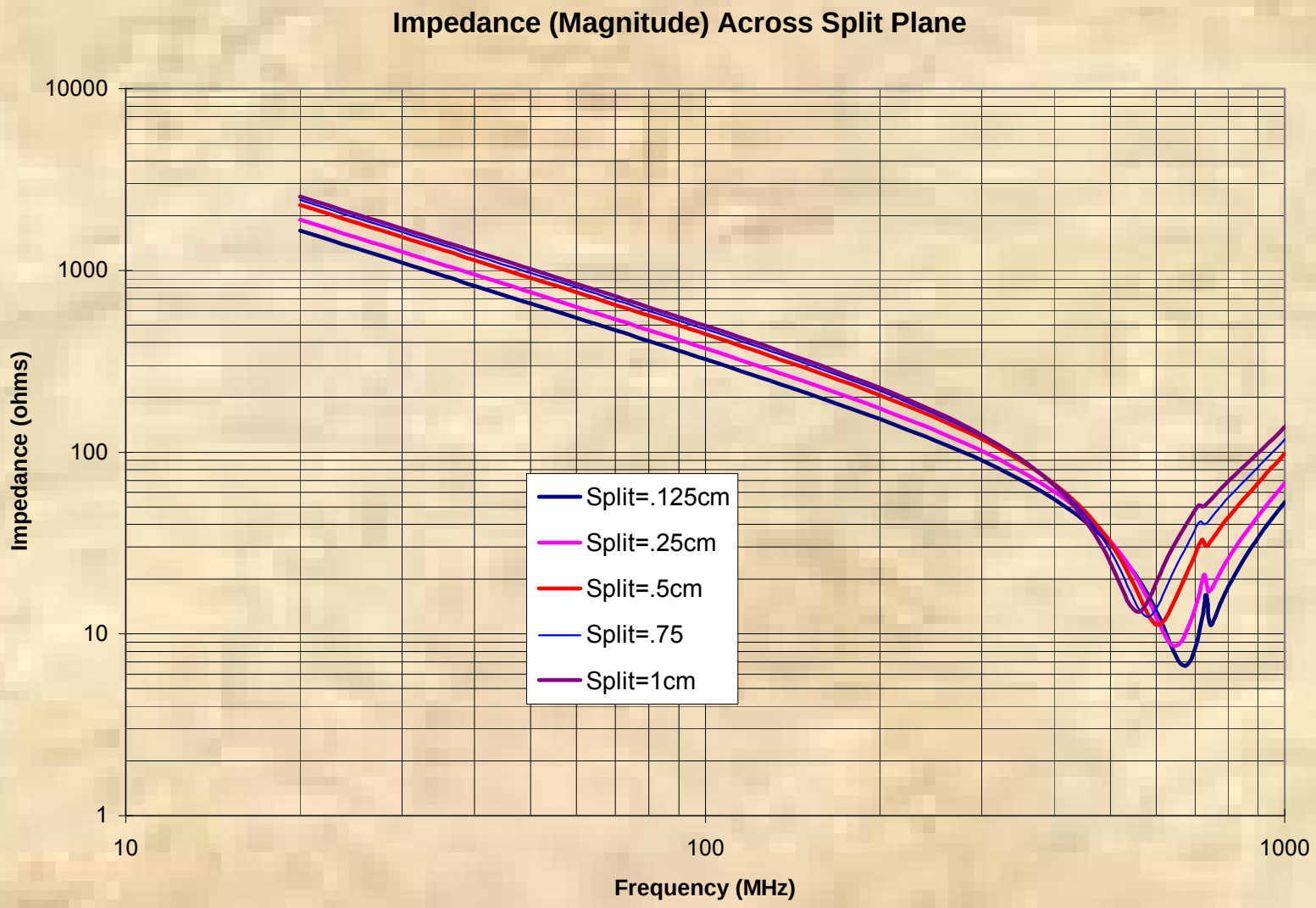
How Can We Stop These Currents?

- Split in Plane
- Treat the “Ground” pin as a *SIGNAL* Pin

I/O Ground Plane Split Example



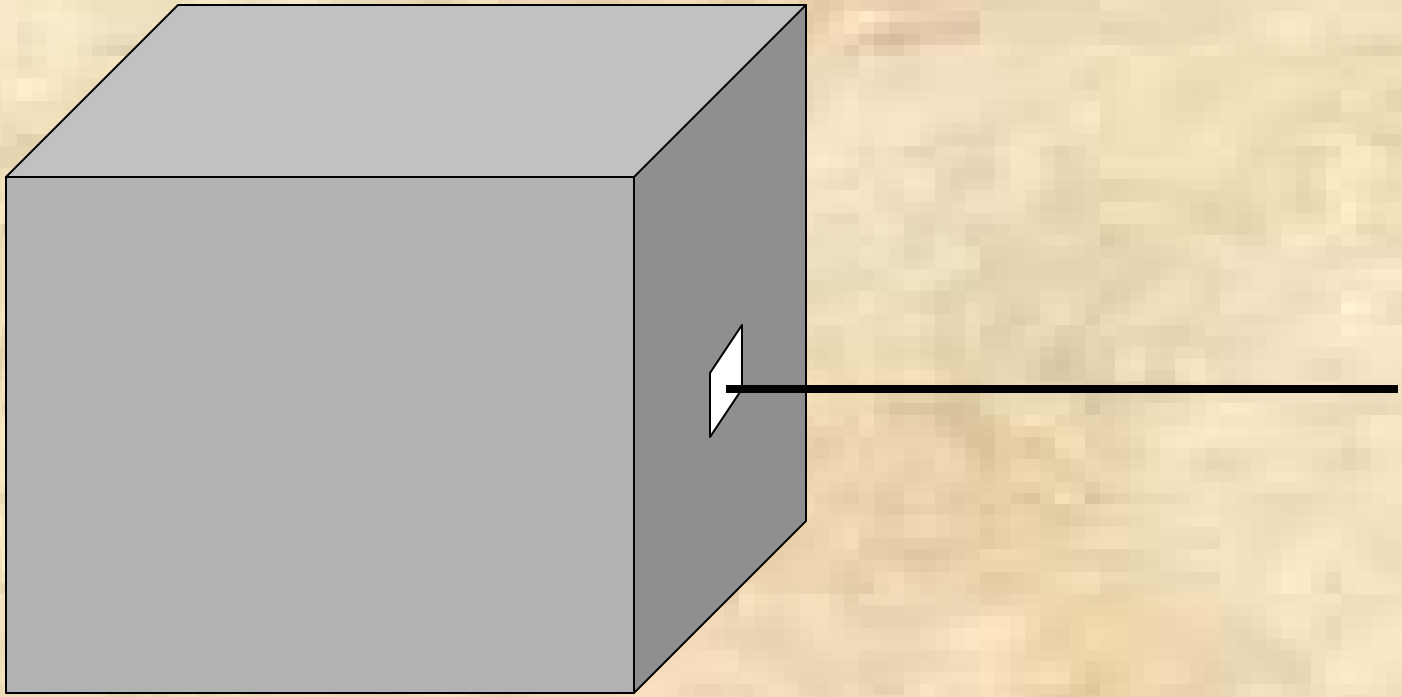
Z of split in Reference Plane

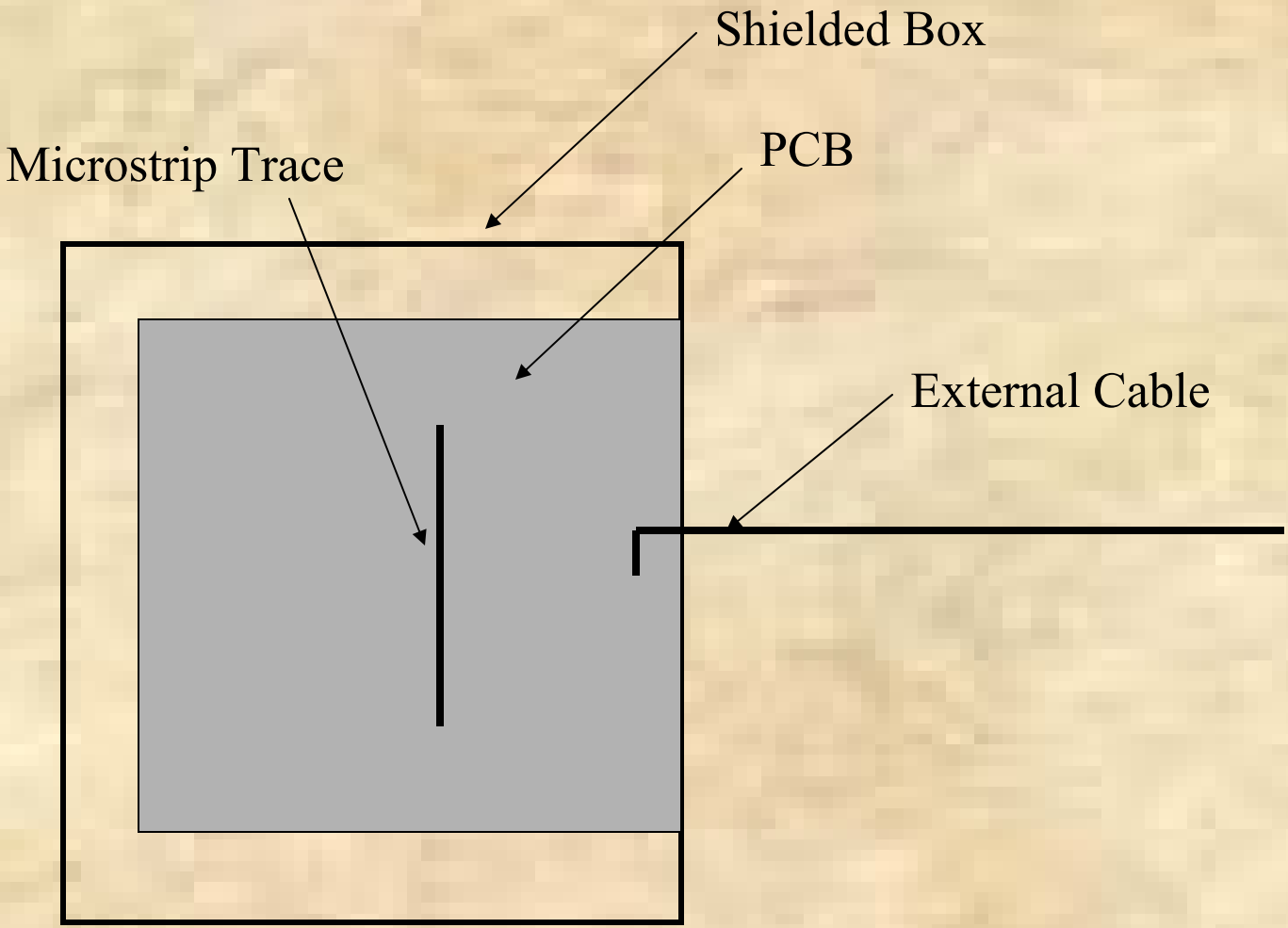


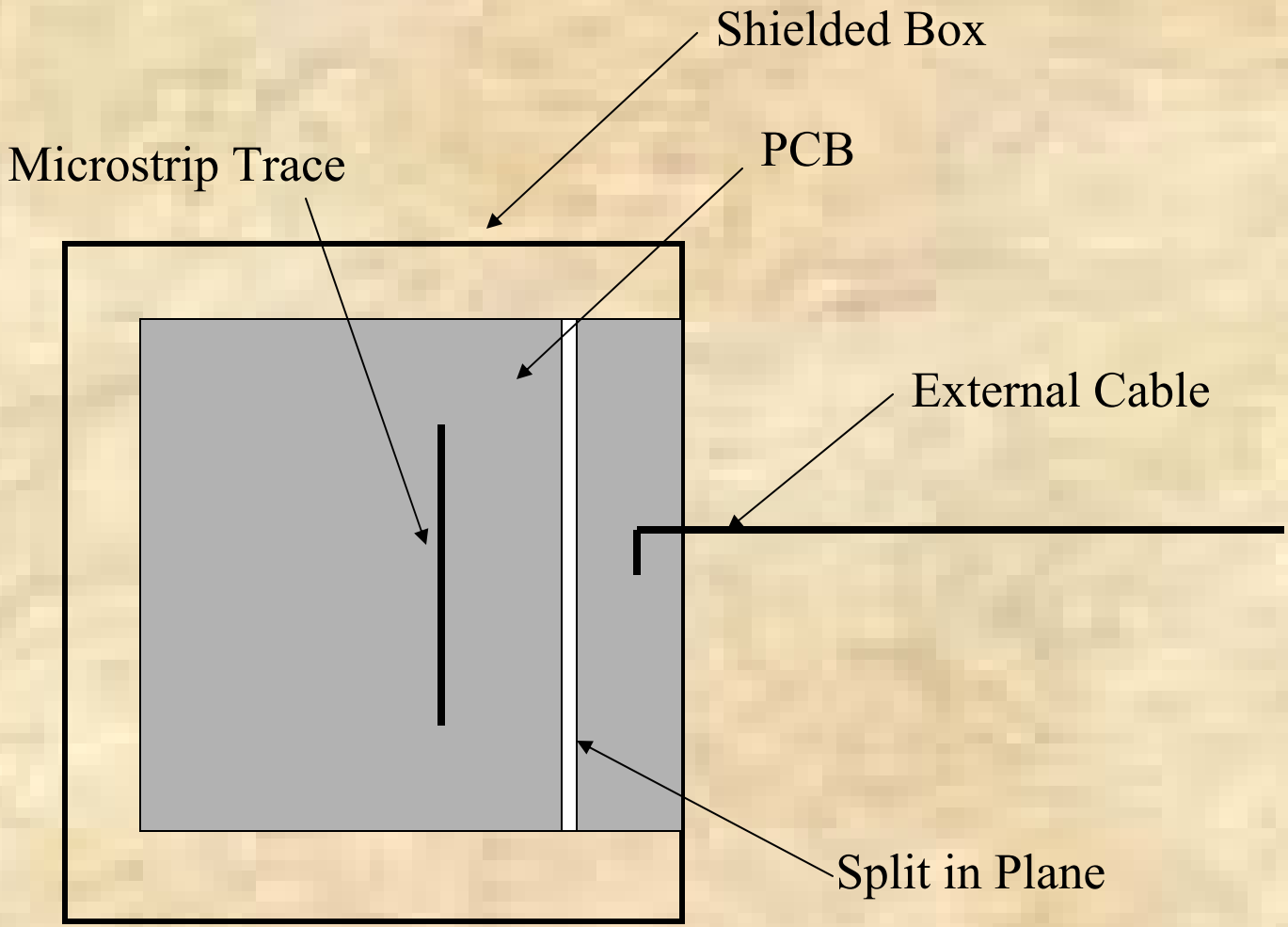
Results

- From experience --- Project X is prime example
  - Controlled Change
- From Models
  - Shielded Box with Internal PCB and single Microstrip trace
  - Connector pin on “Ground” Reference plane
    - NOT Connected to microstrip trace

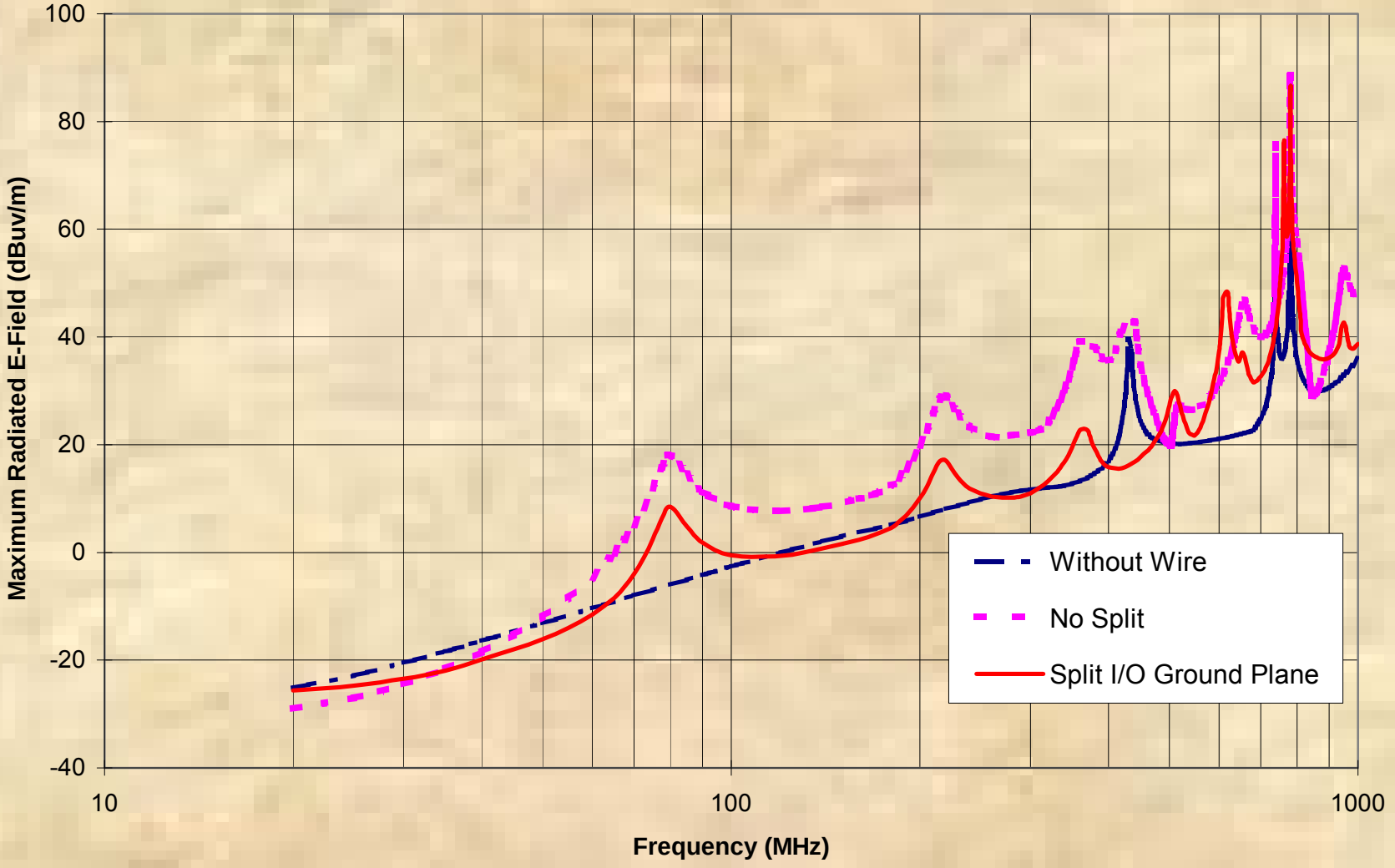
Shielded Box with Connector and Cable Attached




Shielded Box
Microstrip Trace
PCB
External Cable


Shielded Box
PCB
Microstrip Trace
External Cable
Split in Plane

Comparison of Maximum Radiated E-Field for Shielded Box with Internal PC Board With and without Split Plane near I/O area



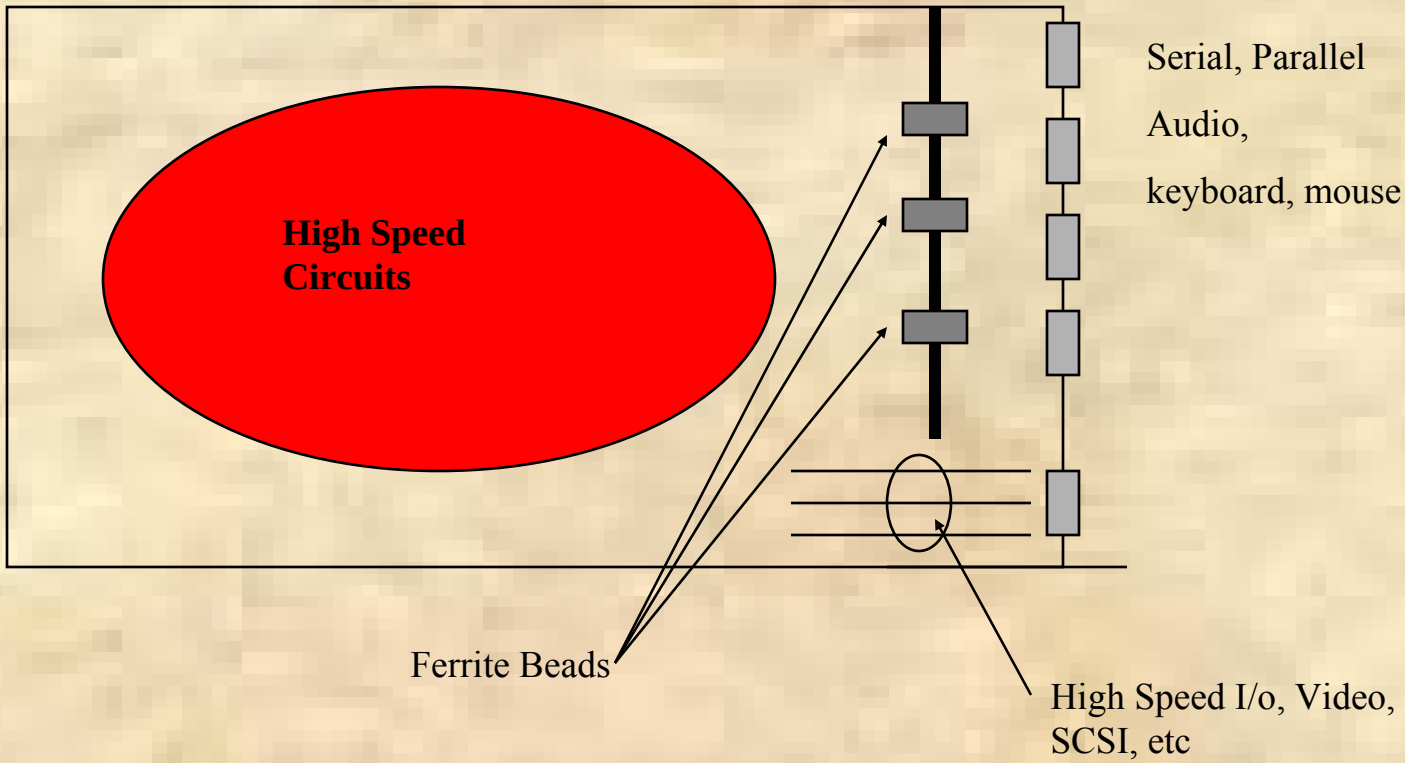
What About I/O Intentional Return Currents?

- Long way around through chassis
  - Functional and quality problems
  - Other EMC problems
- Low frequency I/O (compared to clocks)
  - Use ferrite bead across split near I/O trace crossing
    - High impedance at high frequencies
    - Low impedance at low frequencies

What About I/O Intentional Return Currents?

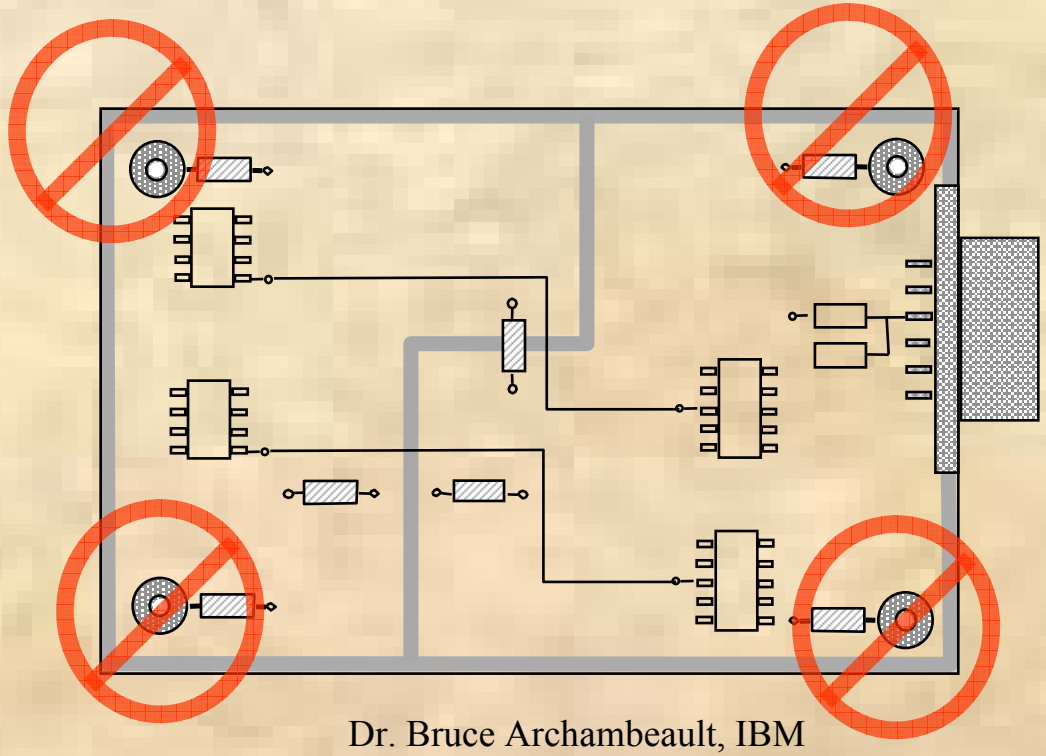
- ***NEVER*** use splits for high frequency I/O
  - Video
  - SCSI
  - USB 2.0
- Consider these signals critical signals

I/O Ground Plane Split Example



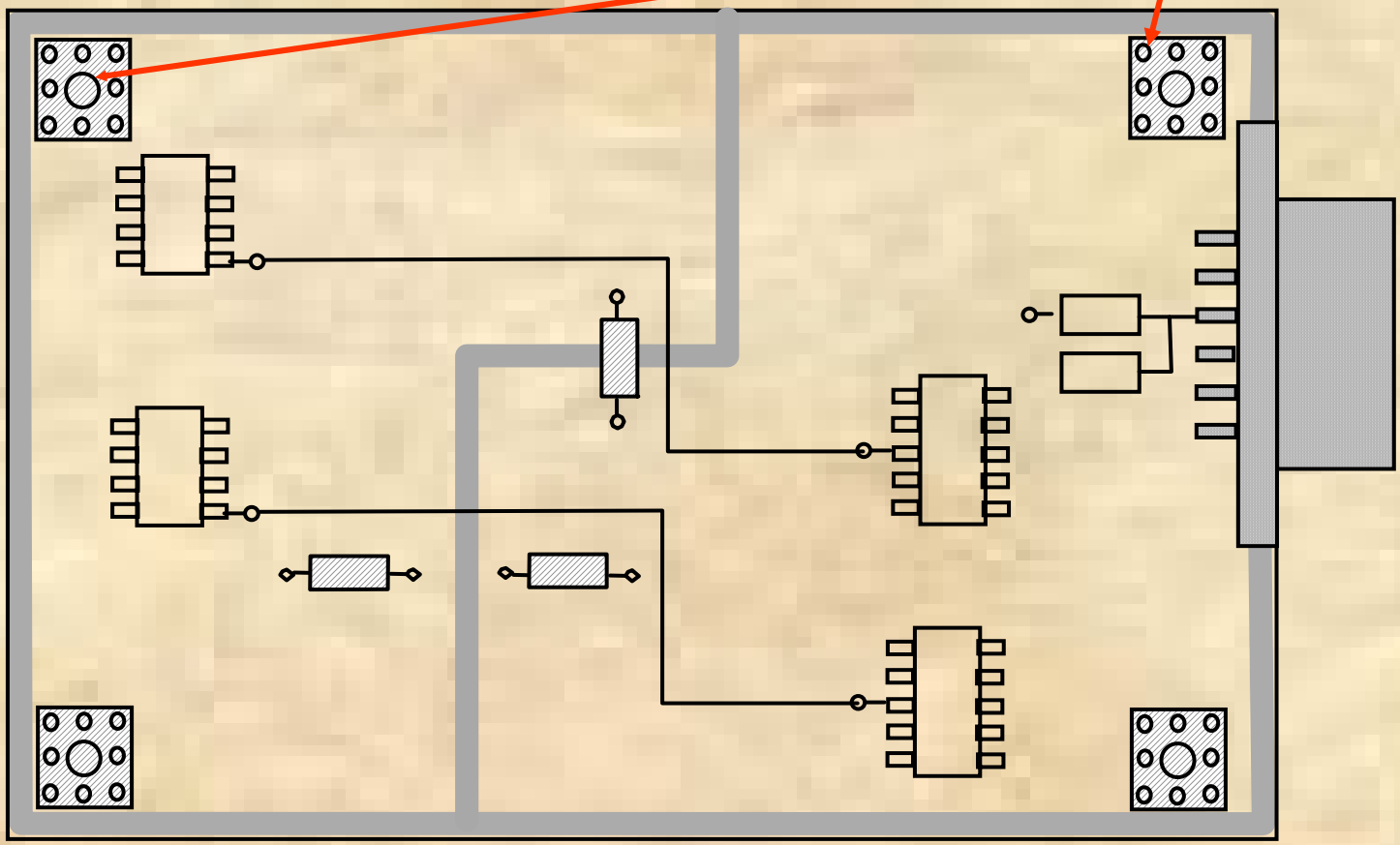
Reference to the Chassis must be through as low an impedance path as possible, especially in the I/O connector area. Never use extra components or traces

(zero ohm resistors = zero ohm ***inductors***)

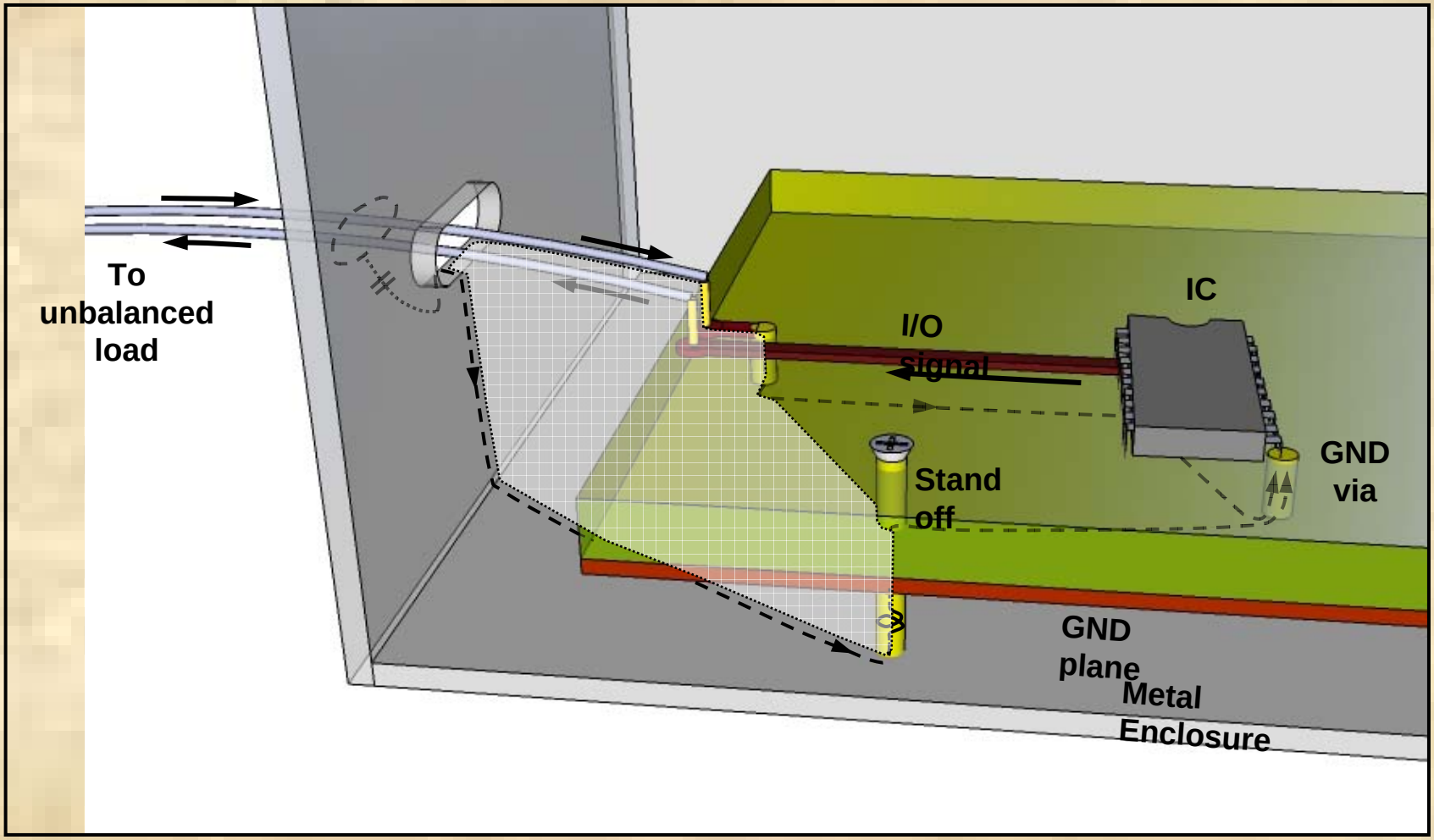


Reference to Chassis

Best Design Practice



Low Impedance Path from PCB GND Plane to Chassis?



To Prevent/Reduce Unintentional Common Mode Emissions

- ✓ Use splits as close to I/O connector as possible
  - Keep currents away from connector pins
- ✓ Ferrite across split
  - to allow intentional I/O signal return currents to return to source
- ✓ Good Low Inductance/Impedance Path to Chassis
  - External Radiation uses chassis as reference

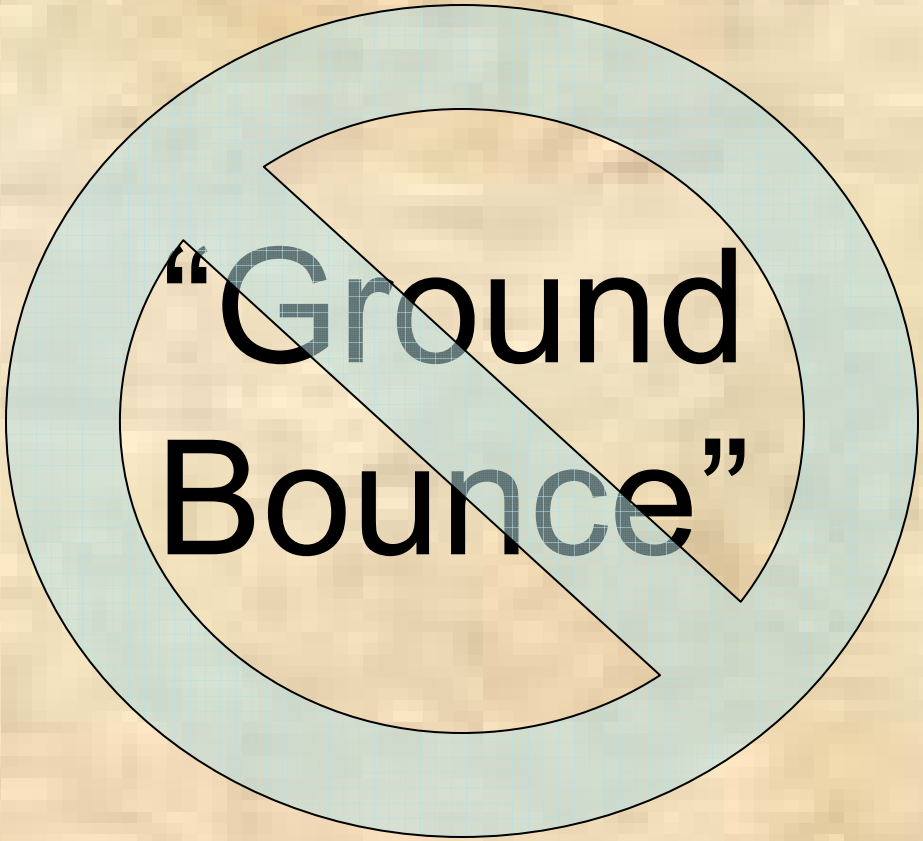
To Prevent/Reduce Unintentional Common Mode Emissions

- ✓Never use splits for high frequency I/O
  - Same as critical signals -- keep return currents close
- ✓Treat ALL connector pins as Signal pins
  - Ground pins are really signal return pins
  - Intentional signal currents are there too!
- ✓Use filters on all lines

Potential Problems

- Intentional Signals
  - Differential Mode
  - Common Mode
- Unintentional Signals
  - Common Mode
  - Crosstalk Coupling
  - Power Plane Bounce
  - Above Board Structures

Power Plane Noise Control



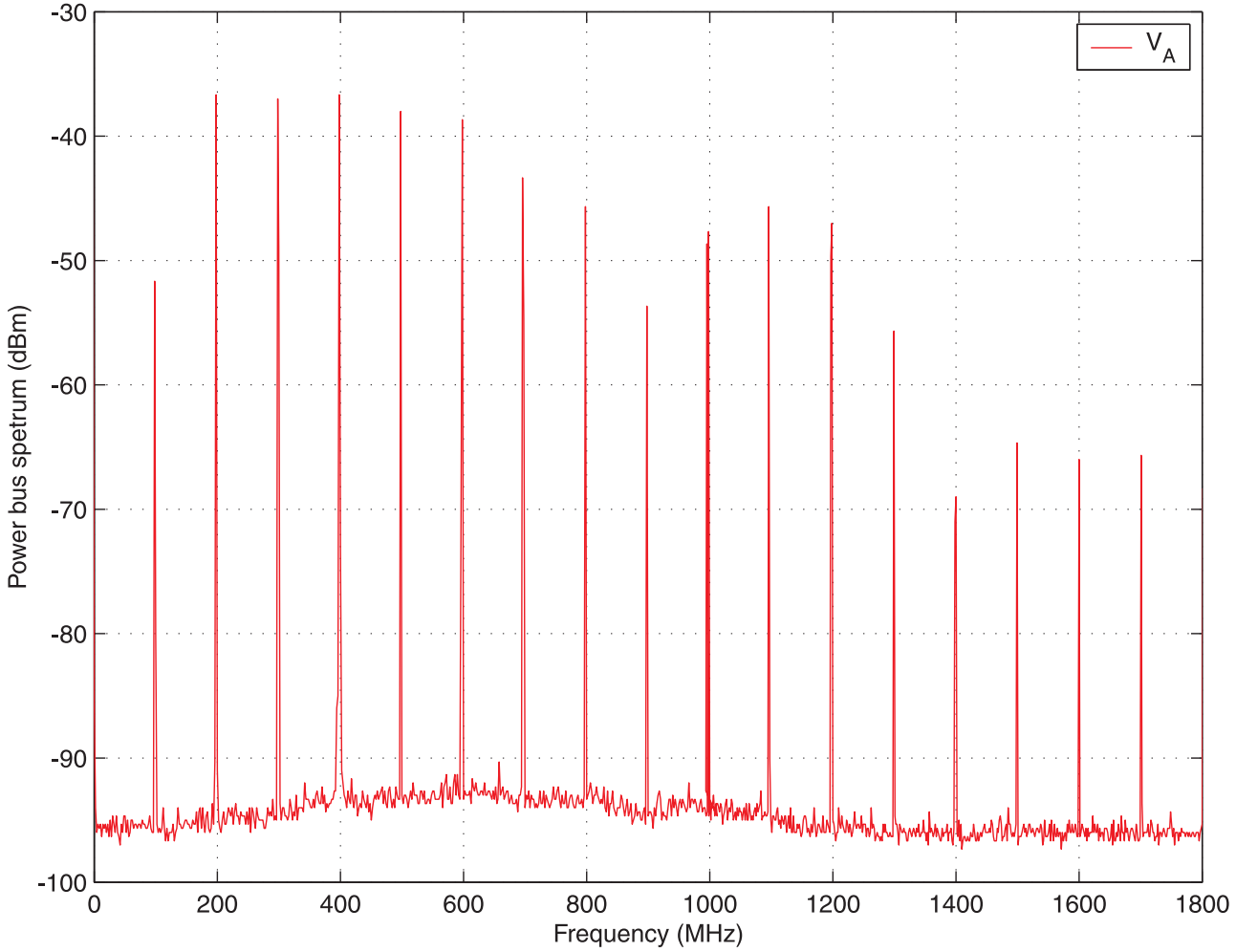
Power/Ground-Reference Plane Noise

- Must consider TWO Major Factors
  - EMC -- Reduce noise along edge of board from IC somewhere else
  - Functionality -- Provide IC with sufficient charge
- Decoupling strategies are FULL of ***Myths***
  - Consider the physics
  - Don't forget ***Inductance!***

Source of Power/Ground-Reference Plane Noise

- Power requirements from IC during switching
- Critical Net currents routed through via

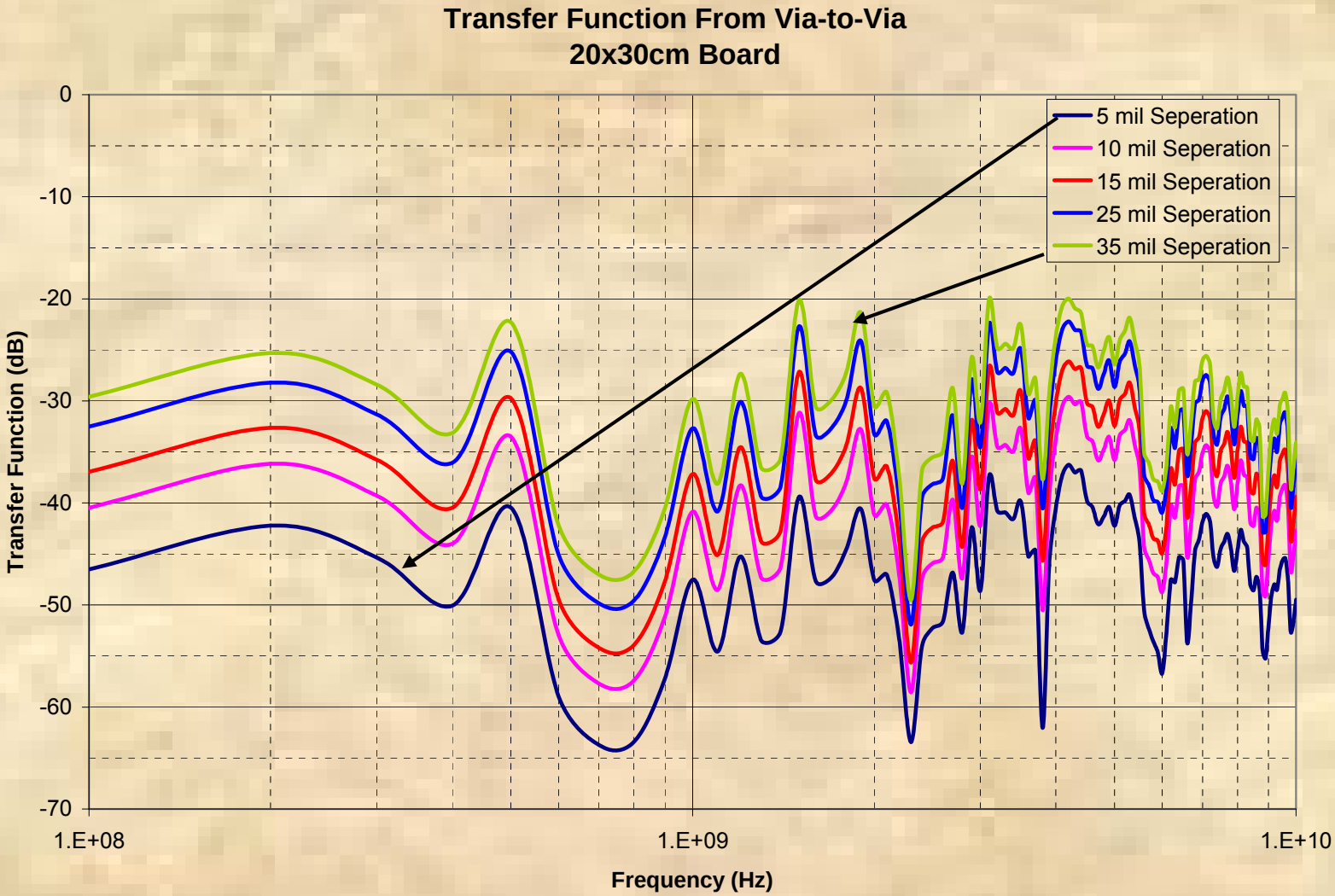
Power Bus Spectrum
Clock Driver IDT74FCT807



Noise Injected between Planes Due to Critical Net Through Via

FR4 ε_r=4.2 Loss tan=0.02

Transfer Function from Via to I/O Pin



Decoupling Must be Analyzed in Different Ways for Different Functions

- EMC
  - Resonance big concern
  - Requires STEADY-STATE analysis
    - Frequency Domain
  - Transfer function analysis
    - Eliminate noise along edge of board due to ASIC/IC located far away

Decoupling Must be Analyzed in Different Ways for Different Functions

- Provide Charge to ASIC/IC
  - Requires TRANSIENT analysis
  - Charge will NOT travel from far corners of the board fast enough
  - Local decoupling capacitors dominate
  - Impedance at ASIC/IC pins important

Steady-State Analysis

- Measurements and Simulations
- Test Board with Decoupling capacitors every 1” square

Test Board Ports

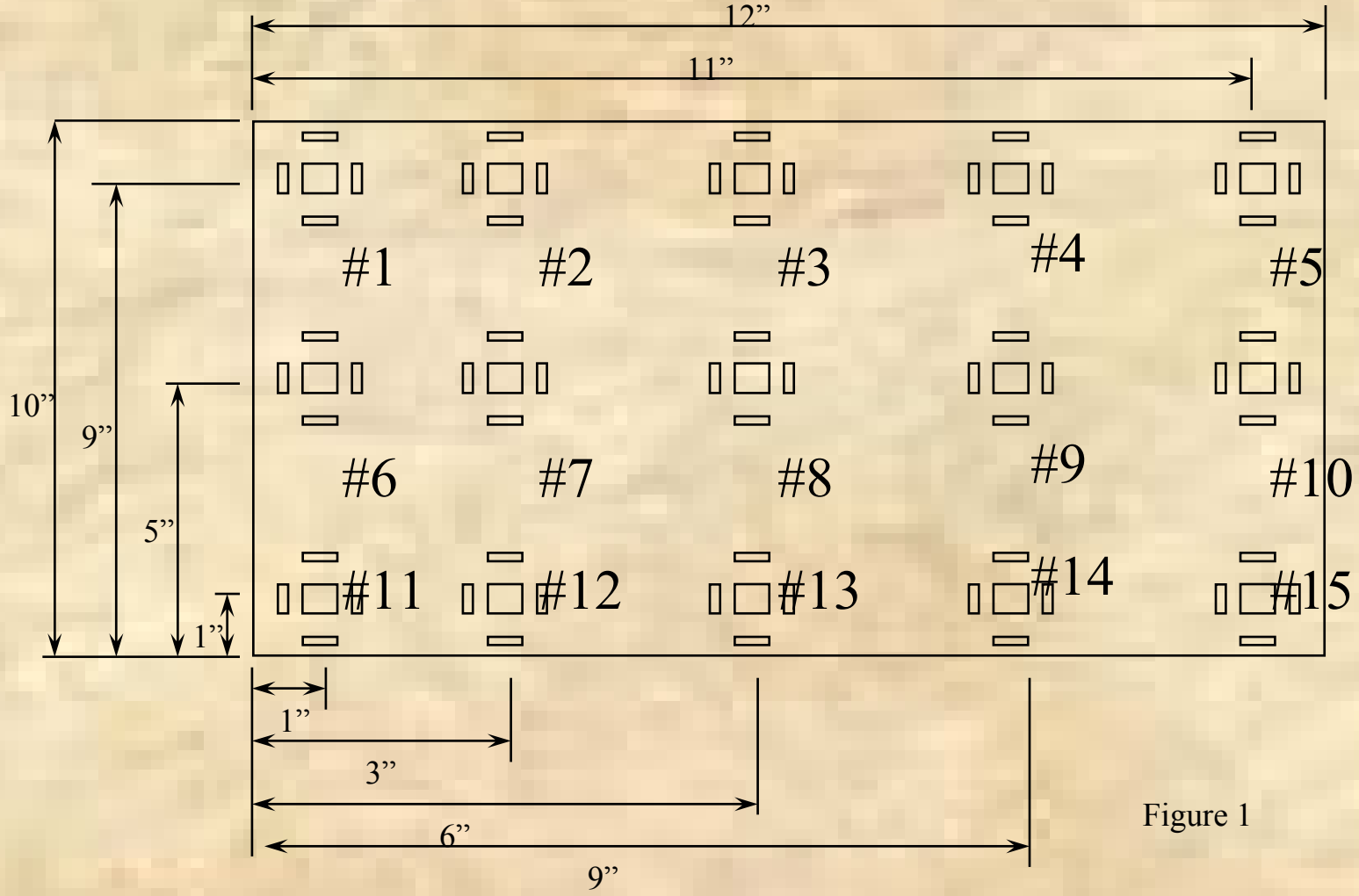
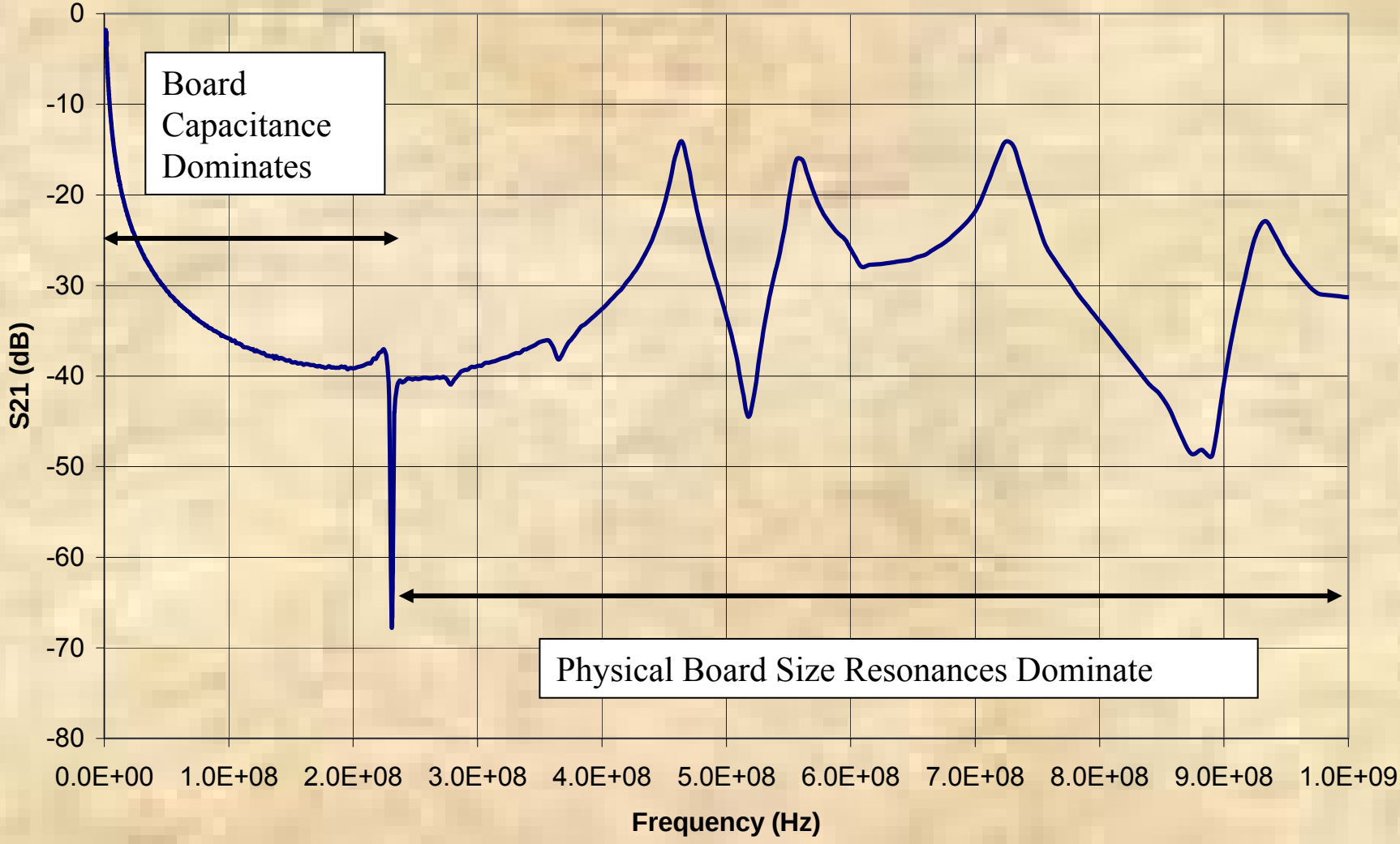


Figure 1

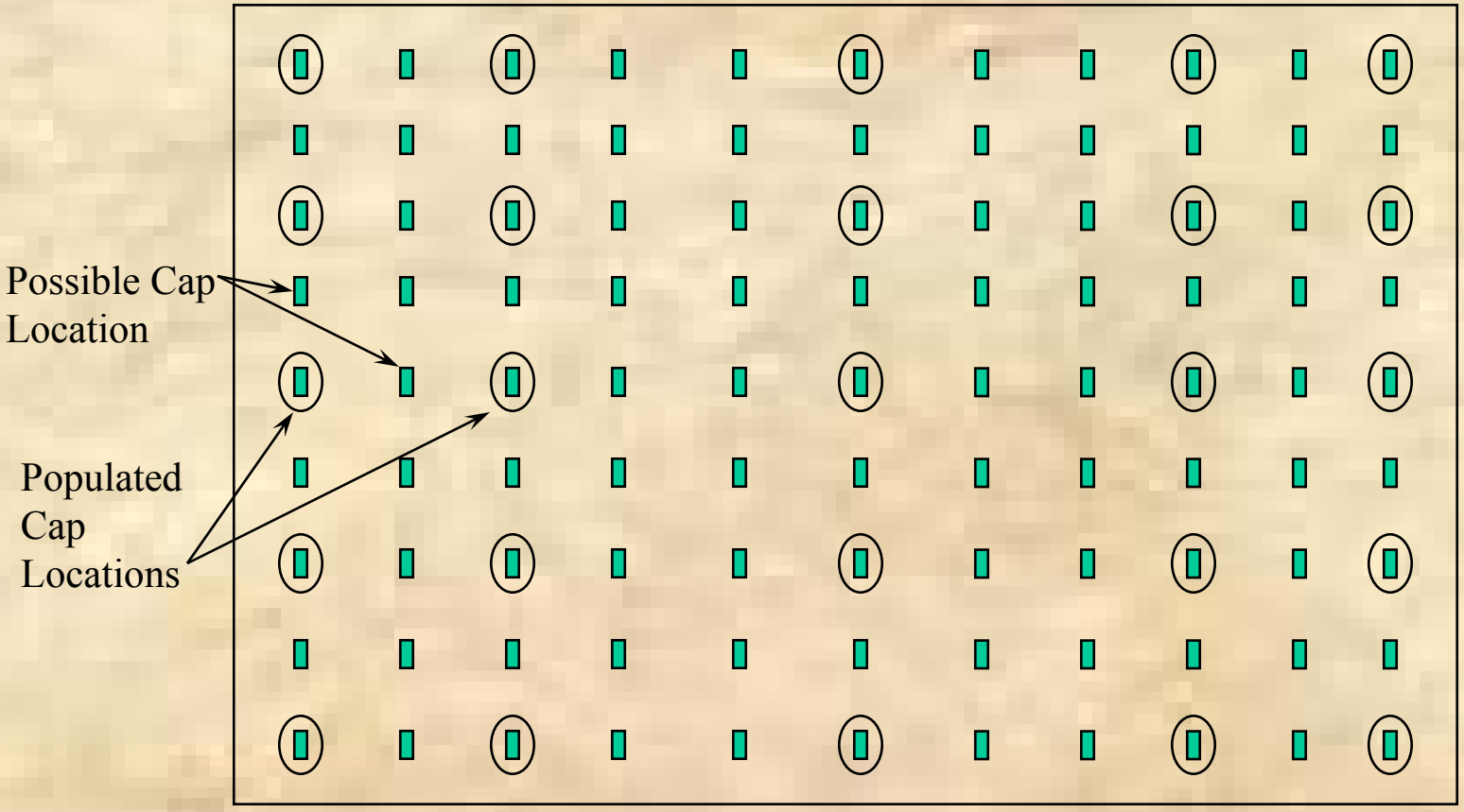
S21 Used for Decoupling "Goodness"

- Ratio of Power 'out' to power 'in'
- Better Indicator of EMI noise transmission across board
- Also used to validate simulations

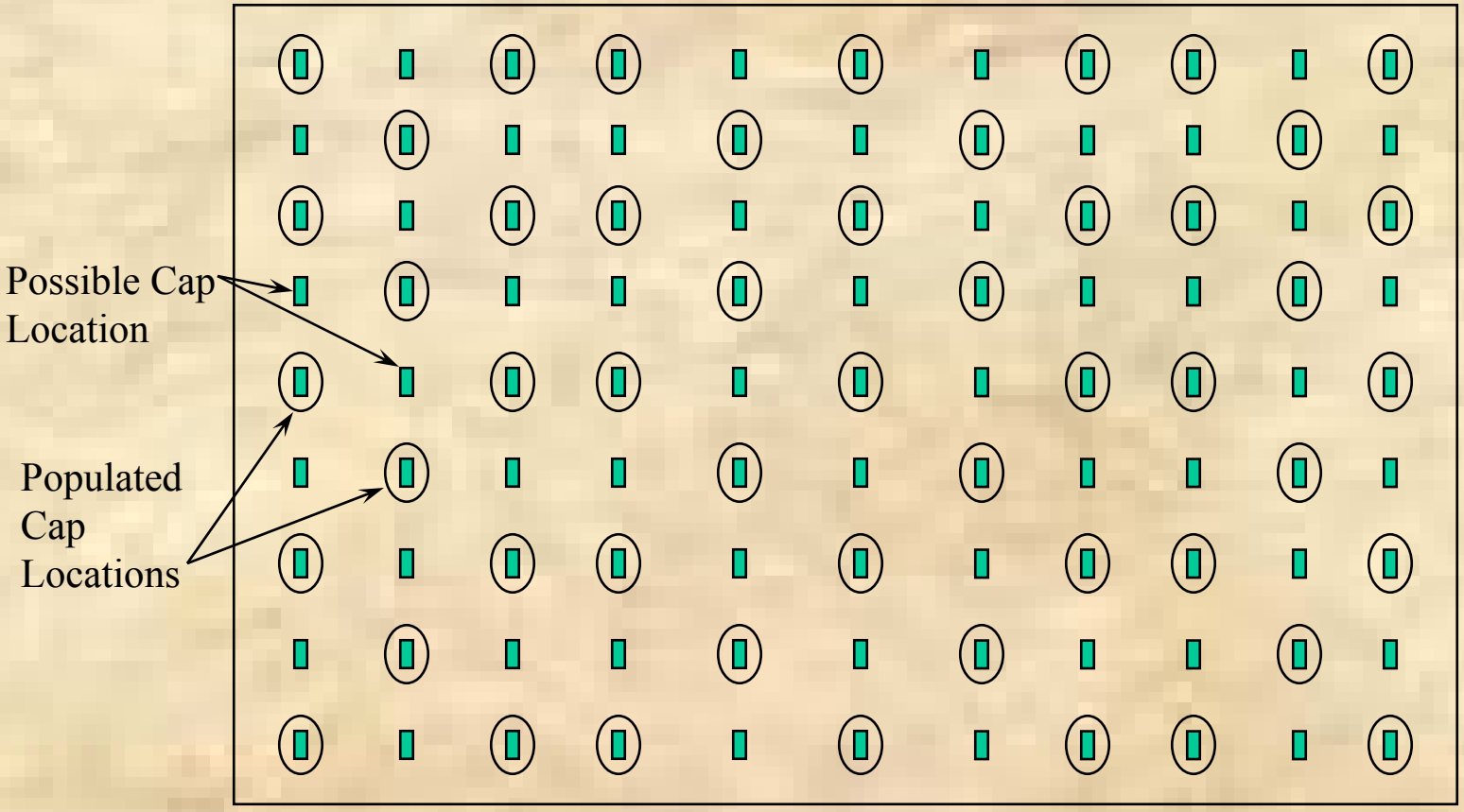
Measured S21 for 12" x 10" PC Board Between Power/Ground Planes with No Decoupling Capacitors (Measured Center to Corner)



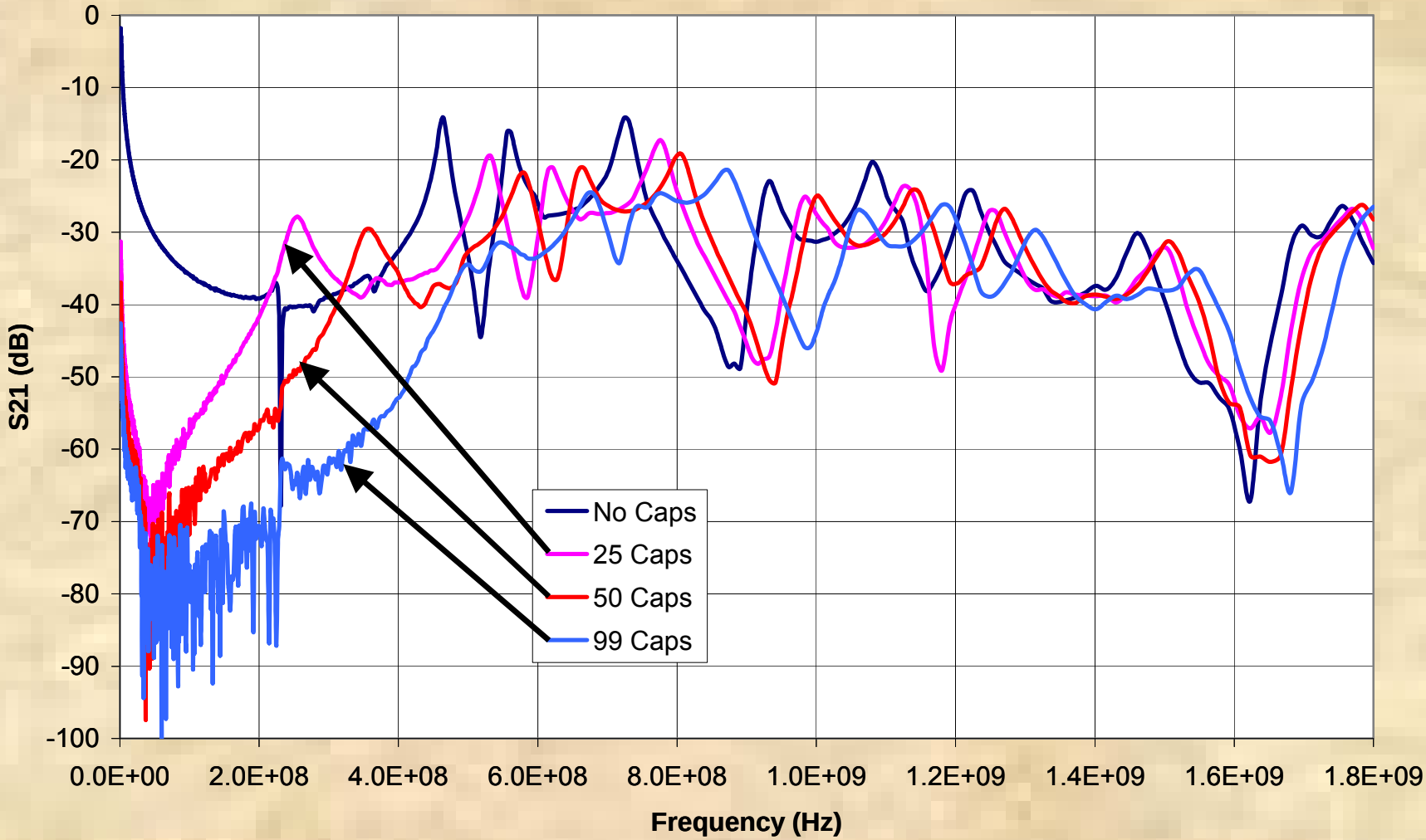
Test Board Decoupling Capacitor Placement for 25 .01 uf Caps

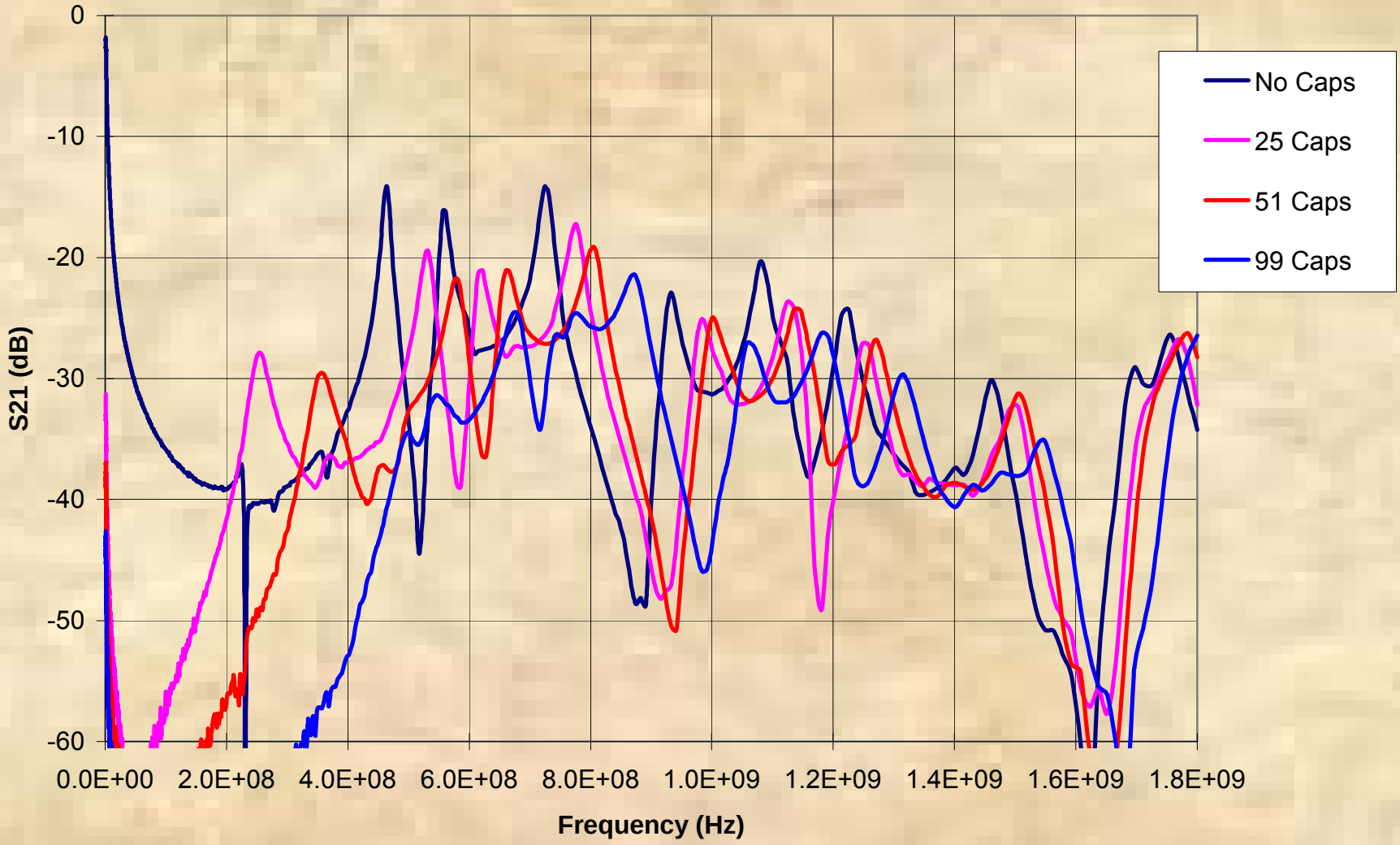


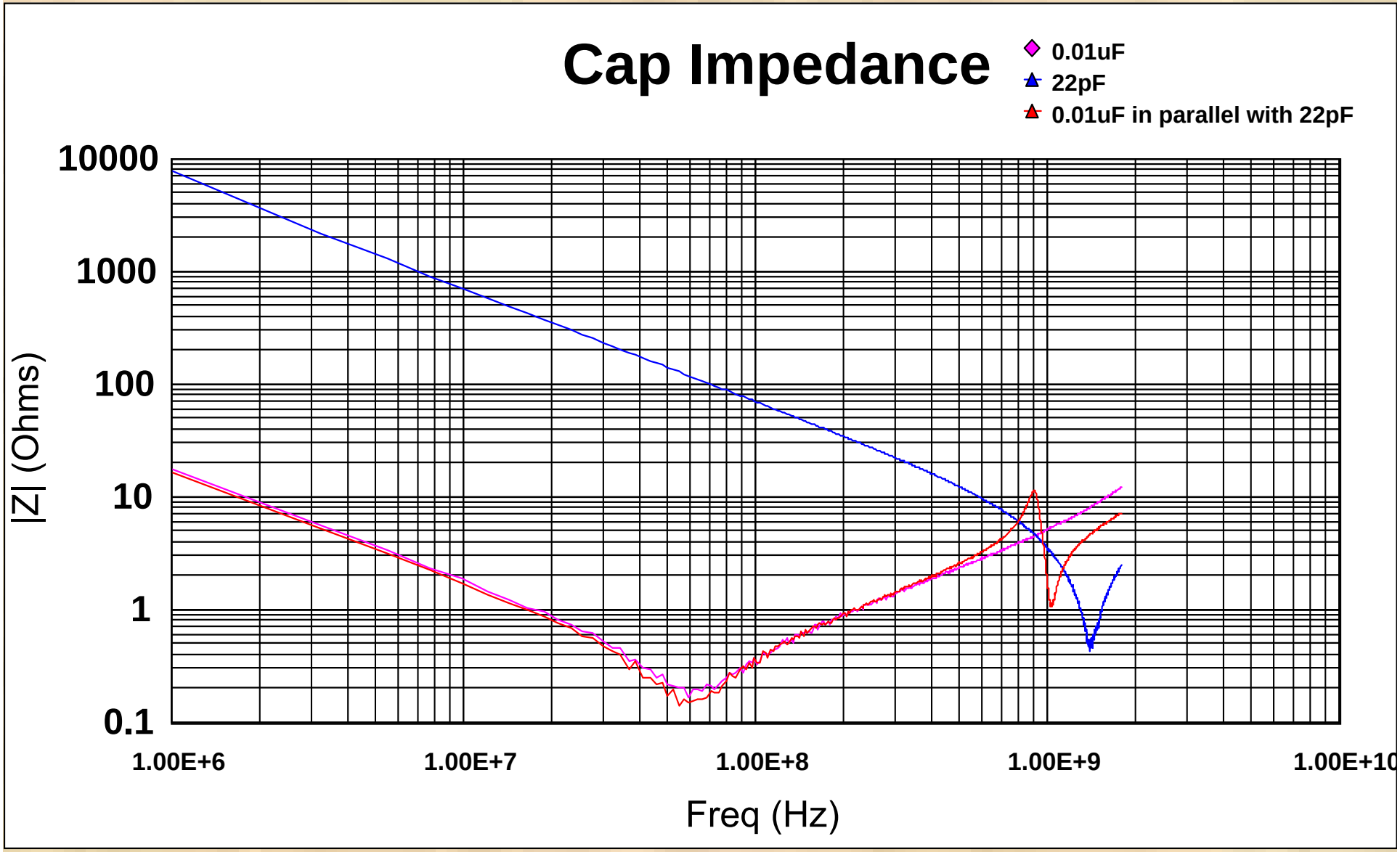
Test Board Decoupling Capacitor Placement for 51 .01 uf Caps



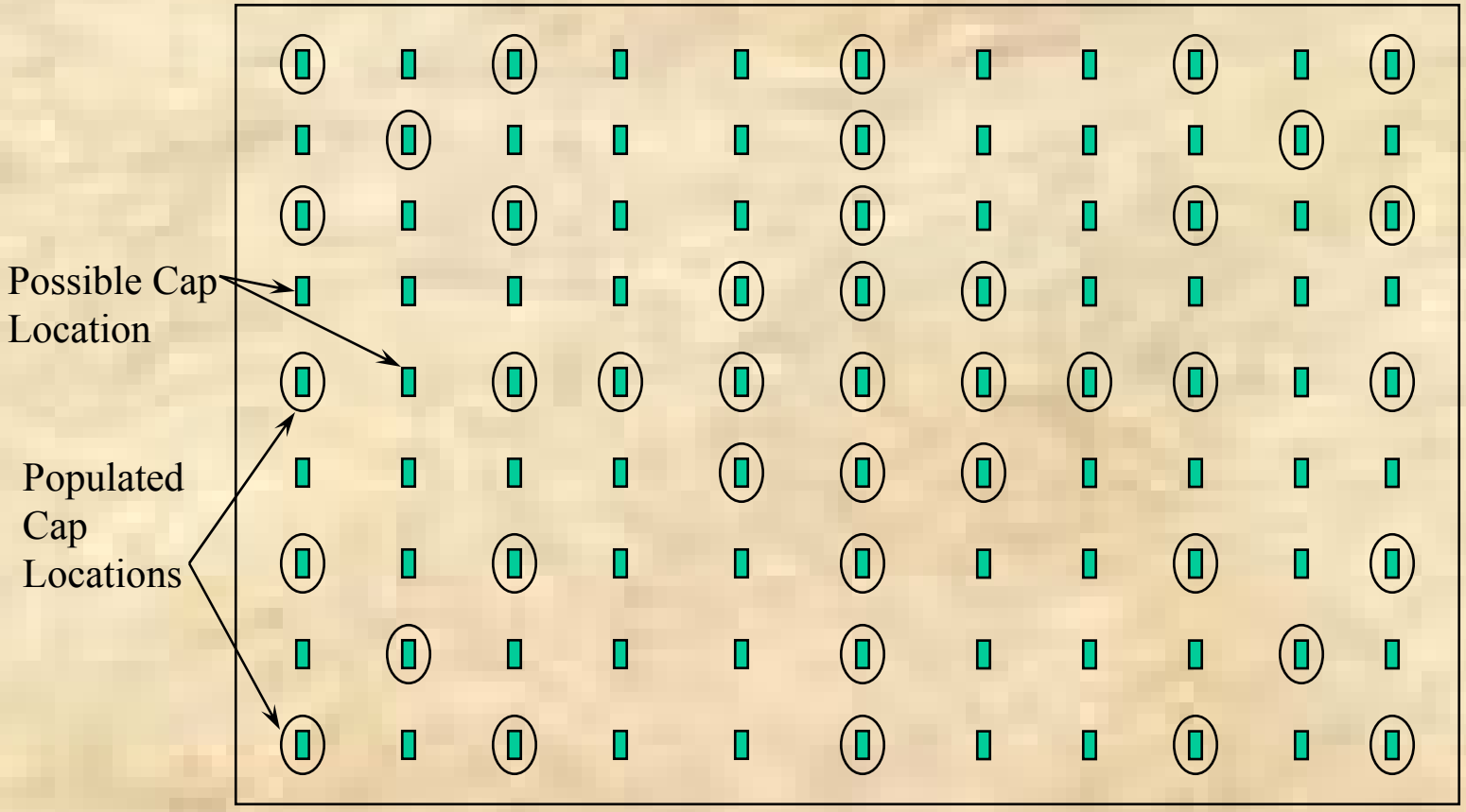
Measured S21 for 12" x 10" PC Board Between Power/Ground Planes with Various Amounts of Decoupling Capacitors (Measured Center to Corner)



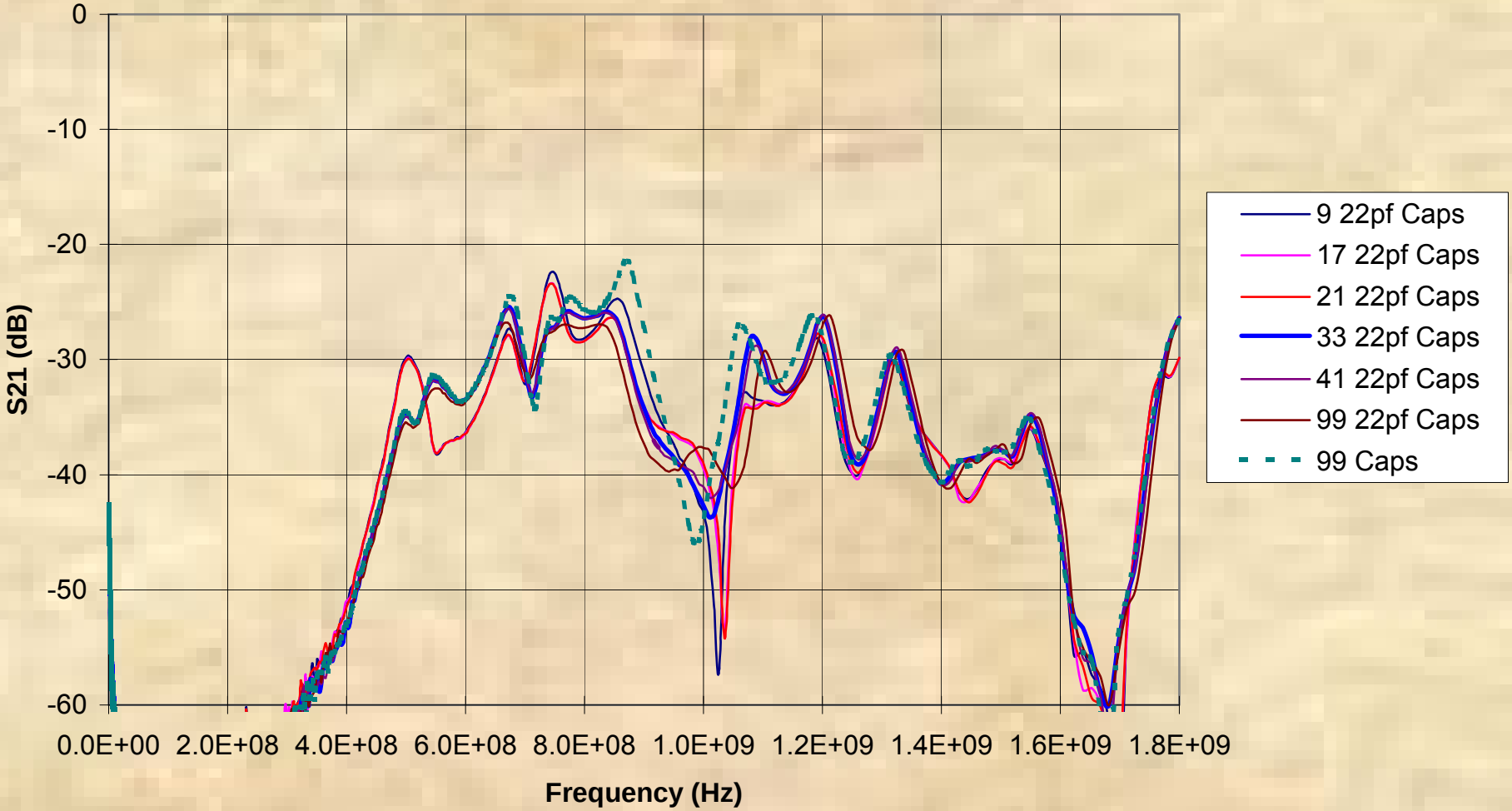

S21 Between Port #8 and Port #1 on Test Board
With Various Amounts of .01 uf Decoupling Capacitors
S21 (dB)
0
-10
-20
-30
-40
-50
-60
0.0E+00
2.0E+08
4.0E+08
6.0E+08
8.0E+08
1.0E+09
1.2E+09
1.4E+09
1.6E+09
1.8E+09
Frequency (Hz)
No Caps
25 Caps
51 Caps
99 Caps


Cap Impedance
0.01uF
22pF
0.01uF in parallel with 22pF
10000
1000
100
10
1
0.1
|Z| (Ohms)
1.00E+6
1.00E+7
1.00E+8
1.00E+9
1.00E+10
Freq (Hz)

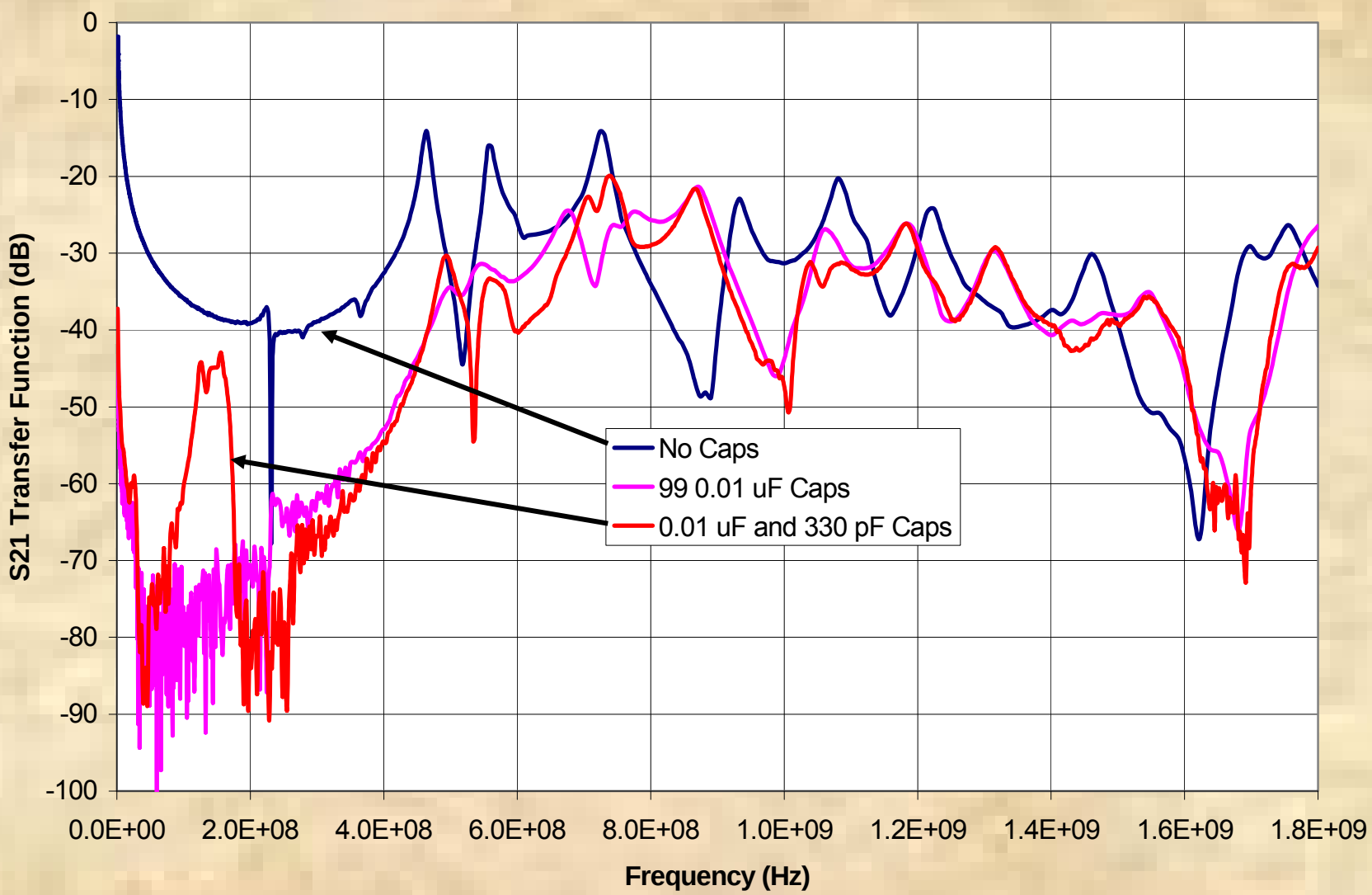
Test Board Decoupling Capacitor Placement for 41 22pf Caps (In Addition to 99 .01uf Caps)

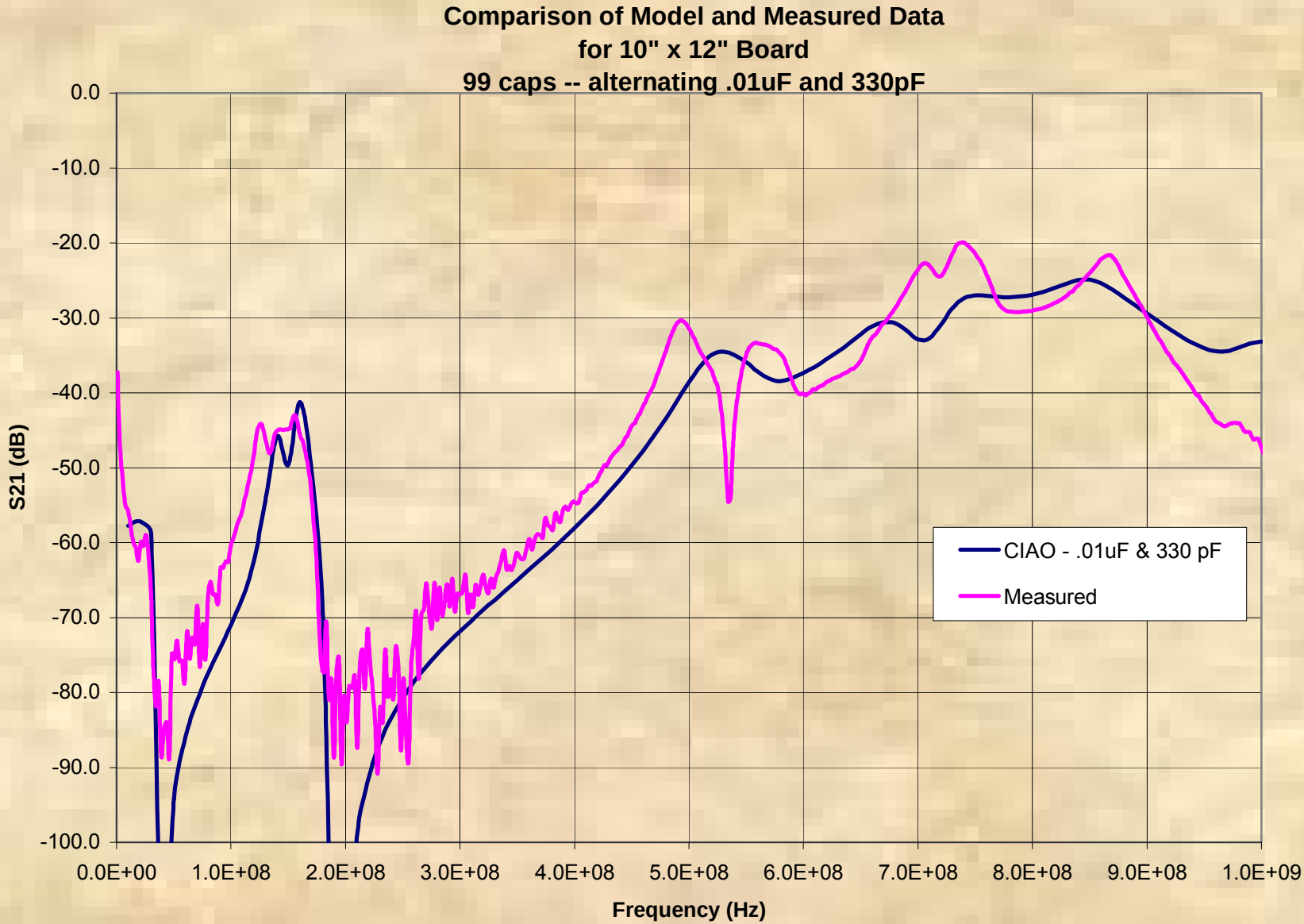


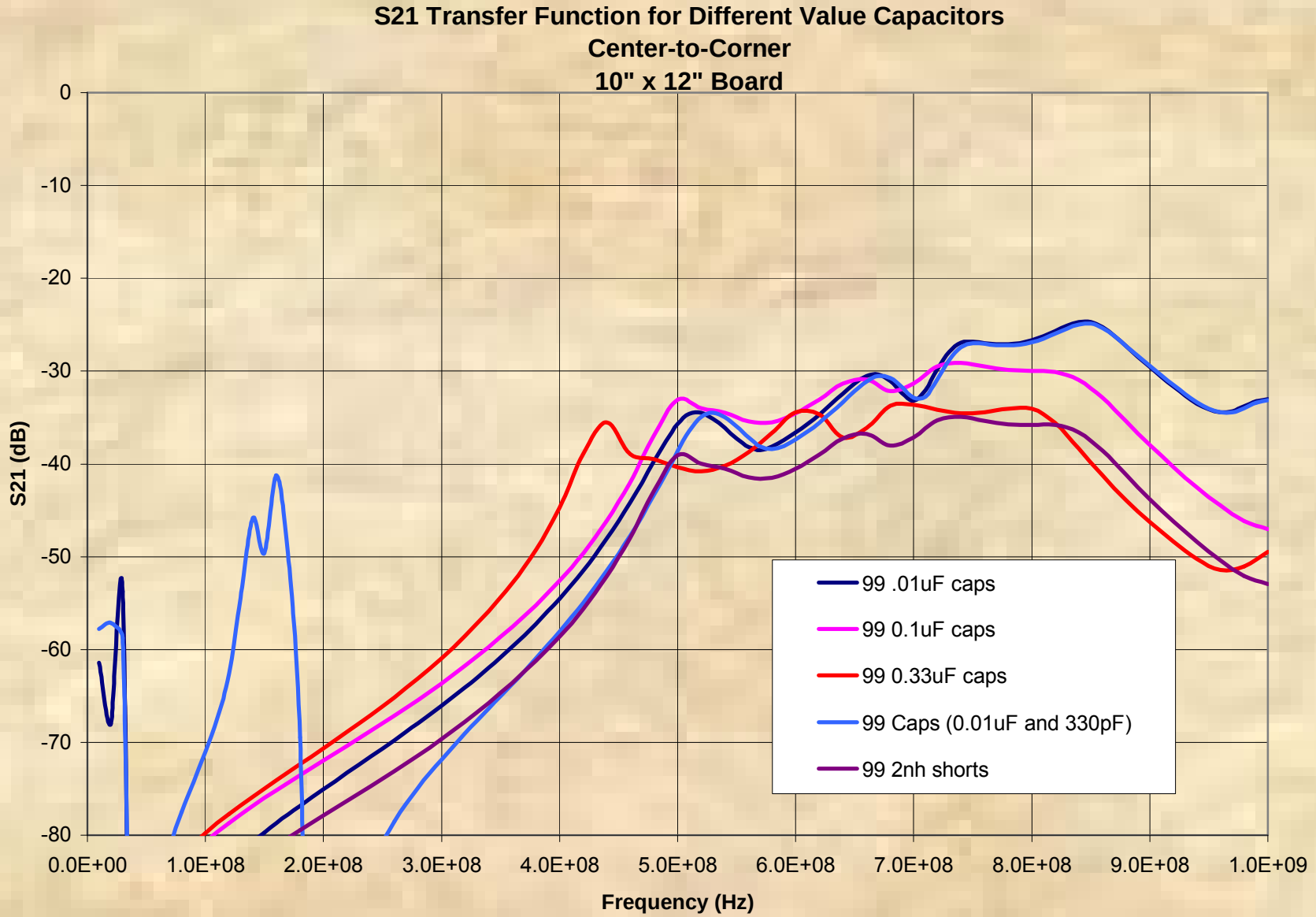
S21 Between Port #8 and Port #1 on Test Board With 99 .01 uf Decoupling Capacitors and Various Amounts of 22pf Capacitors Added



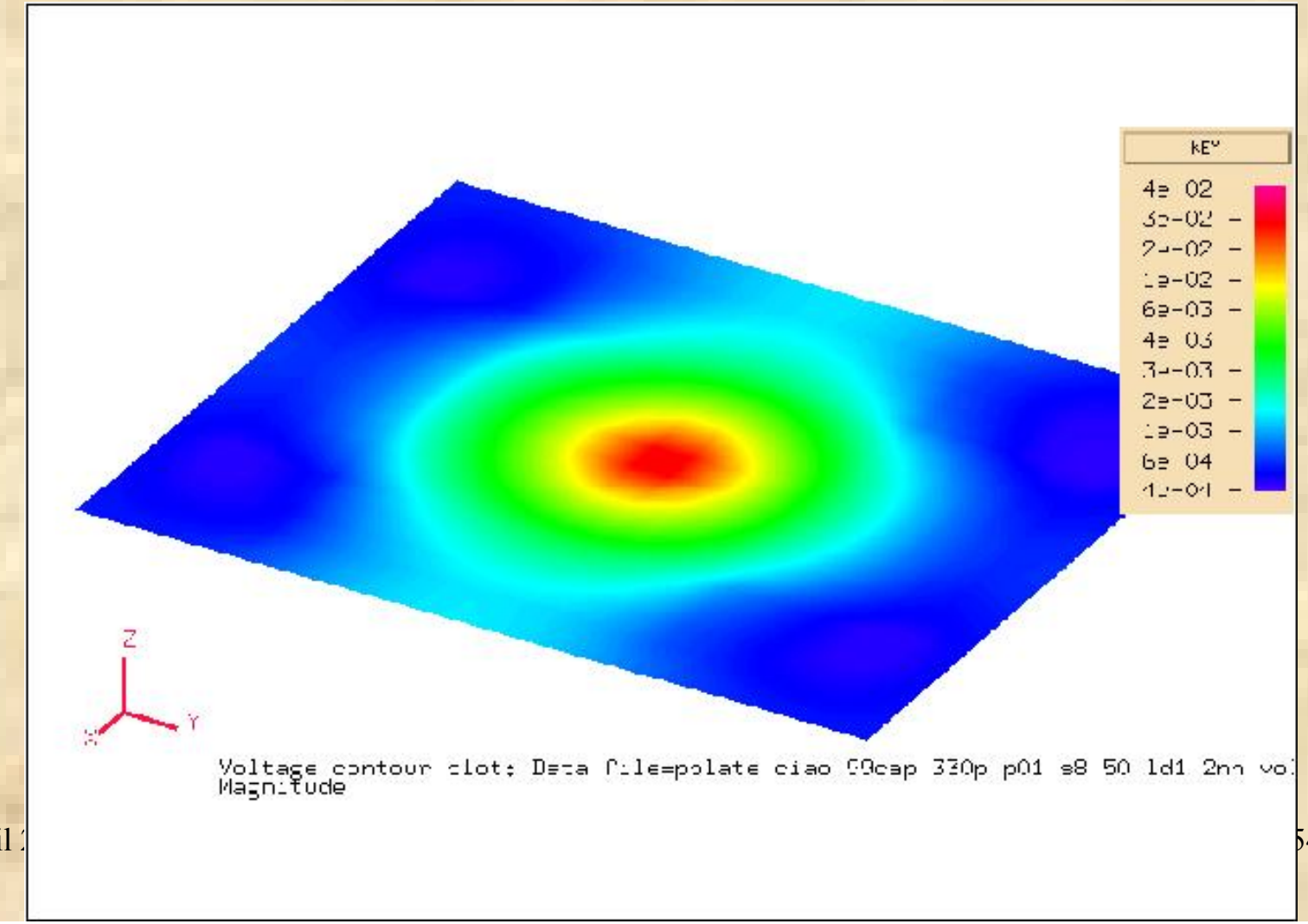
Measured Comparison of Multiple and Single Value Decoupling Capacitor Strategies



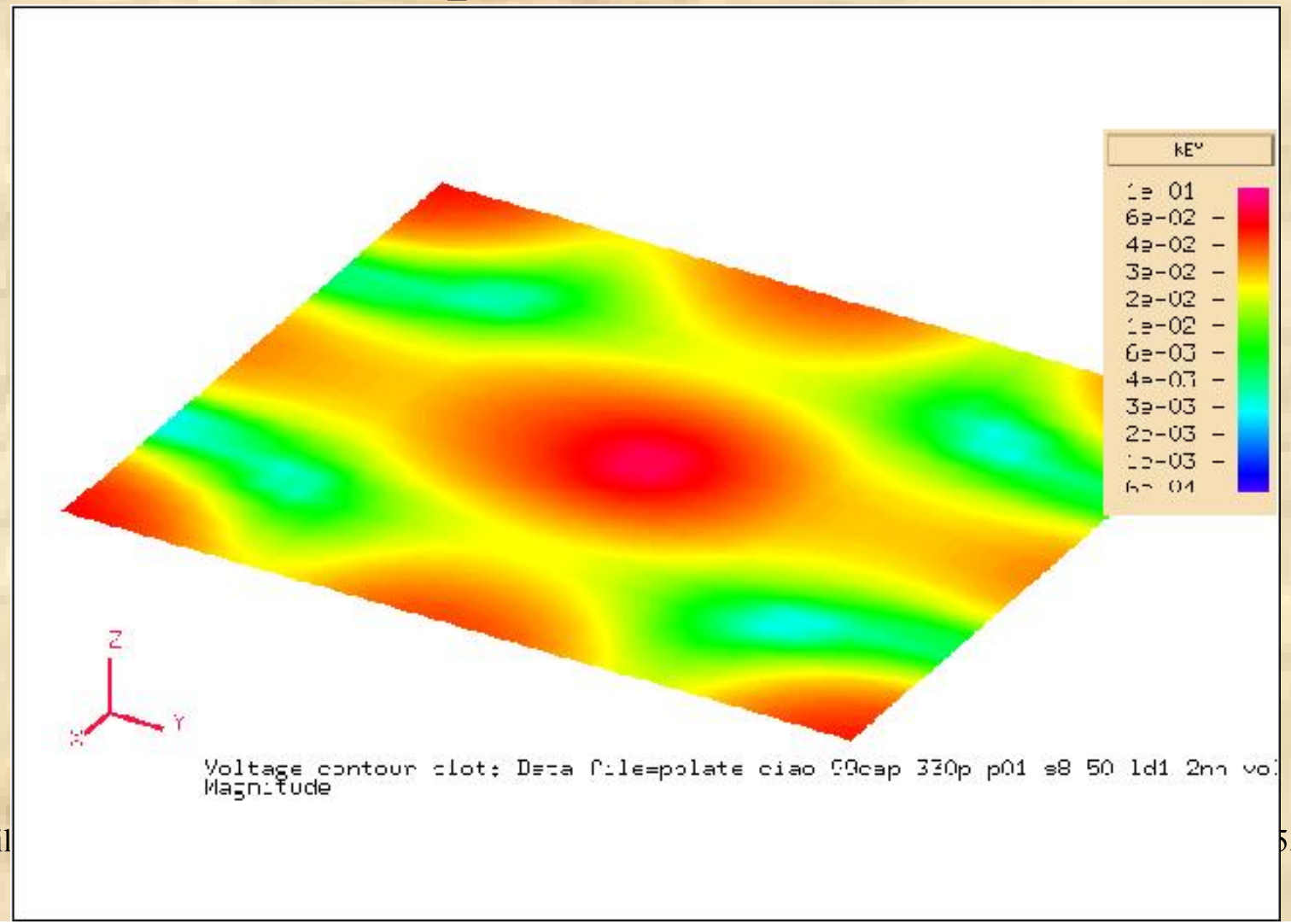

Comparison of Model and Measured Data
for 10" x 12" Board
99 caps -- alternating .01uF and 330pF
S21 (dB)
0.0
-10.0
-20.0
-30.0
-40.0
-50.0
-60.0
-70.0
-80.0
-90.0
-100.0
0.0E+00
1.0E+08
2.0E+08
3.0E+08
4.0E+08
5.0E+08
6.0E+08
7.0E+08
8.0E+08
9.0E+08
1.0E+09
Frequency (Hz)
CIAO - .01uF & 330 pF
Measured


S21 Transfer Function for Different Value Capacitors
Center-to-Corner
10" x 12" Board
S21 (dB)
0
-10
-20
-30
-40
-50
-60
-70
-80
0.0E+00
1.0E+08
2.0E+08
3.0E+08
4.0E+08
5.0E+08
6.0E+08
7.0E+08
8.0E+08
9.0E+08
1.0E+09
Frequency (Hz)
99 .01uF caps
99 0.1uF caps
99 0.33uF caps
99 Caps (0.01uF and 330pF)
99 2nh shorts

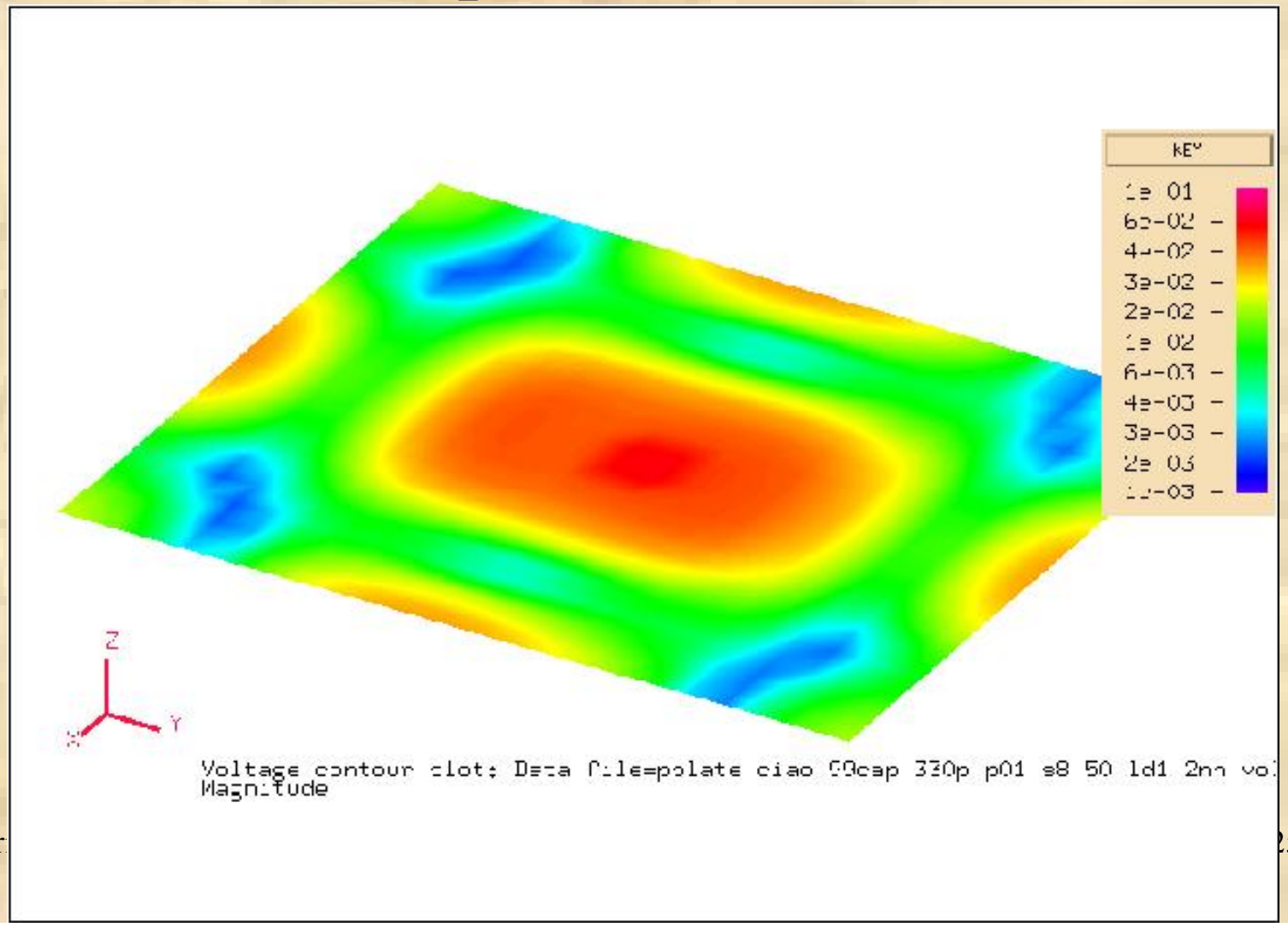
Voltage Distribution @ 350 MHz .01uF and 330pF Case (Source in Center)



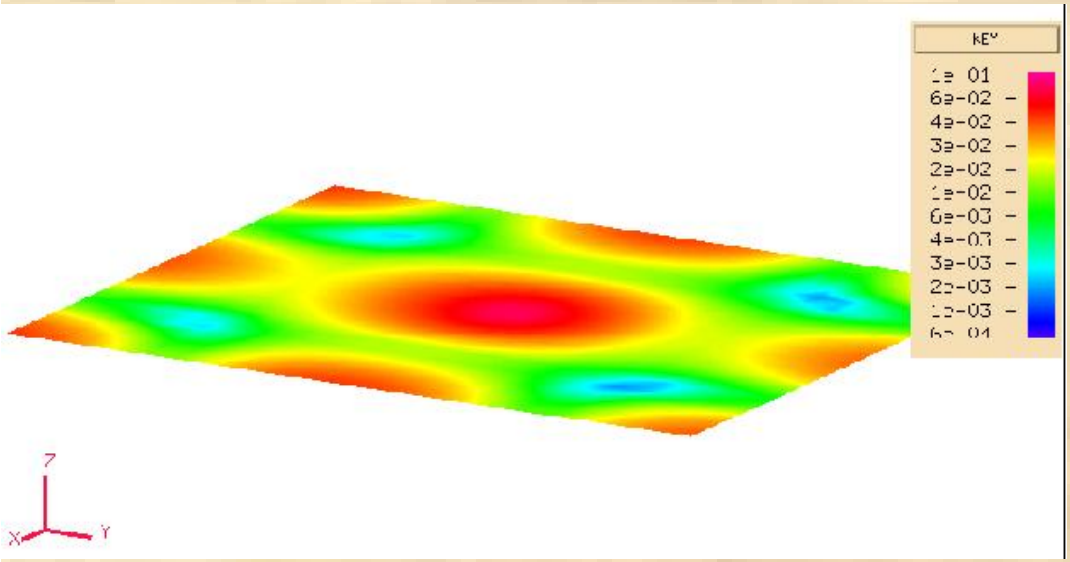
Voltage Distribution @ 750 MHz .01uF and 330pF Case (Source in Center)

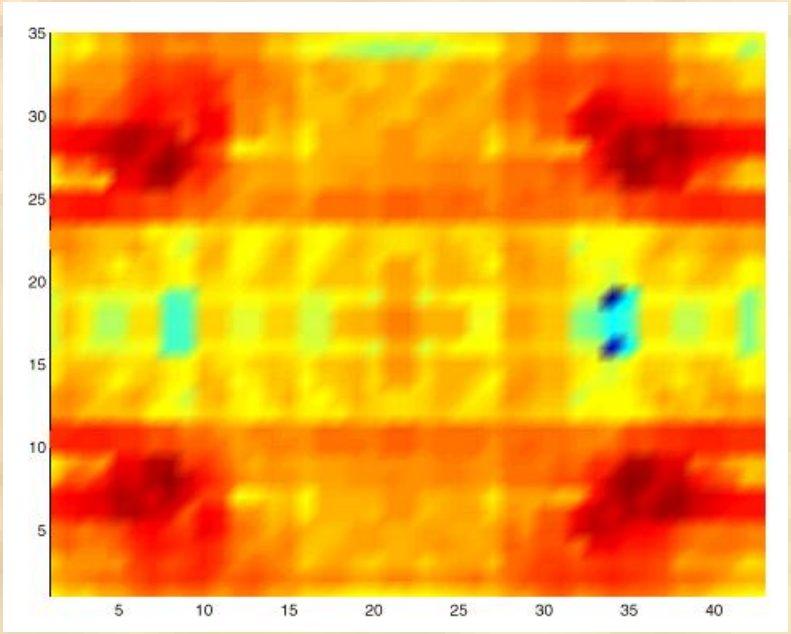


Voltage Distribution @ 950 MHz
.01uF and 330pF Case (Source in Center)



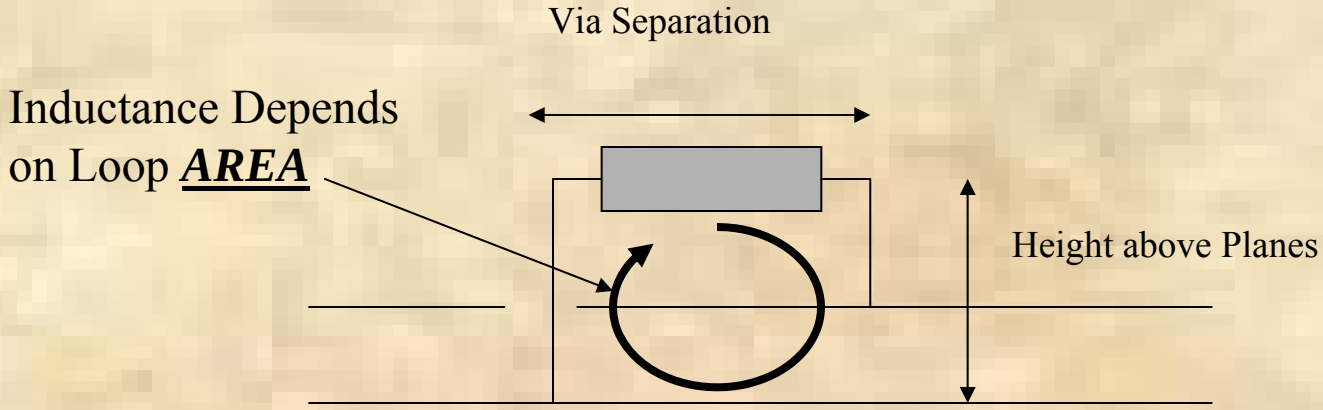
Voltage and Gradient
99 caps @ 800 MHz





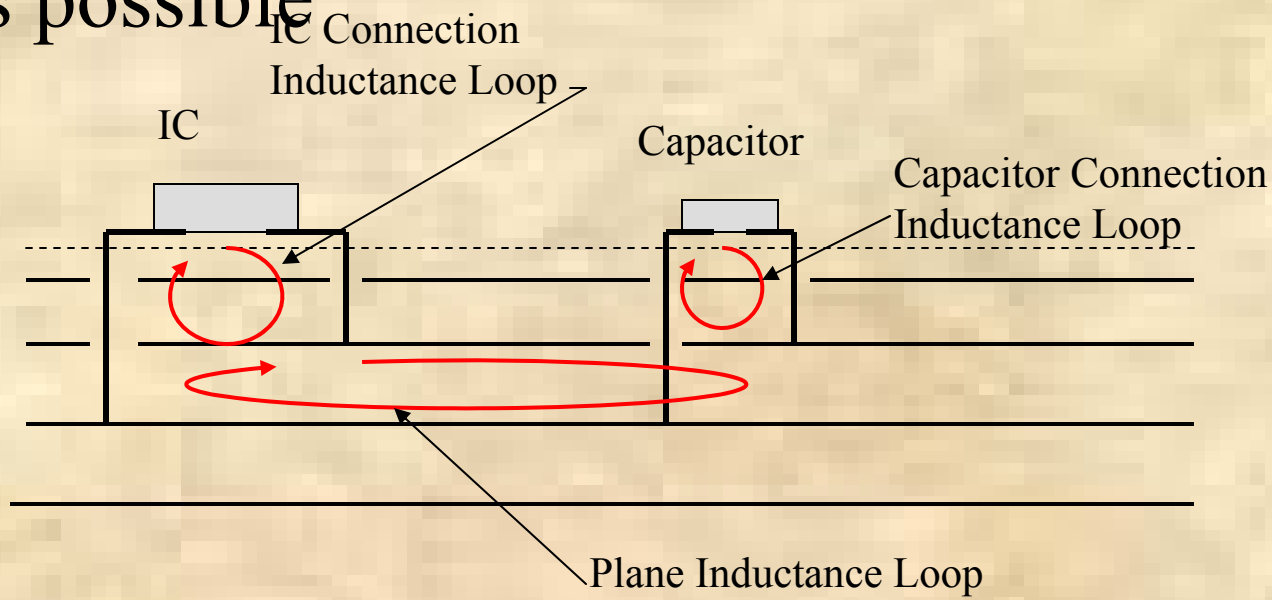
Decoupling Capacitor Mounting

- Keep as to planes as close to capacitor pads as possible

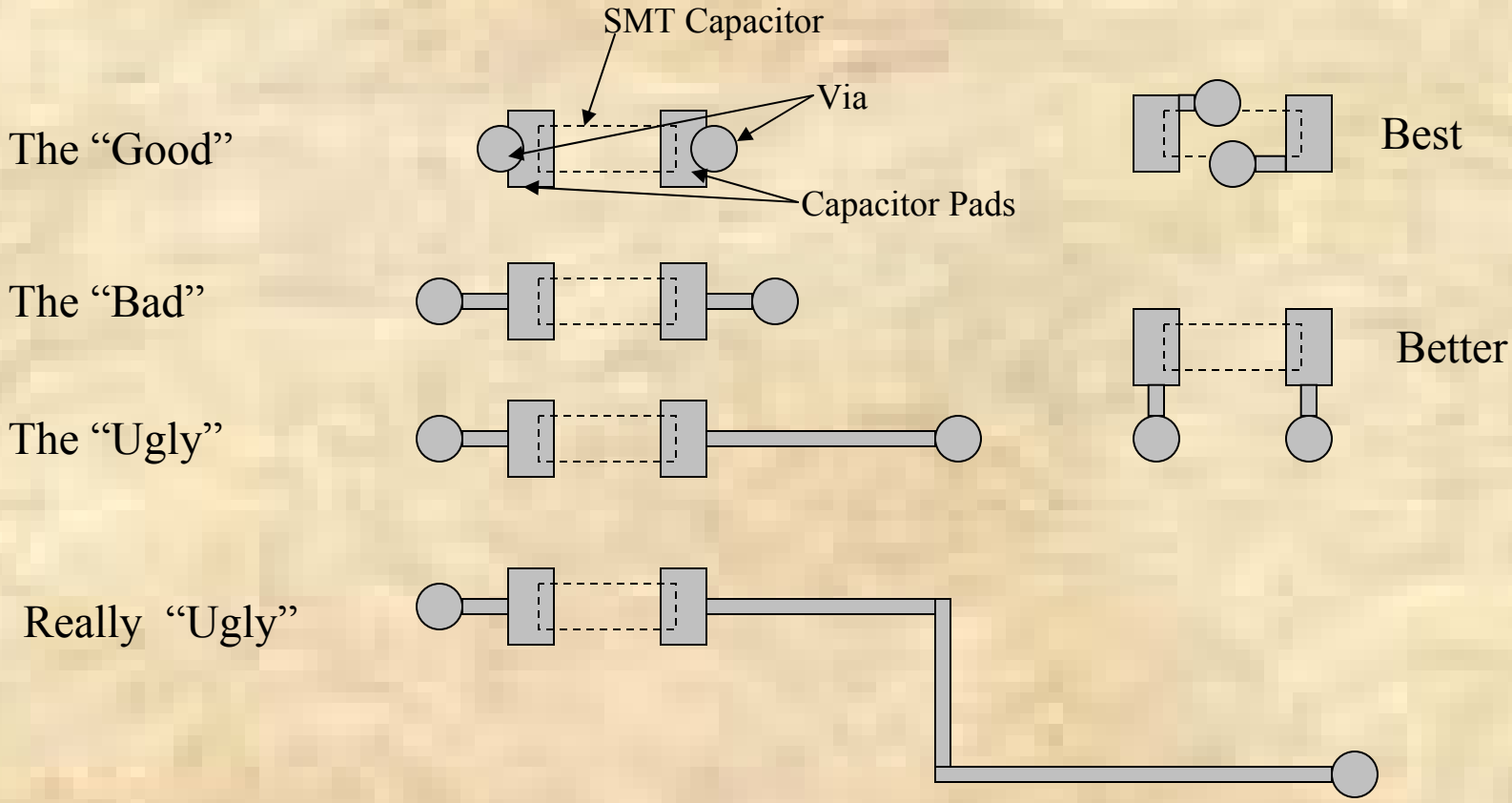


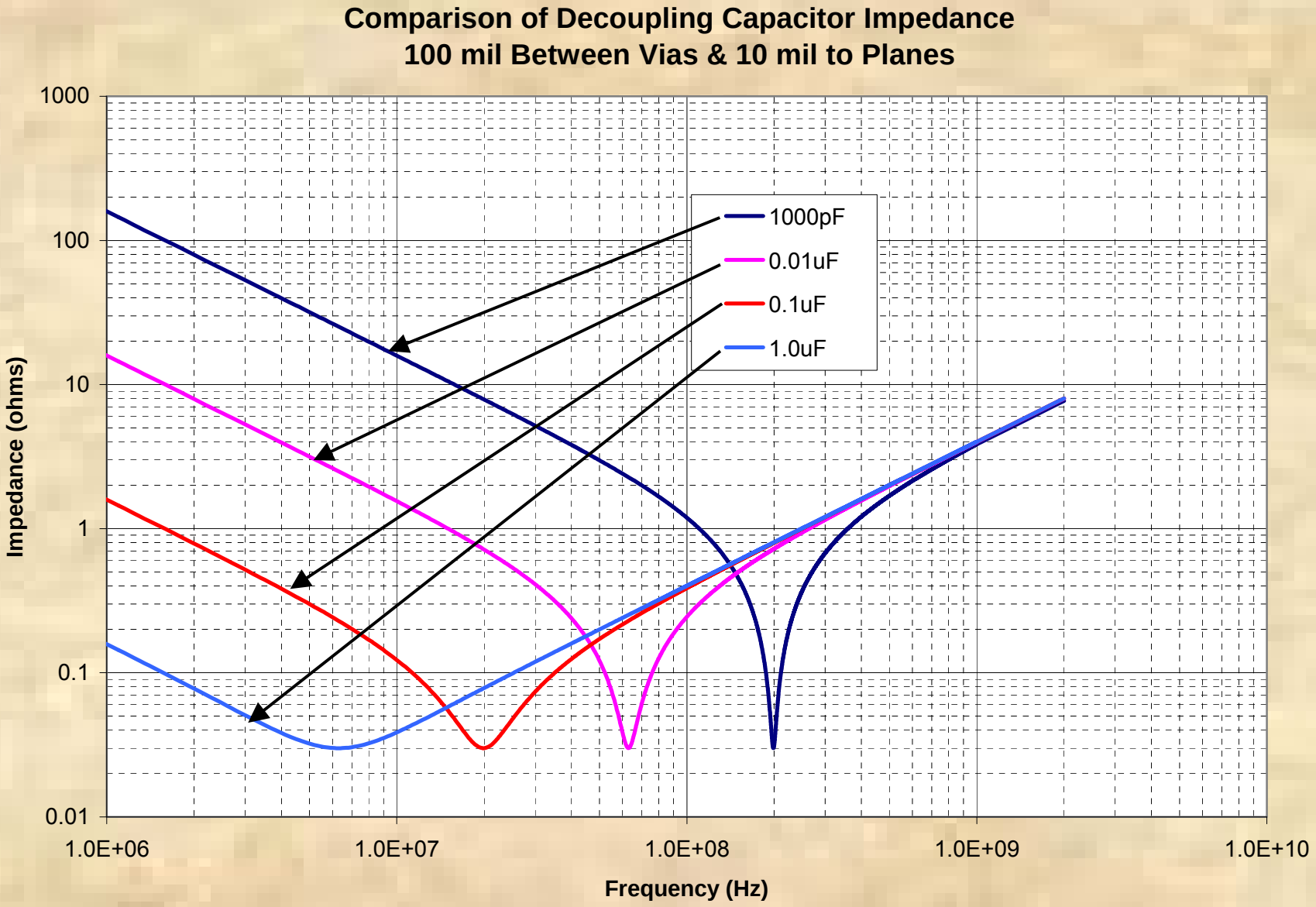
Decoupling Capacitor Mounting

- Keep as to planes as close to capacitor pads as possible

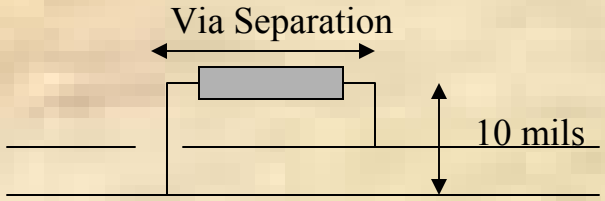


Via Configuration Can Change Inductance




Comparison of Decoupling Capacitor Impedance
100 mil Between Vias & 10 mil to Planes
1000
100
10
1
0.1
0.01
Impedance (ohms)
1000pF
0.01uF
0.1uF
1.0uF
1.0E+06
1.0E+07
1.0E+08
1.0E+09
1.0E+10
Frequency (Hz)

Comparison of Decoupling Capacitor Via Separation Distance Effects



0.1 uF Capacitor

Via Seperation (mils)	Inductance (nH)	Impedance @ 1 GHz (ohms)
20	.06	.41
40	0.21	1.3
60	0.36	2.33
80	0.5	3.1
100	0.64	4.0
150	1.0	6.23
200	1.4	8.5
300	2.1	12.69
400	2.75	17.3
500	3.5	21.7

Example Connection Inductance Values

Spacing between Vias	Complex Formula (20 mils to plane)	Simple rect loop (20 mils to plane)	Complex Formula (10 mils to plane)	Simple rect loop (10 mils to plane)
0805 + 2*10mil	3.0 nH	3.1 nH	2 nH	1.38 nH
0805 + 2*100mil	4.1 nH	4.3 nH	3 nH	2.0 nH
0805 + 2*160mil	5.1 nH	5.1 nH	3.5 nH	2.5 nH
0603 + 2*10mil	2.3 nH	1.74 nH	1.1 nH	0.8 nH
0603 + 2*100mil	3.3 nH	3.15 nH	2.1 nH	1.5 nH
0603 + 2*160mil	4.2 nH	4.3 nH	2.4 nH	2.07 nH

Sources for complex formula:

Knighten, James L., Bruce Archambeault, Jun Fan, Samuel Connor, James L. Drewniak, "PDN Design Strategies: II. Ceramic SMT Decoupling Capacitors – Does Location Matter?," *IEEE EMC Society Newsletter*, Issue No. x, Winter 2006, pp. 56-67. (www.emcs.org)

Fan, Jun, Wei Cui, James L. Drewniak, Thomas Van Doren, and James L. Knighten, "Estimating the Noise Mitigating Effect of Local Decoupling in Printed Circuit Boards," *IEEE Trans. on Advanced Packaging*, Vol. 25, No. 2, May 2002, pp. 154-165

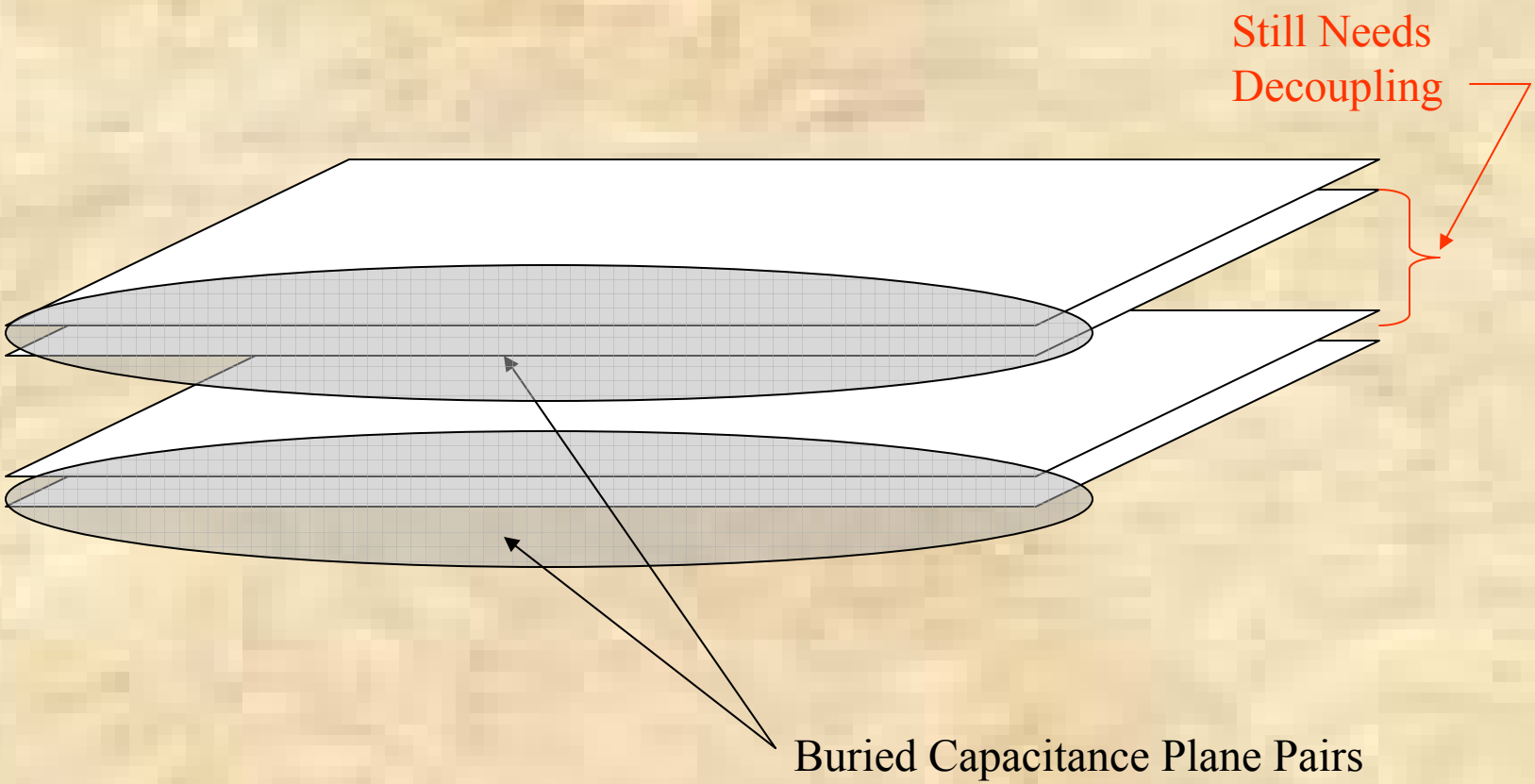
Other Design Possibilities

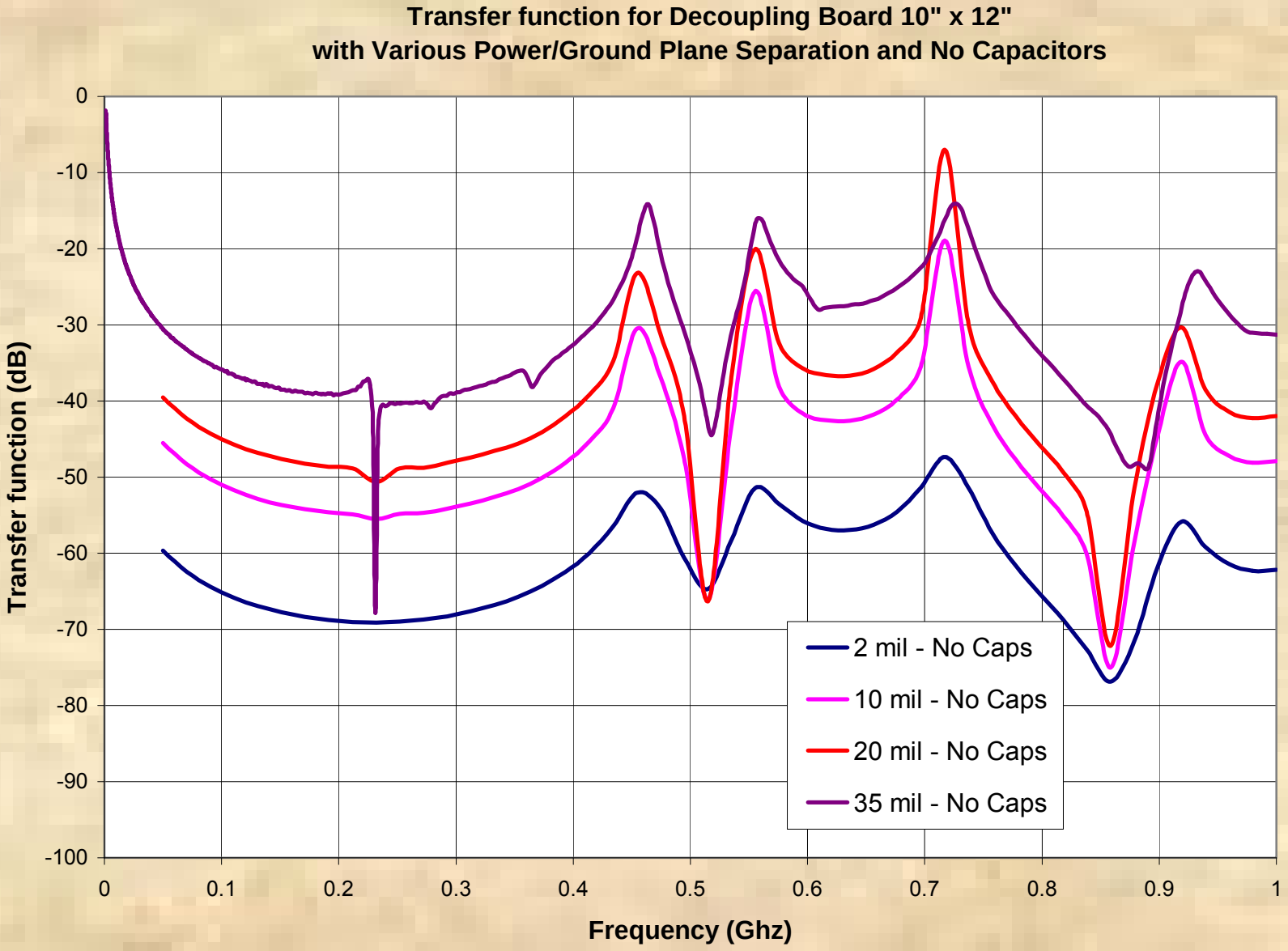
- So-called Buried Capacitance
  - Reduces high frequency transfer function
  - Allows less capacitors to be used
  - Really should be called ‘increased distributed capacitance’
- Lossy decoupling
  - Reduces high frequency transfer function
  - Allows less capacitors to be used

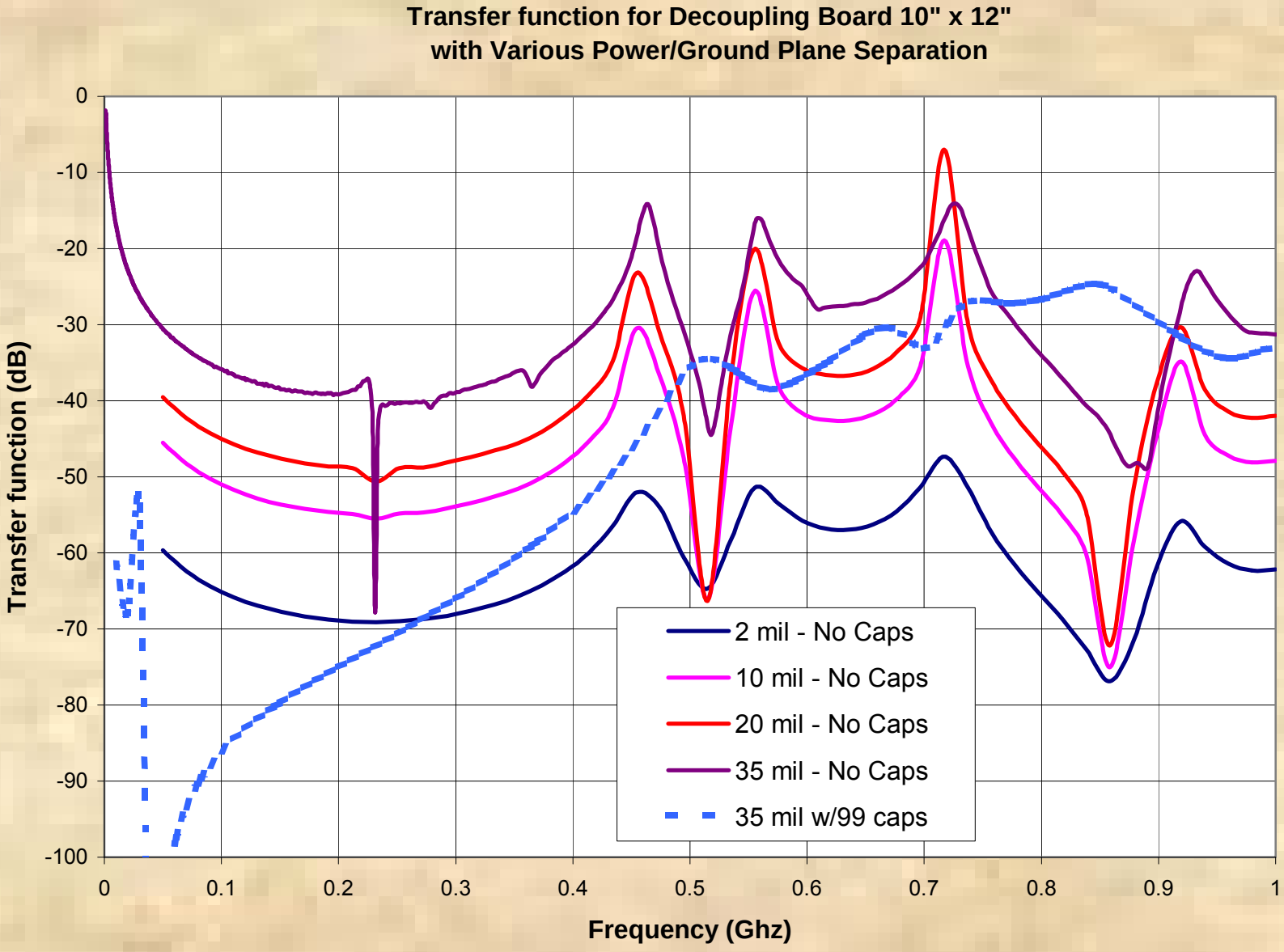
Buried Capacitance

- Planes very close together (2 mils)
- Only effective for the power/ground plane pair !!!
- Other sets of Planes must still be decoupled the traditional way

Buried Capacitance ***ONLY*** Applies to Plane Pairs




Transfer function for Decoupling Board 10" x 12"
with Various Power/Ground Plane Separation and No Capacitors
Transfer function (dB)
0
-10
-20
-30
-40
-50
-60
-70
-80
-90
-100
0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1
Frequency (Ghz)
2 mil - No Caps
10 mil - No Caps
20 mil - No Caps
35 mil - No Caps

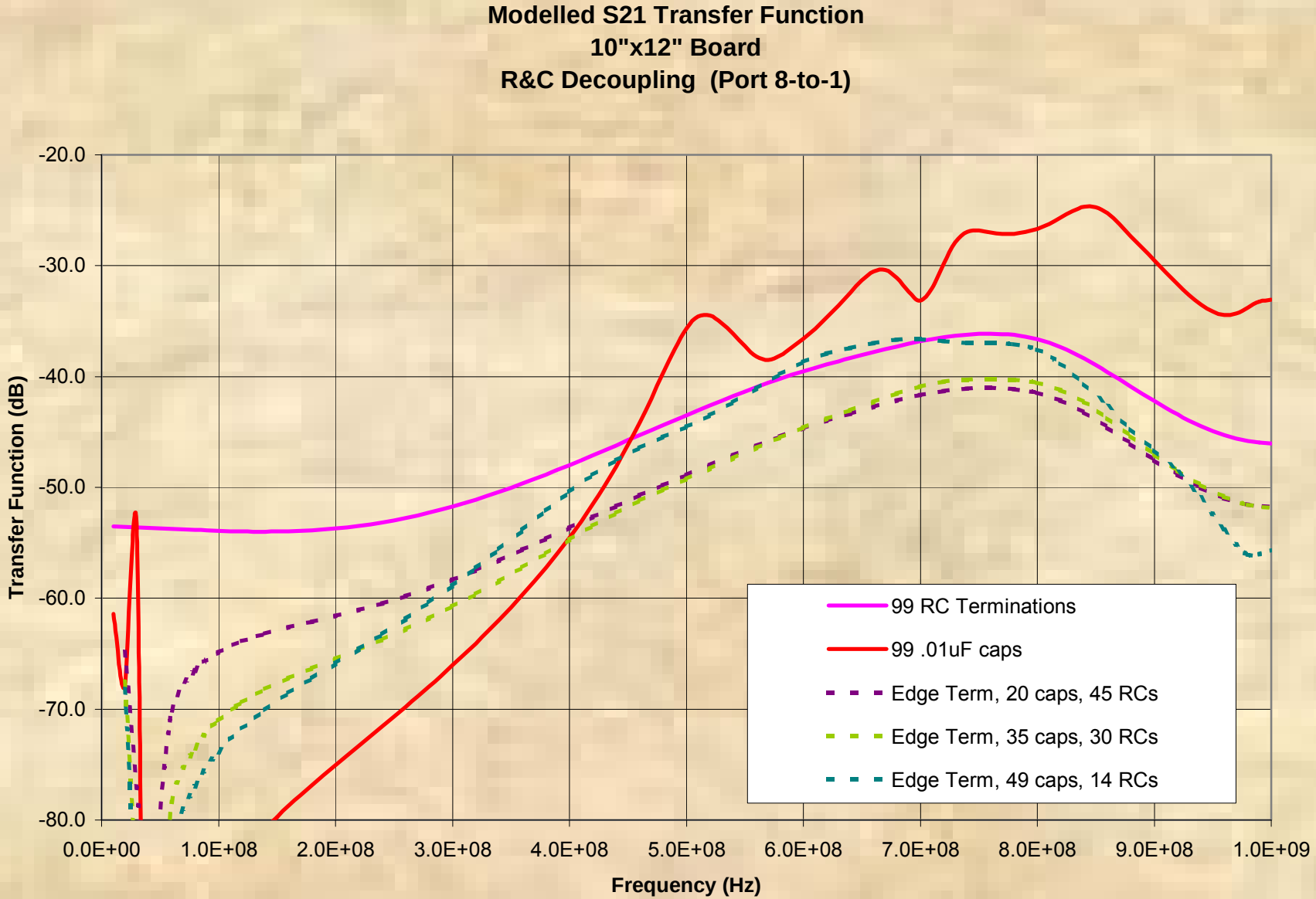

Transfer function for Decoupling Board 10" x 12"
with Various Power/Ground Plane Separation
Transfer function (dB)
0
-10
-20
-30
-40
-50
-60
-70
-80
-90
-100
0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1
Frequency (Ghz)
2 mil - No Caps
10 mil - No Caps
20 mil - No Caps
35 mil - No Caps
35 mil w/99 caps

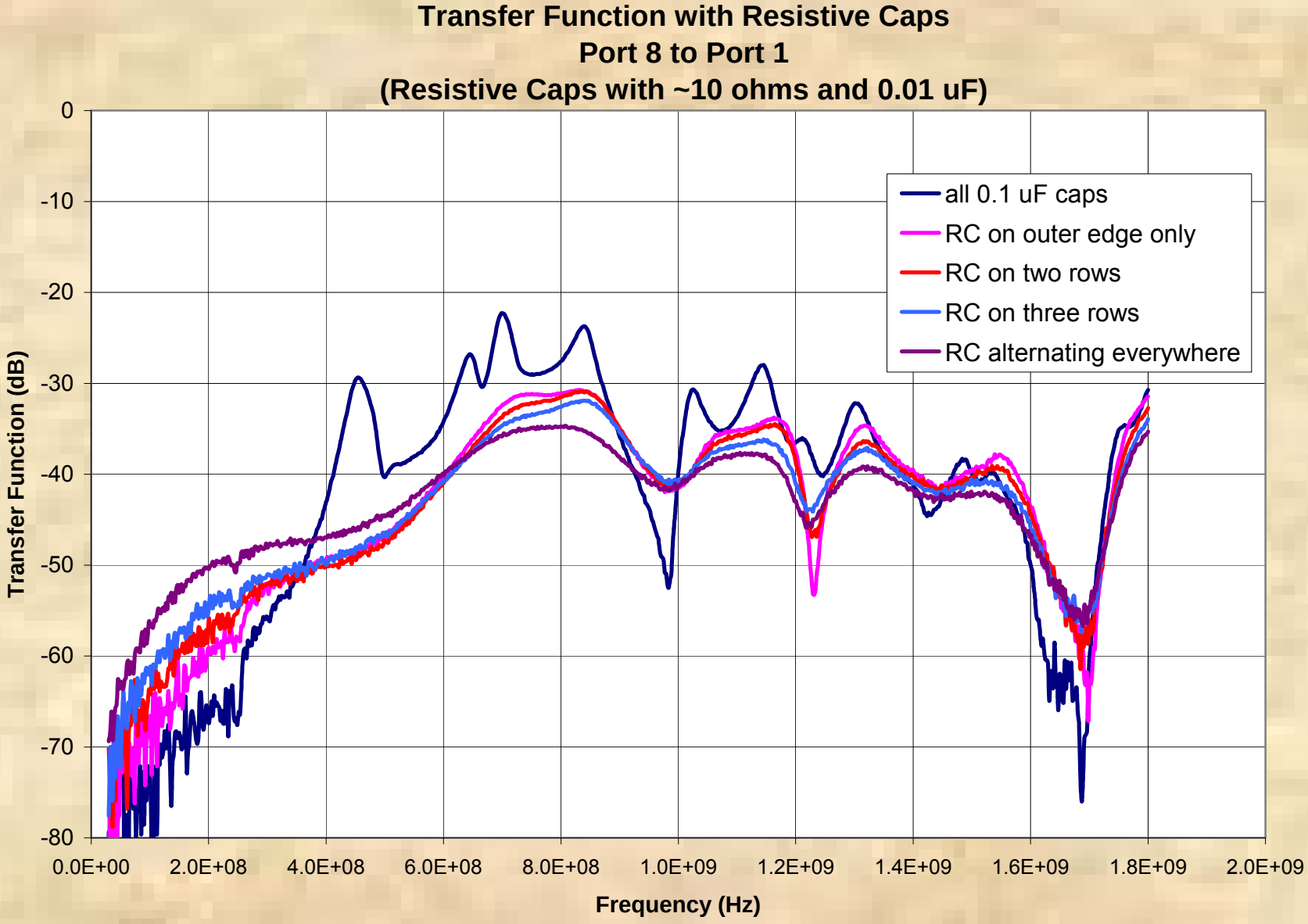
Lossy Decoupling

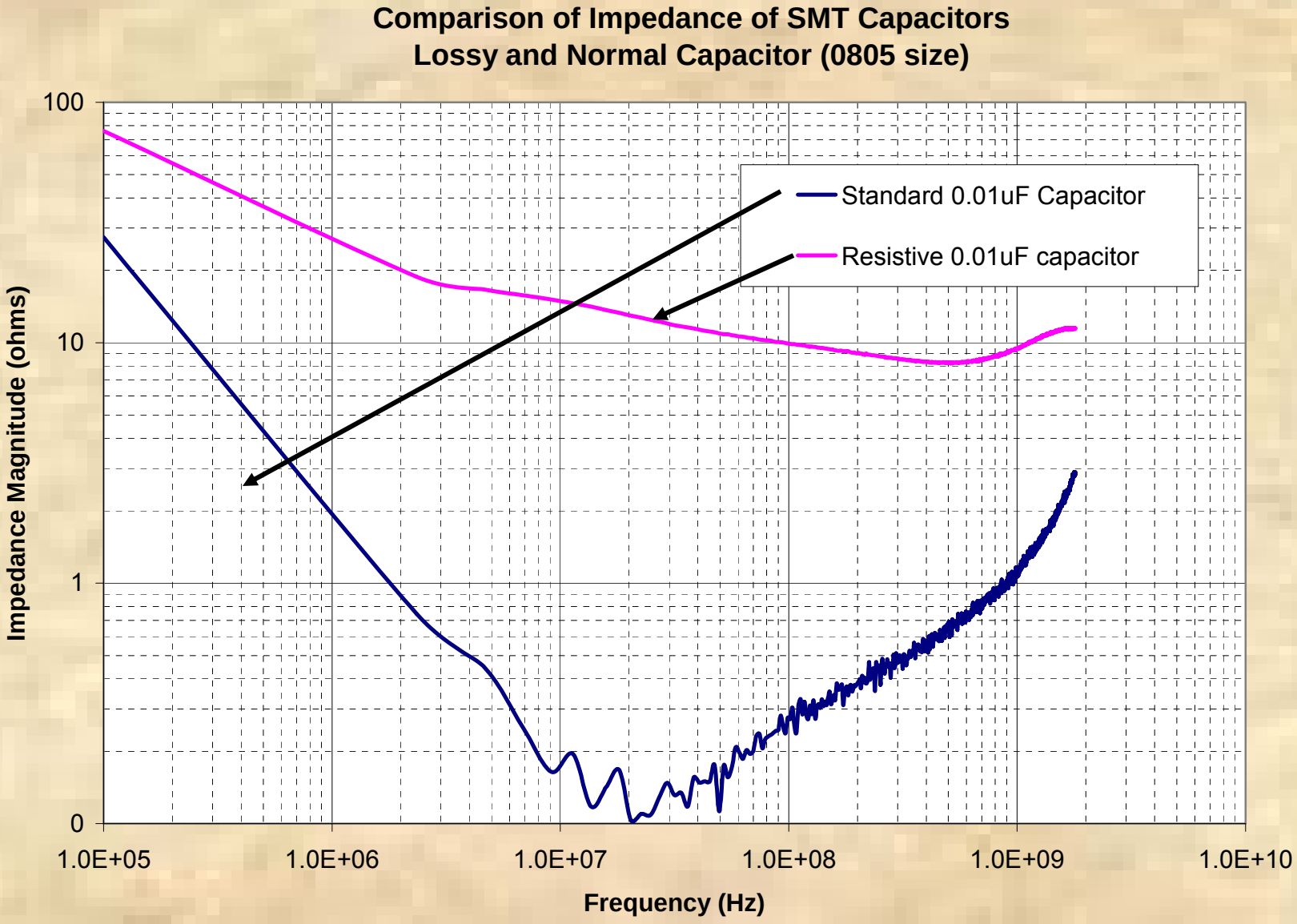
- New technique
- Series resistance and capacitance in same SMT package
- Need to use both low ESR capacitors and lossy capacitors
  - fewer total parts

Cause of Failure above 400 - 500 MHz?

- Inductance is limiting factor for capacitors
- Board size cause resonances which causes problems
- Need to reduce resonance effects by lowering Q-factor
  - add resistive loss


Modelled S21 Transfer Function
10"x12" Board
R&C Decoupling (Port 8-to-1)
Transfer Function (dB)
-20.0
-30.0
-40.0
-50.0
-60.0
-70.0
-80.0
0.0E+00
1.0E+08
2.0E+08
3.0E+08
4.0E+08
5.0E+08
6.0E+08
7.0E+08
8.0E+08
9.0E+08
1.0E+09
Frequency (Hz)
99 RC Terminations
99 .01uF caps
Edge Term, 20 caps, 45 RCs
Edge Term, 35 caps, 30 RCs
Edge Term, 49 caps, 14 RCs

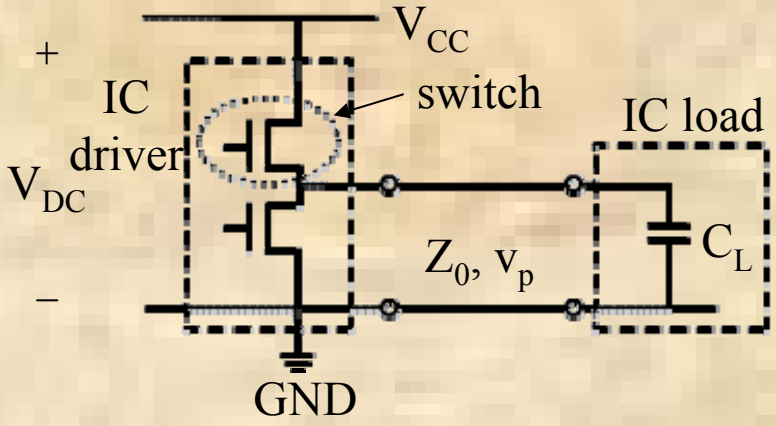

Transfer Function with Resistive Caps
Port 8 to Port 1
(Resistive Caps with ~10 ohms and 0.01 uF)
Transfer Function (dB)
0
-10
-20
-30
-40
-50
-60
-70
-80
0.0E+00
2.0E+08
4.0E+08
6.0E+08
8.0E+08
1.0E+09
1.2E+09
1.4E+09
1.6E+09
1.8E+09
2.0E+09
Frequency (Hz)
all 0.1 uF caps
RC on outer edge only
RC on two rows
RC on three rows
RC alternating everywhere

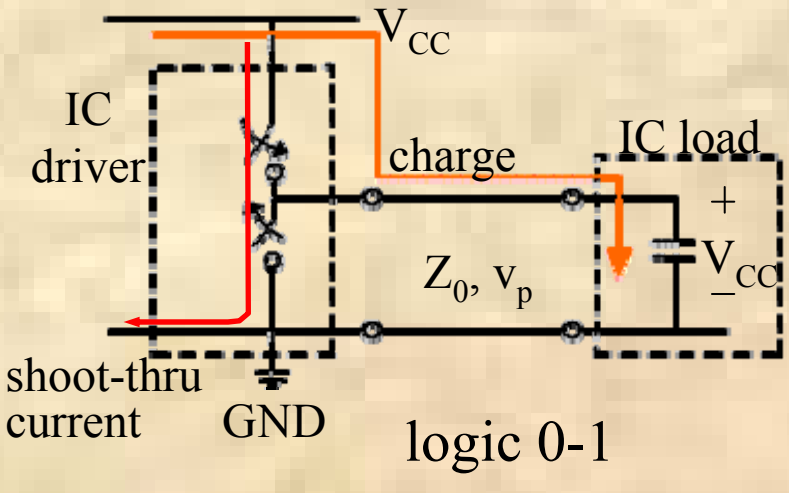

Comparison of Impedance of SMT Capacitors
Lossy and Normal Capacitor (0805 size)
Impedance Magnitude (ohms)
100
10
1
0
1.0E+05
1.0E+06
1.0E+07
1.0E+08
1.0E+09
1.0E+10
Frequency (Hz)
Standard 0.01uF Capacitor
Resistive 0.01uF capacitor

Transient Analysis
(Time Limited)

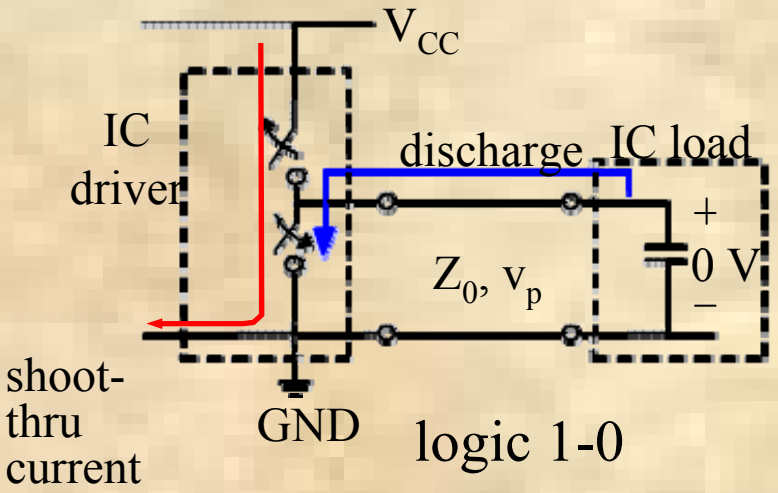
- Provide charge to ASIC/IC
- Inductance dominates impedance
  - Loop area 1st order effect
- Traditional analysis not accurate enough

Current in IC During Logic Transitions (CMOS)



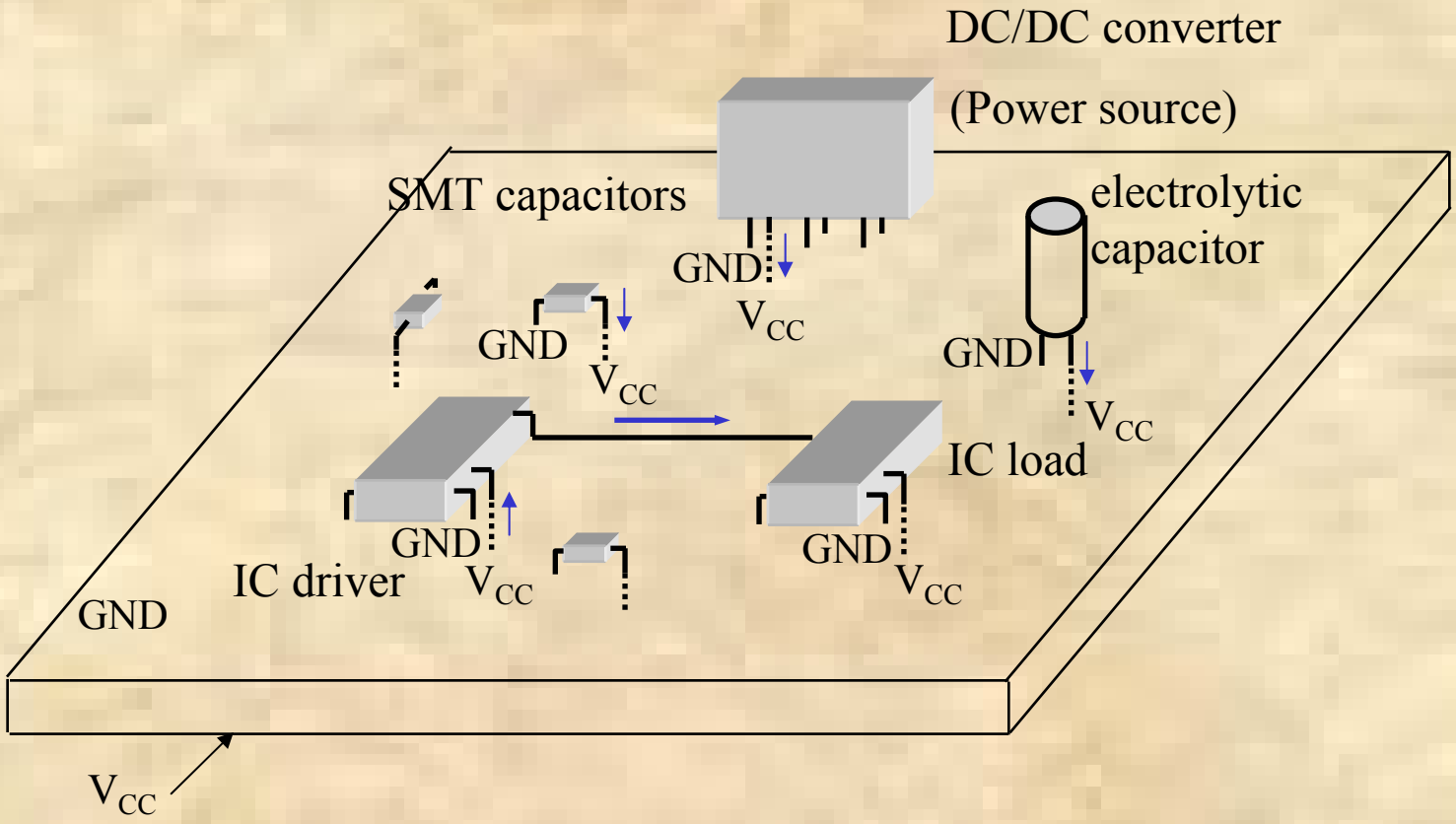


logic 0-1

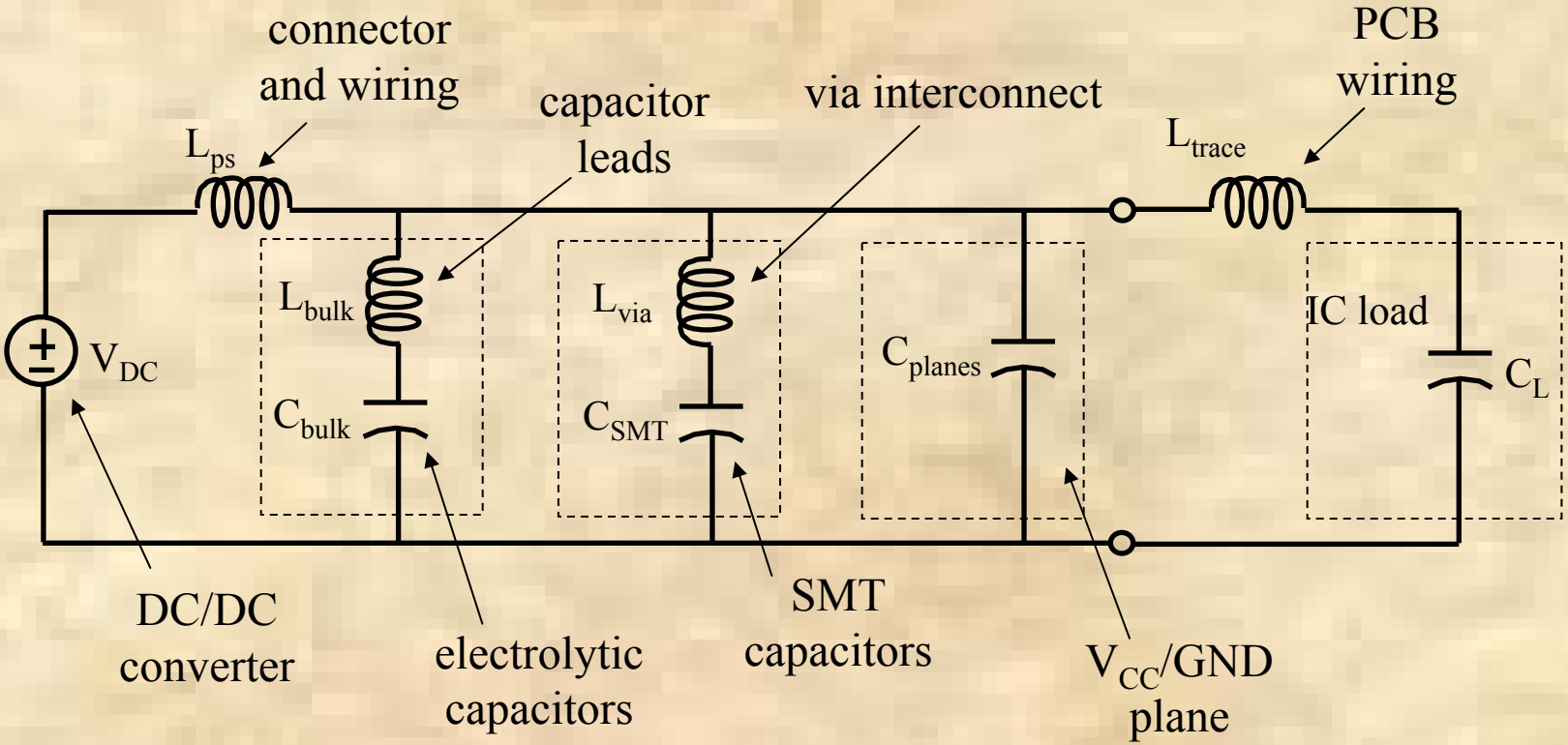


logic 1-0

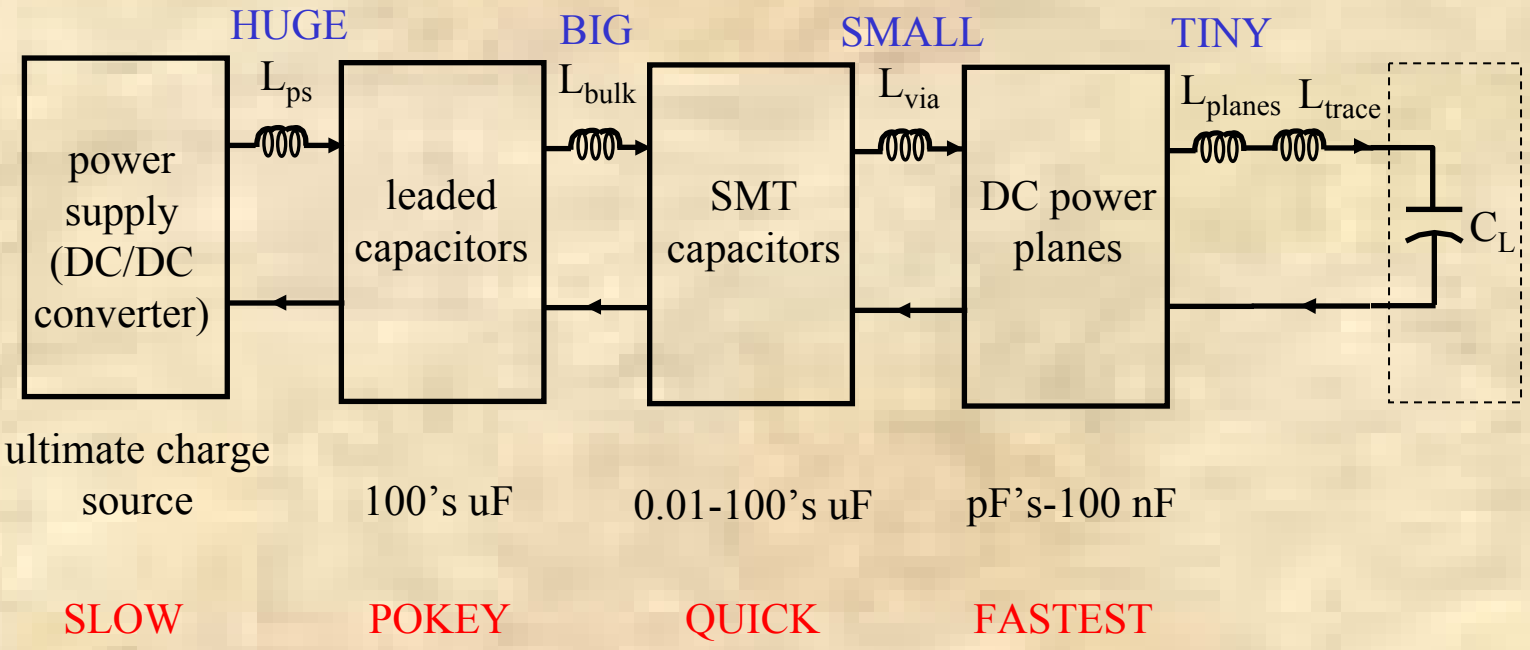
Typical PCB Power Delivery



Equivalent Circuit for Power Current Delivery to IC

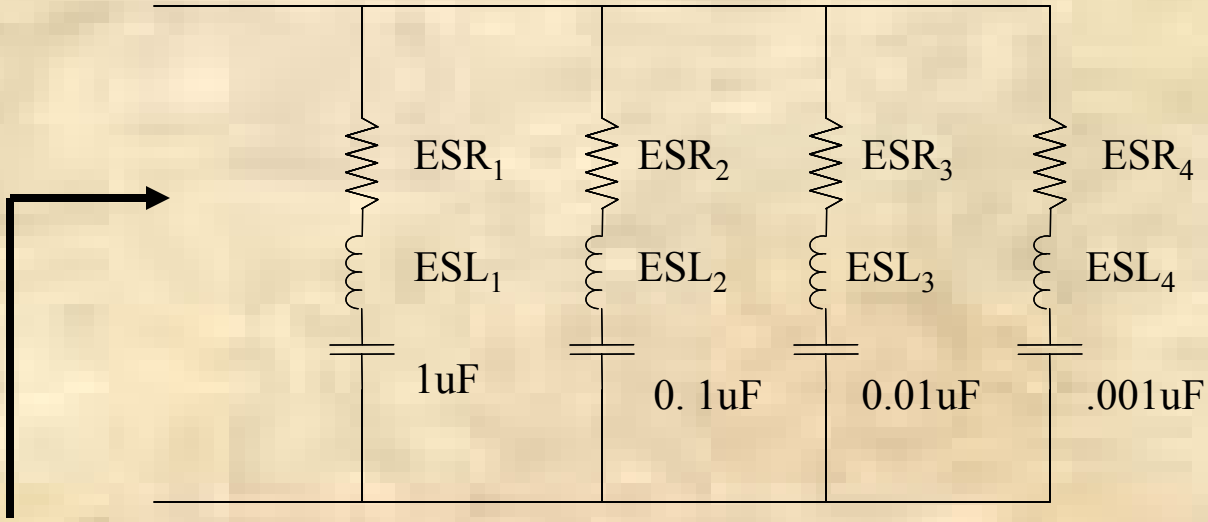


Power Bus Charging Hierarchy



Traditional Analysis #1

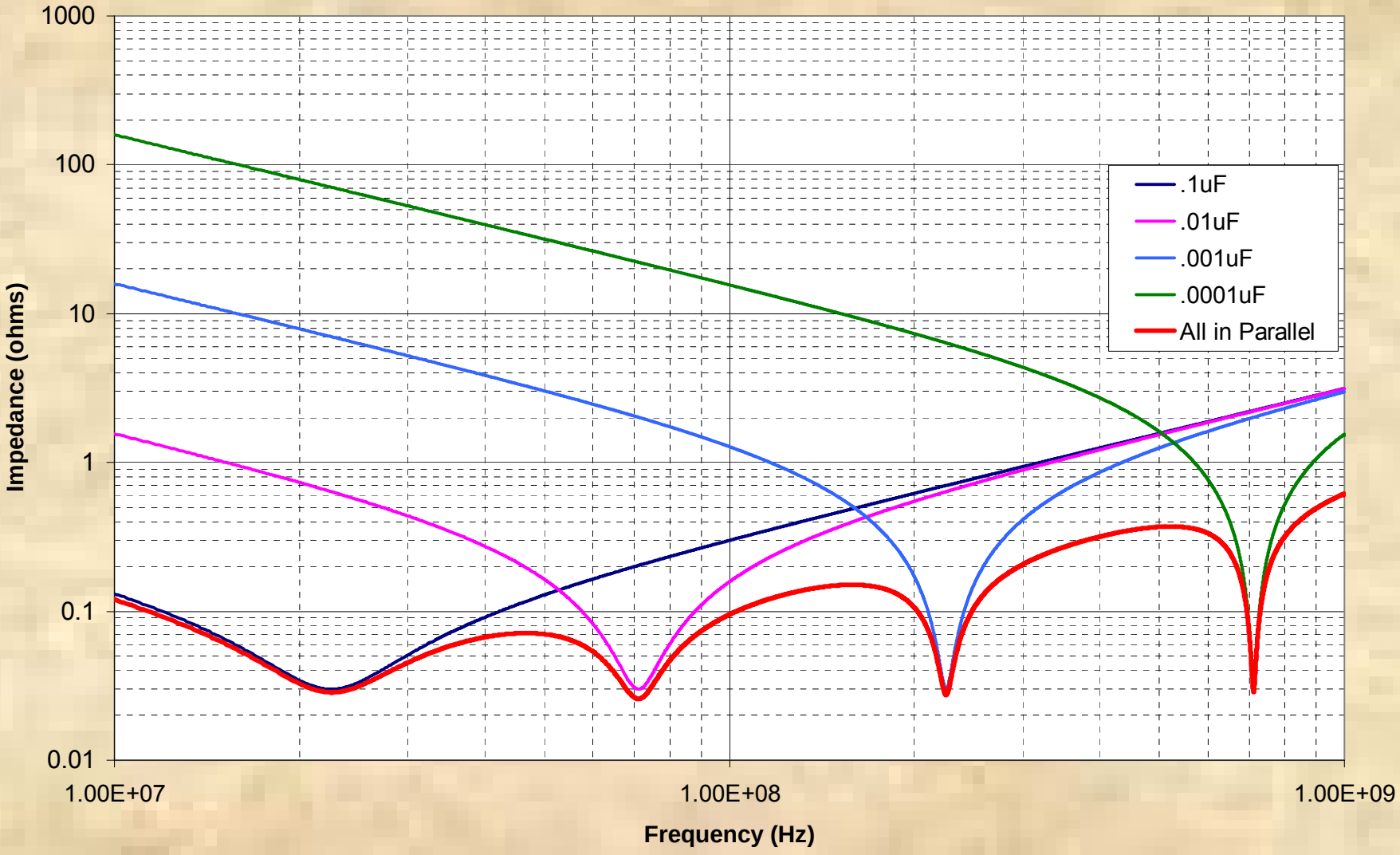
- Use impedance of capacitors in parallel



Impedance to IC power/gnd pins

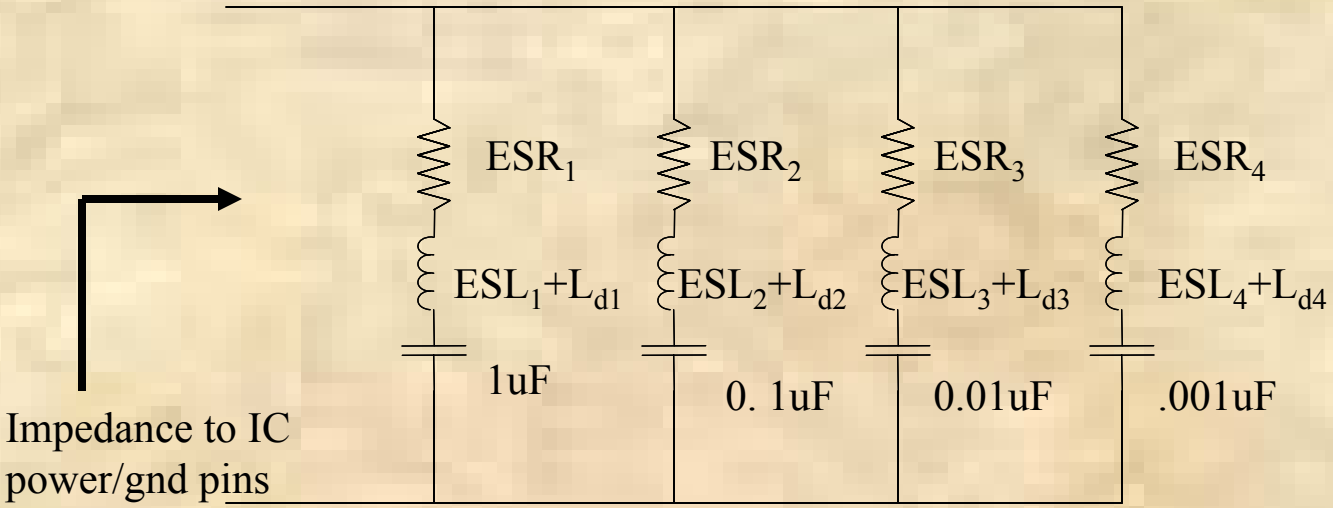
No Effect of Distance Between Capacitors and IC Included!

Traditional Impedance Calculation for Four Decoupling Capacitor Values



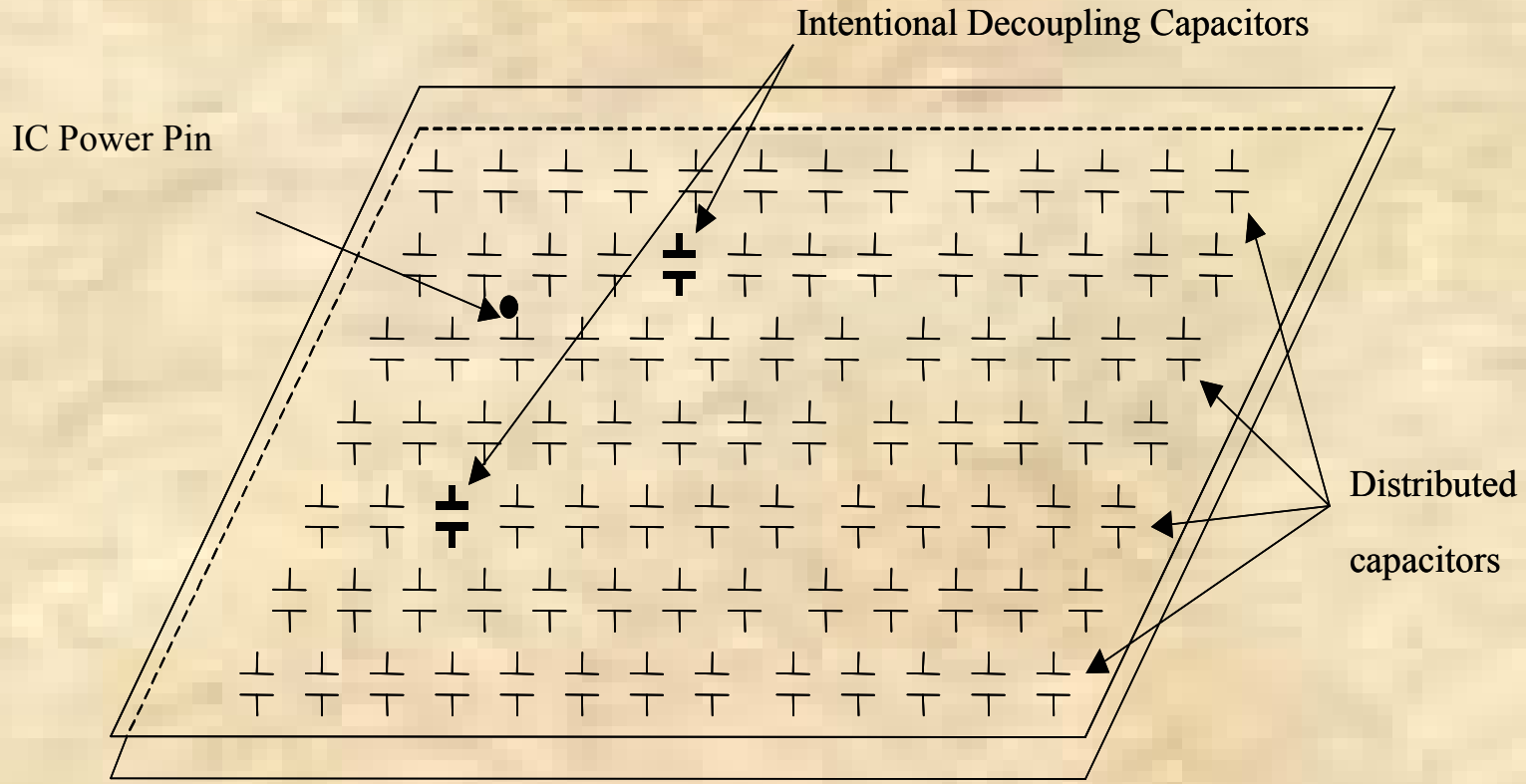
Traditional Analysis #2

- Calculate loop area – Traditional loop Inductance formulas
  - Which loop area? Which size conductor

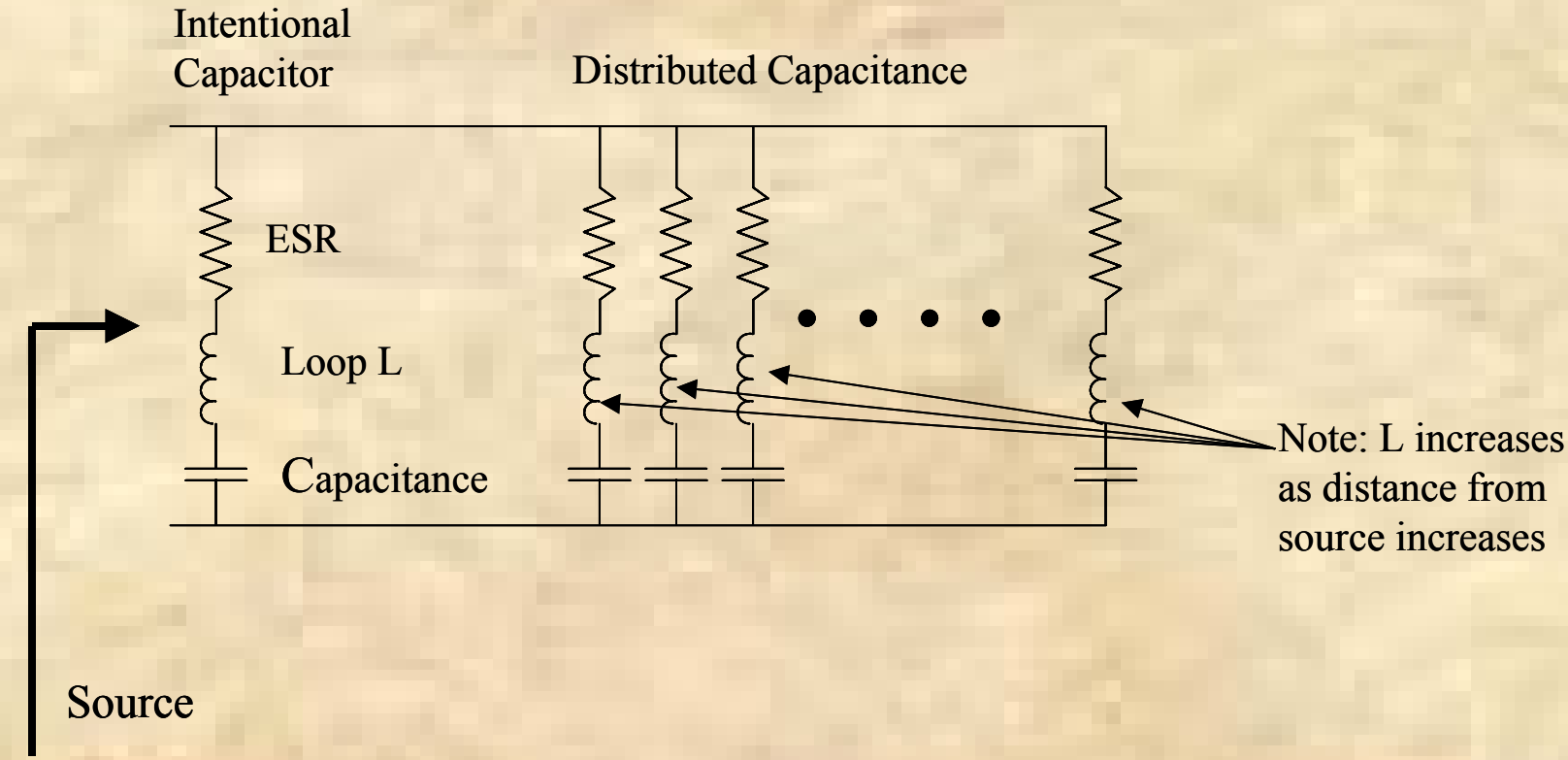


Over Estimates L and Ignores Distributed Capacitance

More Accurate Model Includes Distributed Capacitance



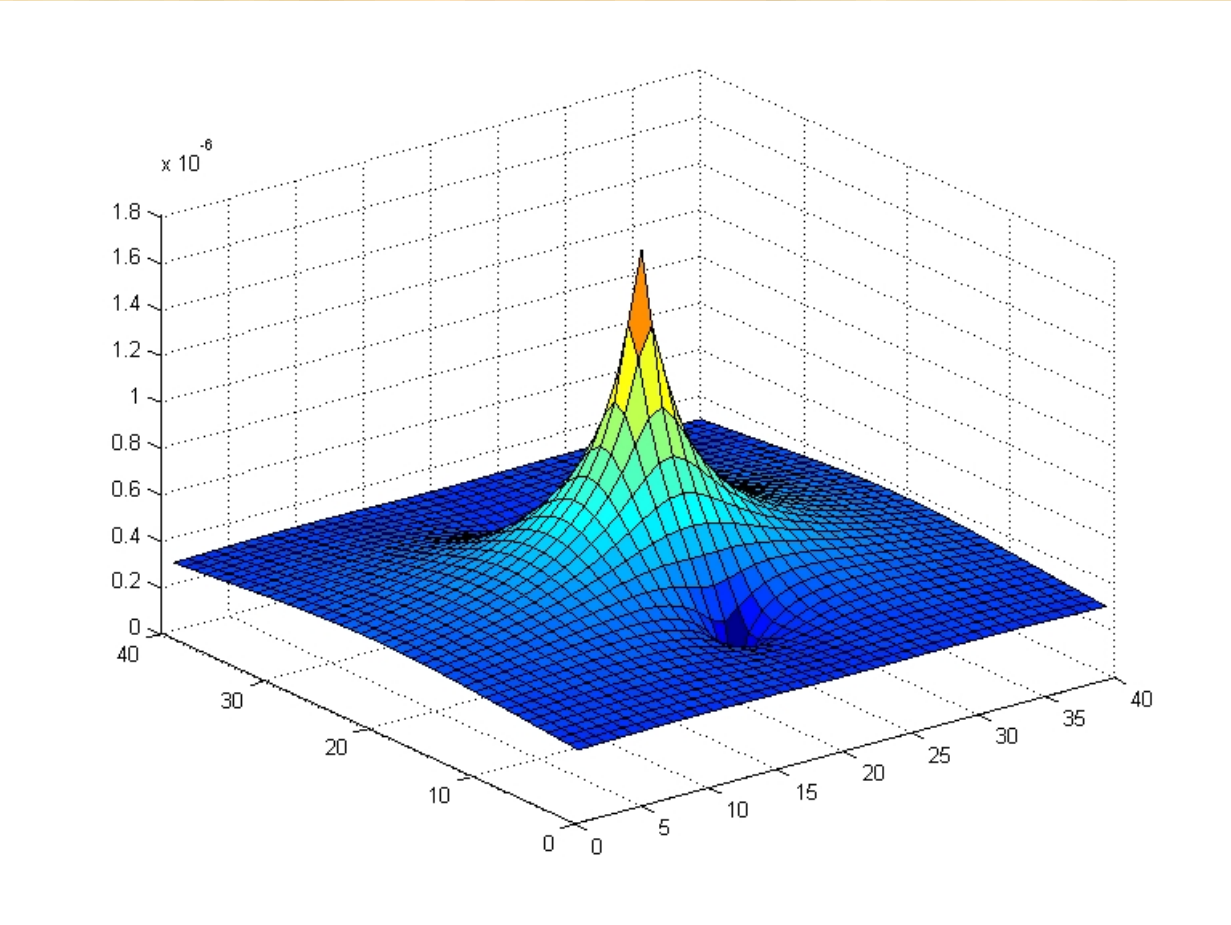
Distributed Capacitance Schematic



Effect of Distributed Capacitance

- Can NOT be calculated/estimated using traditional capacitance equation
- Displacement current amplitude changes with position and distance from the source

Displacement Current
500 MHz via @450 mils from Source



Need to Find the Real Effect of Decoupling Capacitor Distance

- Perfect decoupling capacitor is a via between planes
- FDTD simulation to find the effect of shorting via distance from source
- Vary spacing between planes, distance to via, frequency, etc

Impedance Result

- Linear with frequency (on log scale)
- Looks like an inductance only!
- Consider this inductance an **Apparent Inductance**
- Apparent inductance is constant with frequency

Formulas to Predict Apparent Inductance

$$L_{one-via} = (0.1336s - 0.0654)Ln(dist) + (-0.2609s + 0.2675)$$

$$L_{two-via} = (0.1307s - 0.0492)Ln(dist) + (-0.2948s + 0.1943)$$

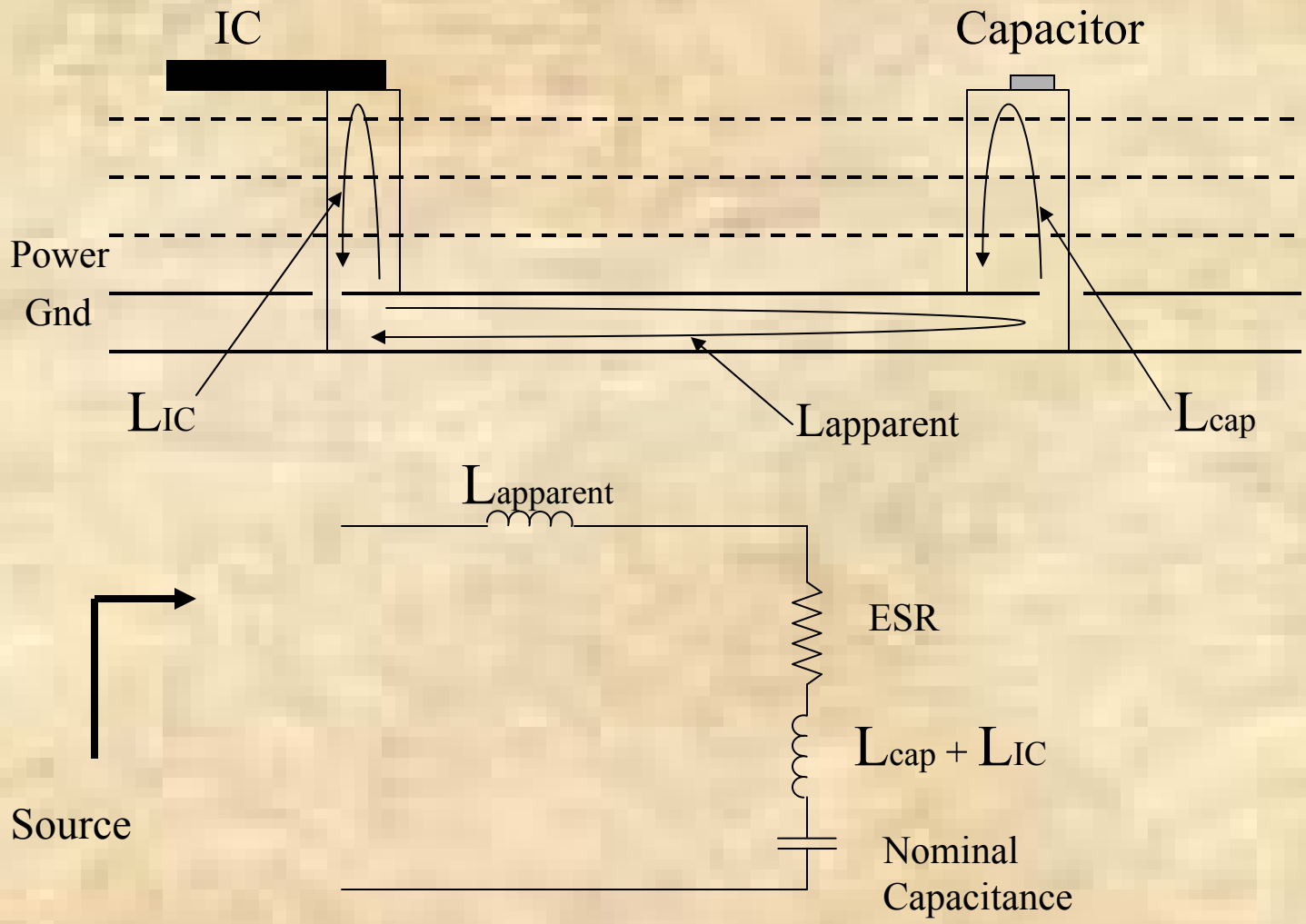
$$L_{three-via} = (0.1242s - 0.0447)Ln(dist) + (-0.2848s + 0.1763)$$

$$L_{four-via} = (0.1192s - 0.0403)Ln(dist) + (-0.2774s + 0.1592)$$

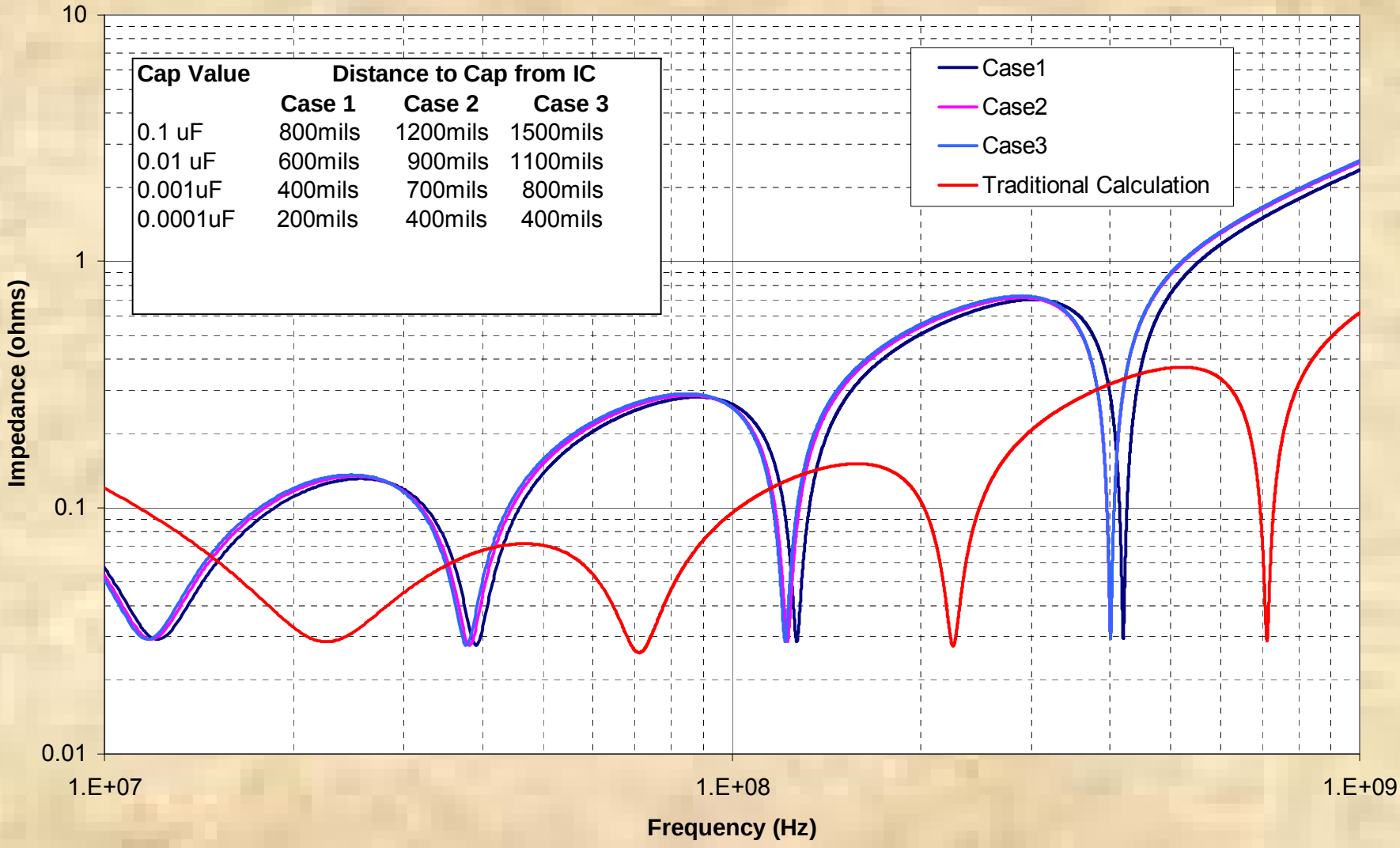
s = separation between plates (mils/10)

$dist$ = distance to via

True Impedance for Decoupling Capacitor



Impedance Calculation with Apparent Inductance for Four Decoupling Capacitor Values

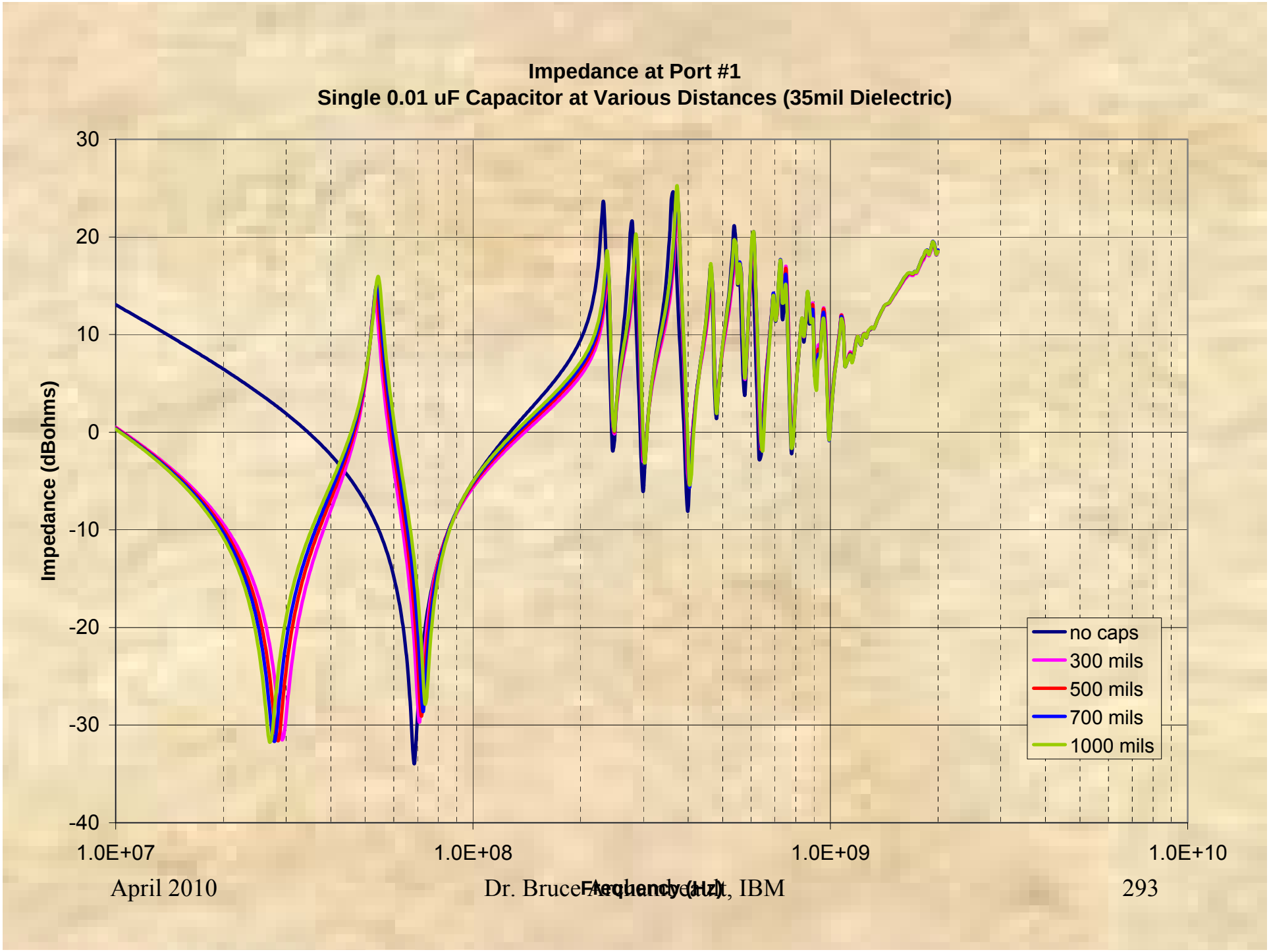


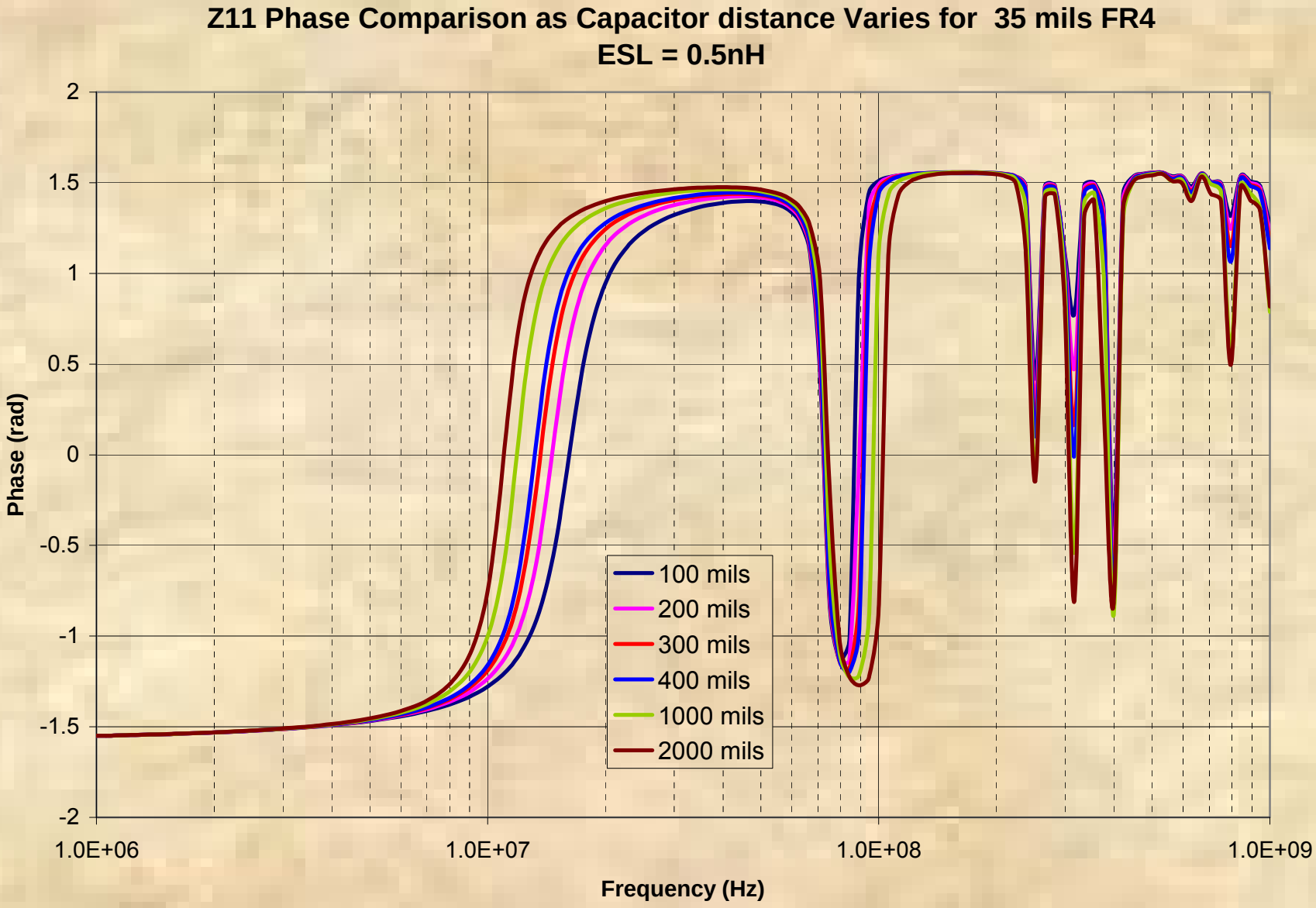
Effect of Distributed Capacitance

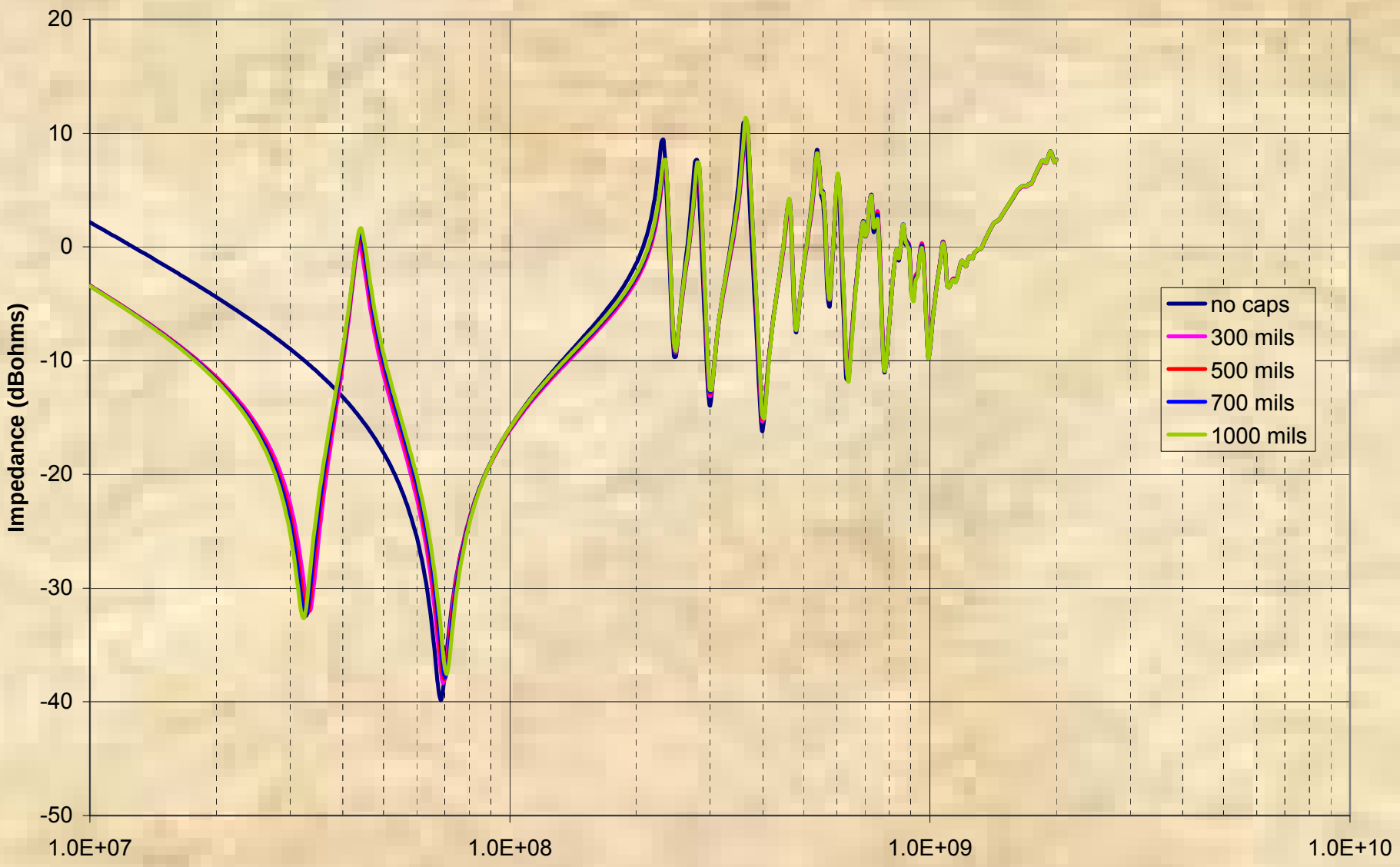
- Can NOT be calculated/estimated using traditional capacitance equation
- Displacement current amplitude changes with position and distance from the source
- Following examples use cavity resonance technique (EZ-PowerPlane)
  - Frequency Domain to compare to measurements
  - Time Domain using SPICE circuit from cavity resonance analysis

Parameters for Comparison to Measurements

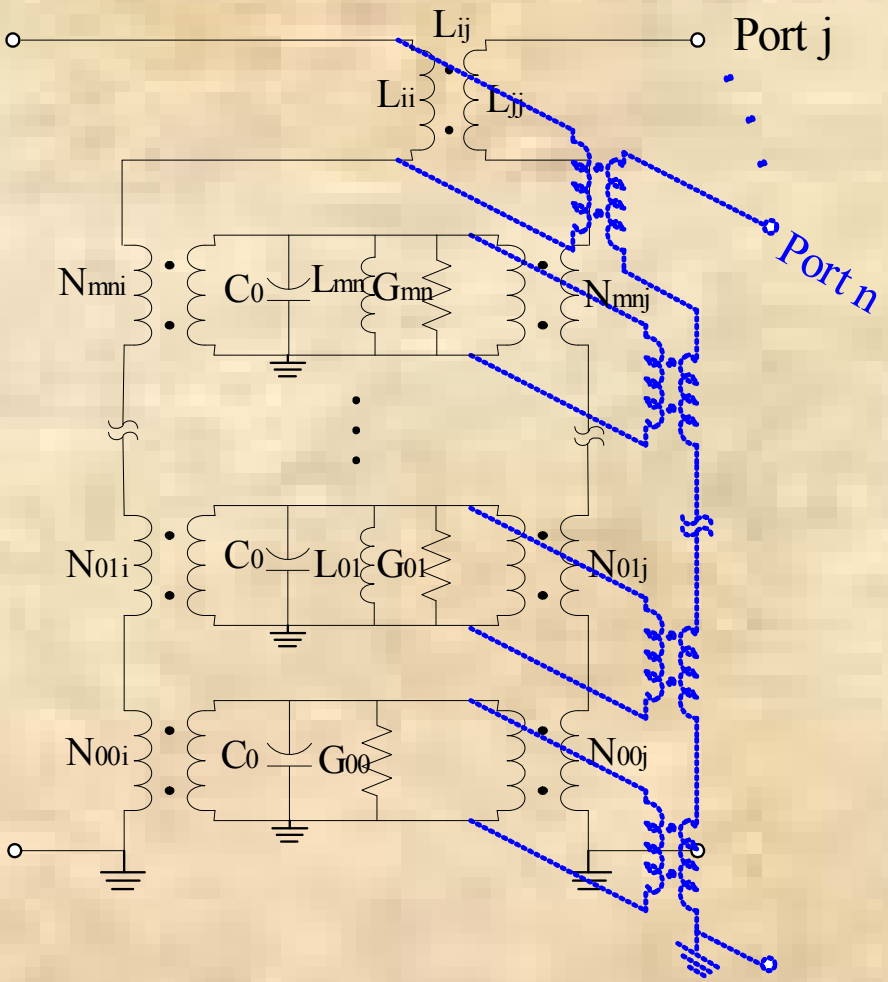
- Dielectric thickness = 35 mils
- Dielectric constant = 4.5, Loss tan = 0.02
- Copper conductivity = 5.8 e7 S/m

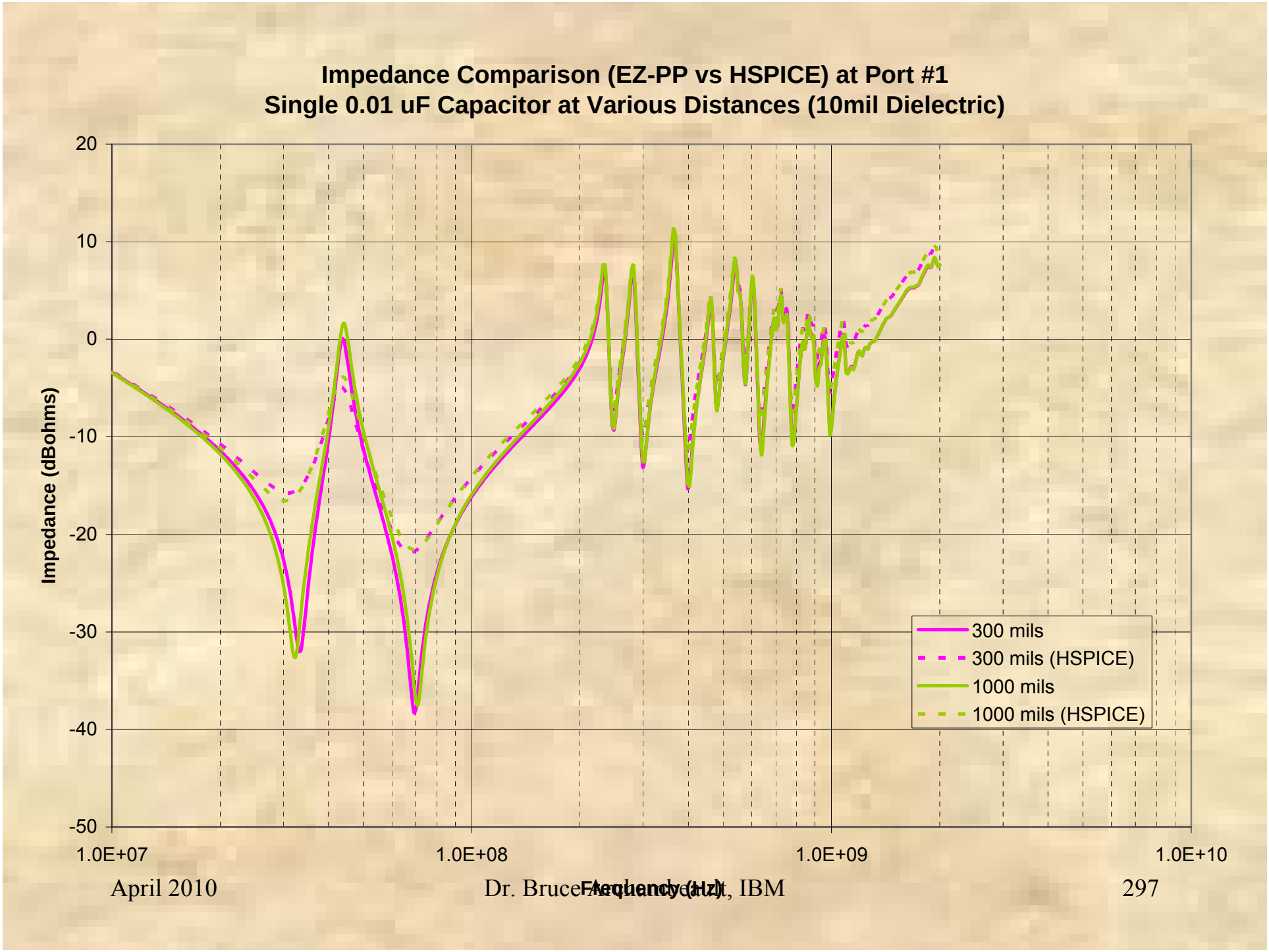

Impedance at Port #1
Single 0.01 uF Capacitor at Various Distances (35mil Dielectric)
Impedance (dBohms)
30
20
10
0
-10
-20
-30
-40
1.0E+07
1.0E+08
1.0E+09
1.0E+10
Frequency (Hz)
no caps
300 mils
500 mils
700 mils
1000 mils

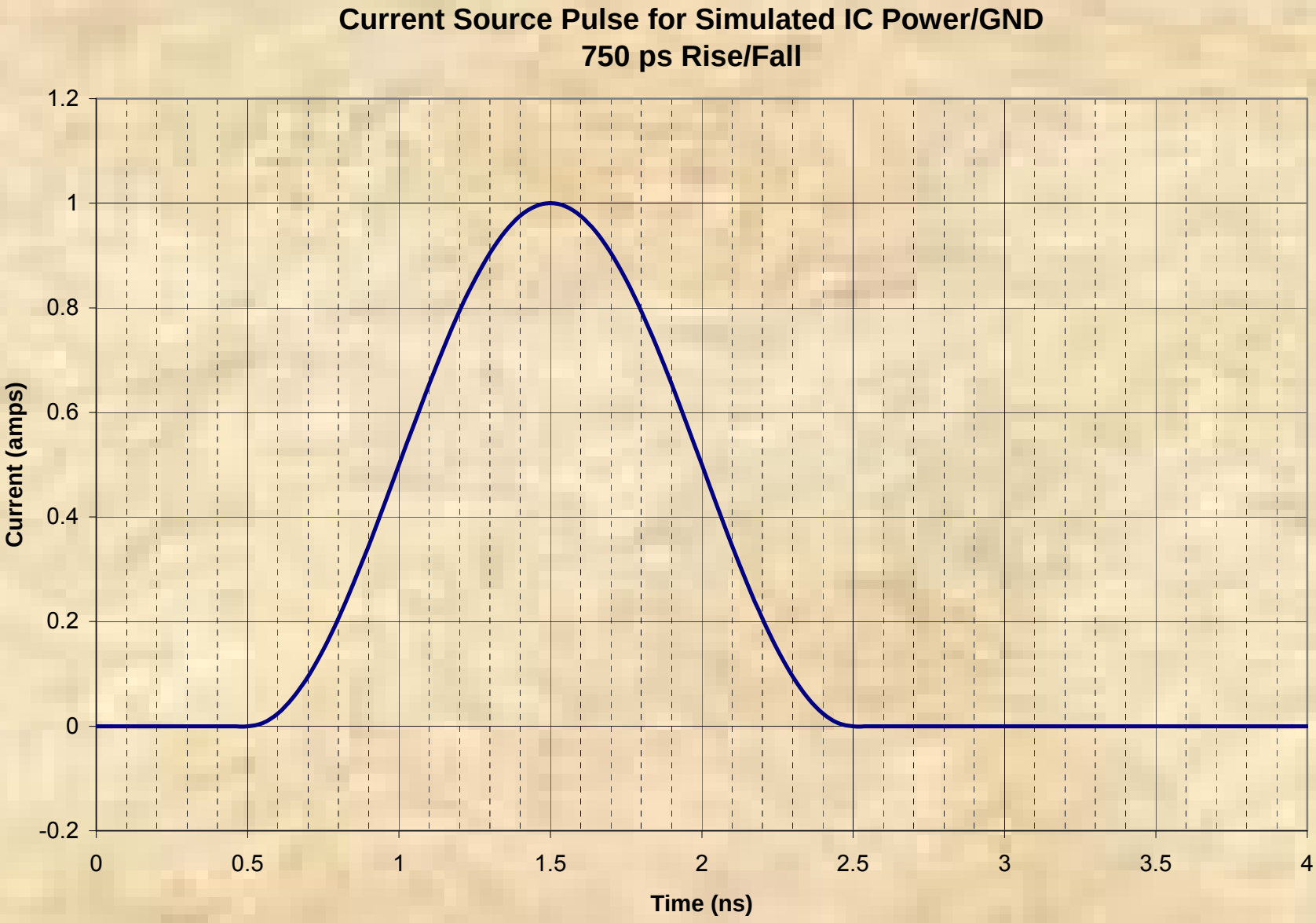

Z11 Phase Comparison as Capacitor distance Varies for 35 mils FR4
ESL = 0.5nH
Phase (rad)
2
1.5
1
0.5
0
-0.5
-1
-1.5
-2
1.0E+06
1.0E+07
1.0E+08
1.0E+09
Frequency (Hz)
100 mils
200 mils
300 mils
400 mils
1000 mils
2000 mils

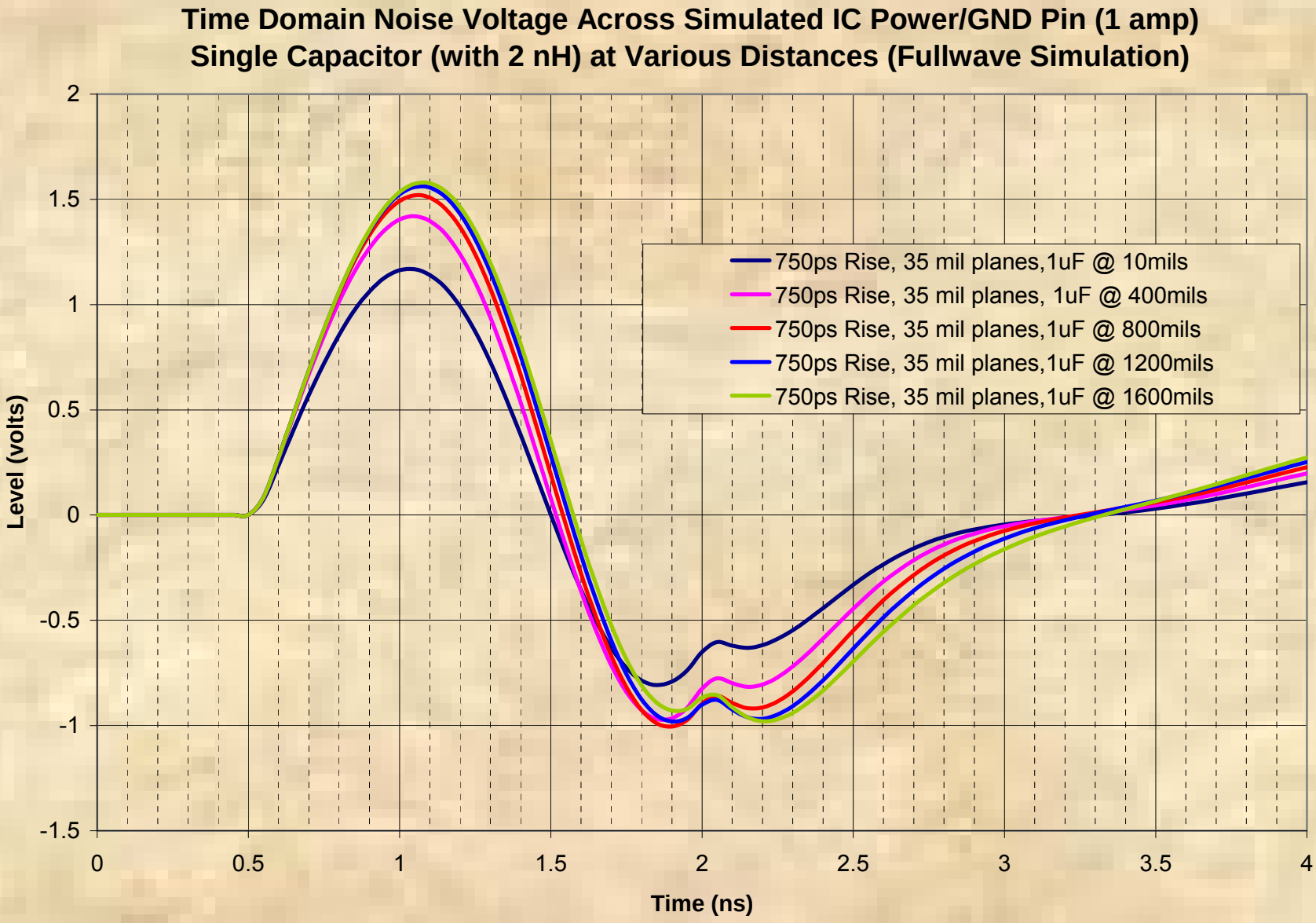

Impedance at Port #1
Single 0.01 uF Capacitor at Various Distances (10mil Dielectric)
Impedance (dBohms)
20
10
0
-10
-20
-30
-40
-50
1.0E+07
1.0E+08
1.0E+09
1.0E+10
Frequency (Hz)
no caps
300 mils
500 mils
700 mils
1000 mils

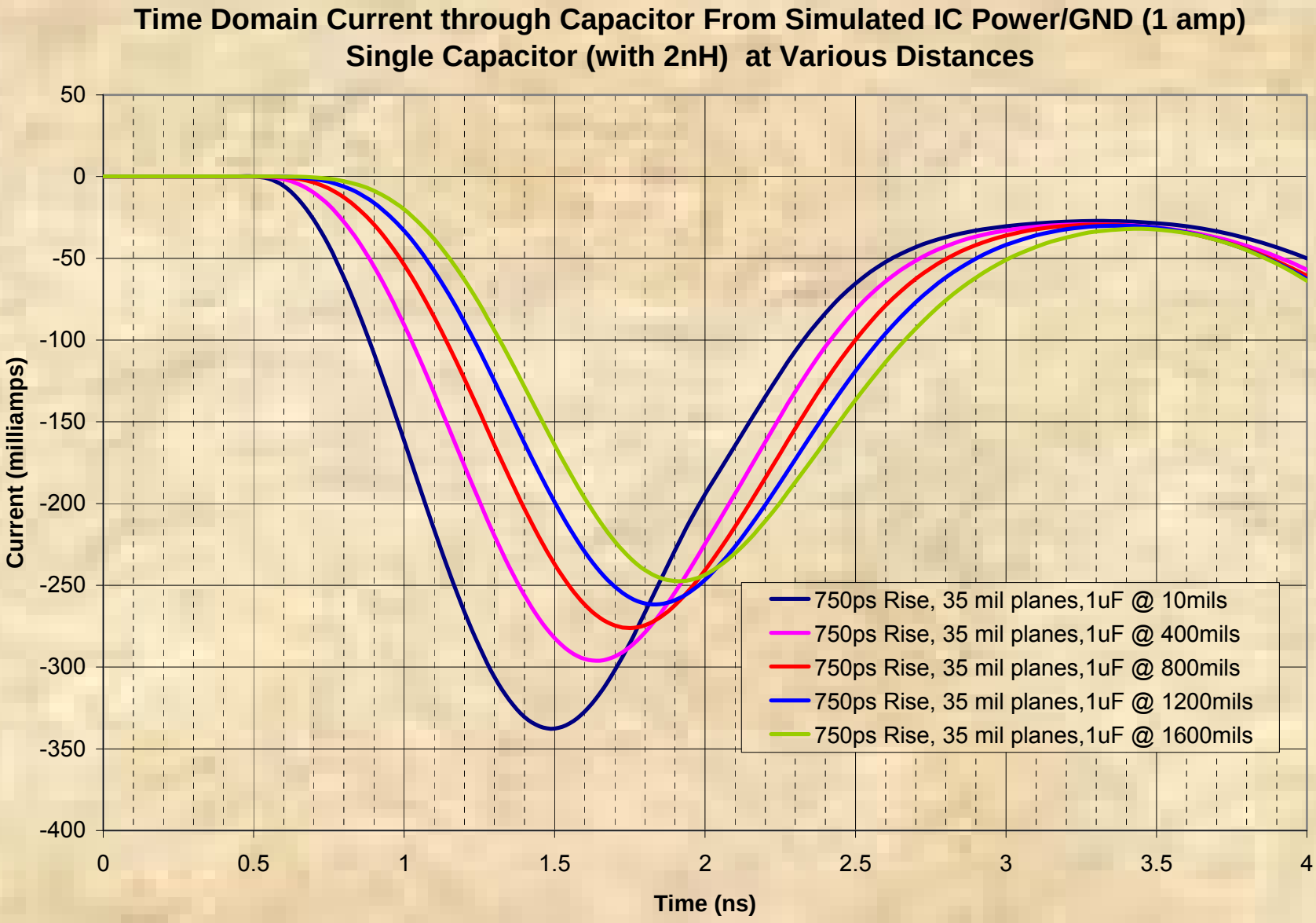
Cavity Resonance (EZ-PowerPlane) Equivalent Circuit for HSPICE



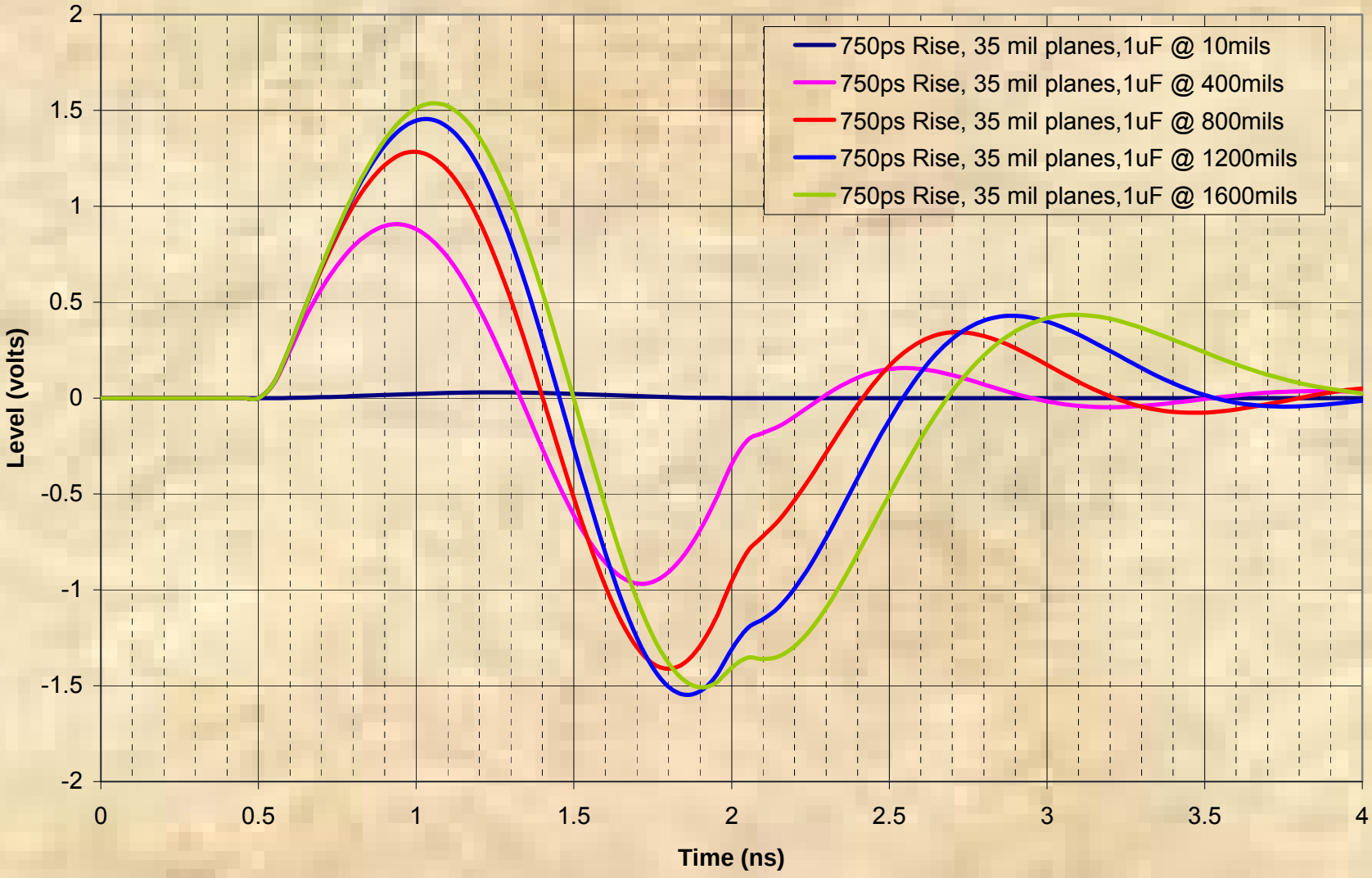

Impedance Comparison (EZ-PP vs HSPICE) at Port #1
Single 0.01 uF Capacitor at Various Distances (10mil Dielectric)
Impedance (dBohms)
20
10
0
-10
-20
-30
-40
-50
1.0E+07
1.0E+08
1.0E+09
1.0E+10
Frequency (Hz)
300 mils
300 mils (HSPICE)
1000 mils
1000 mils (HSPICE)

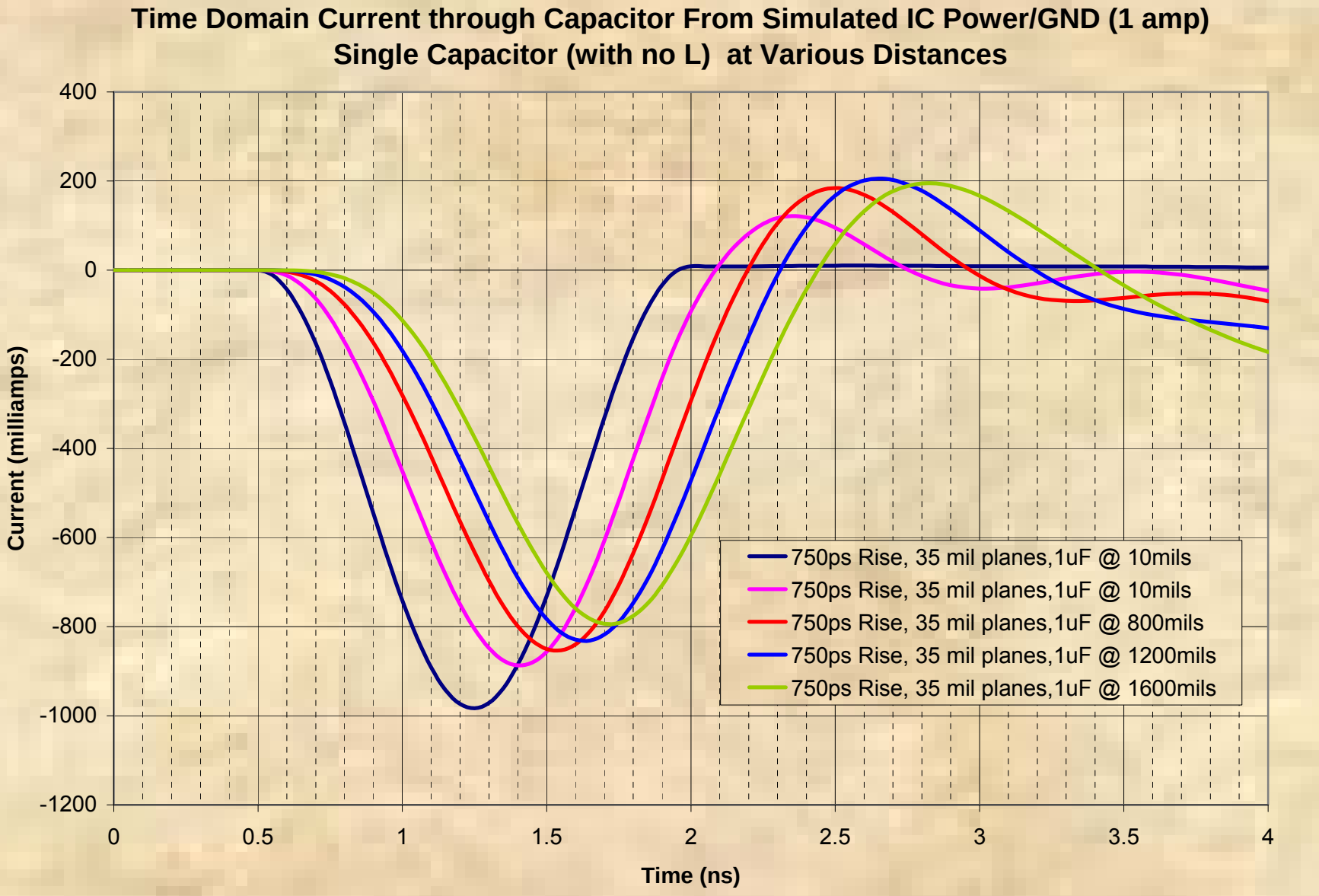

Current Source Pulse for Simulated IC Power/GND
750 ps Rise/Fall
Current (amps)
1.2
1
0.8
0.6
0.4
0.2
0
-0.2
0
0.5
1
1.5
2
2.5
3
3.5
4
Time (ns)


Time Domain Noise Voltage Across Simulated IC Power/GND Pin (1 amp)
Single Capacitor (with 2 nH) at Various Distances (Fullwave Simulation)
Level (volts)
Time (ns)
2
1.5
1
0.5
0
-0.5
-1
-1.5
0
0.5
1
1.5
2
2.5
3
3.5
4
750ps Rise, 35 mil planes,1uF @ 10mils
750ps Rise, 35 mil planes, 1uF @ 400mils
750ps Rise, 35 mil planes,1uF @ 800mils
750ps Rise, 35 mil planes,1uF @ 1200mils
750ps Rise, 35 mil planes,1uF @ 1600mils

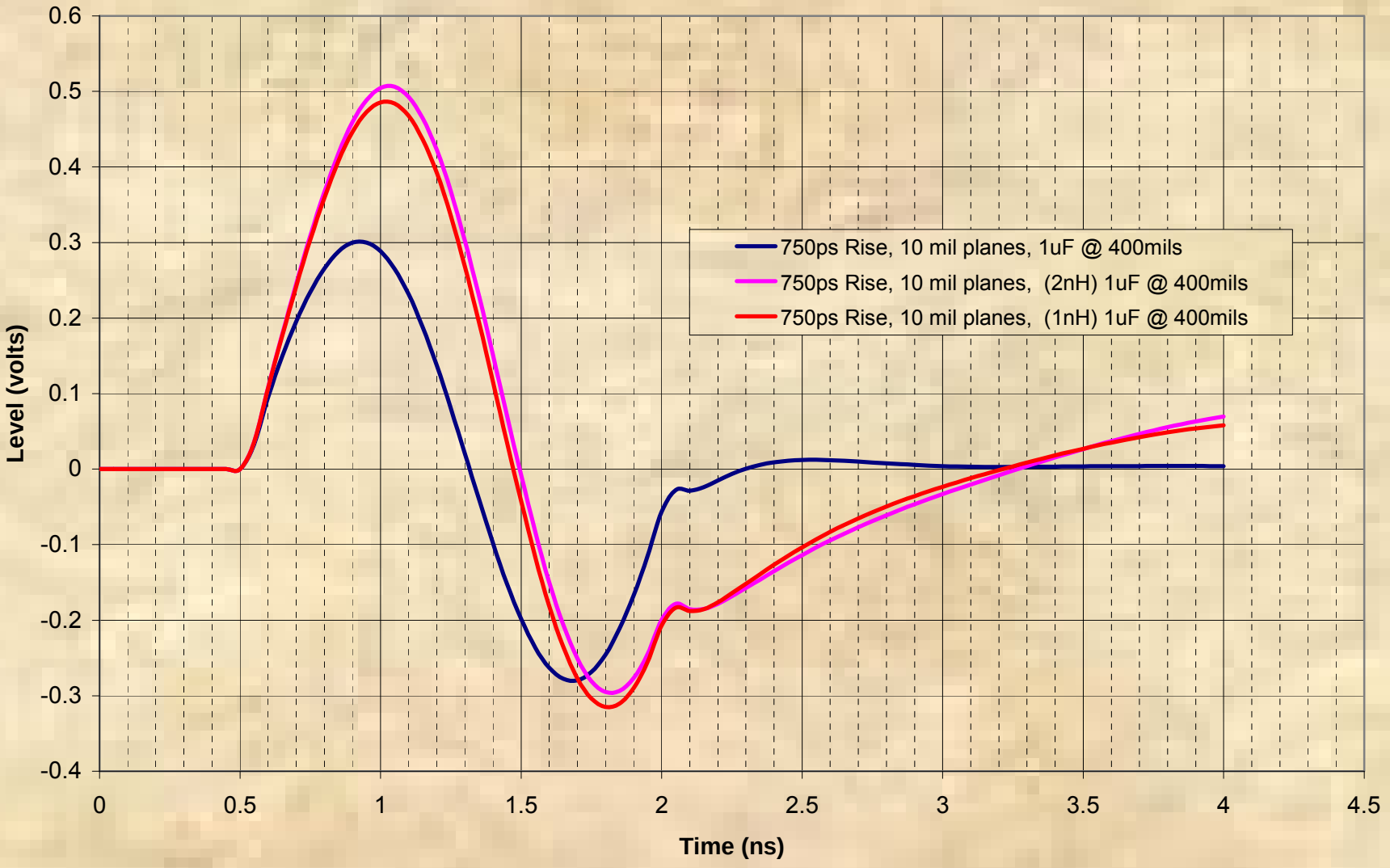

Time Domain Current through Capacitor From Simulated IC Power/GND (1 amp)
Single Capacitor (with 2nH) at Various Distances
Current (milliamps)
50
0
-50
-100
-150
-200
-250
-300
-350
-400
0
0.5
1
1.5
2
2.5
3
3.5
4
Time (ns)
750ps Rise, 35 mil planes,1uF @ 10mils
750ps Rise, 35 mil planes,1uF @ 400mils
750ps Rise, 35 mil planes,1uF @ 800mils
750ps Rise, 35 mil planes,1uF @ 1200mils
750ps Rise, 35 mil planes,1uF @ 1600mils

Time Domain Noise Voltage Across Simulated IC Power/GND Pin (1 amp)
Single Capacitor (with No L) at Various Distances

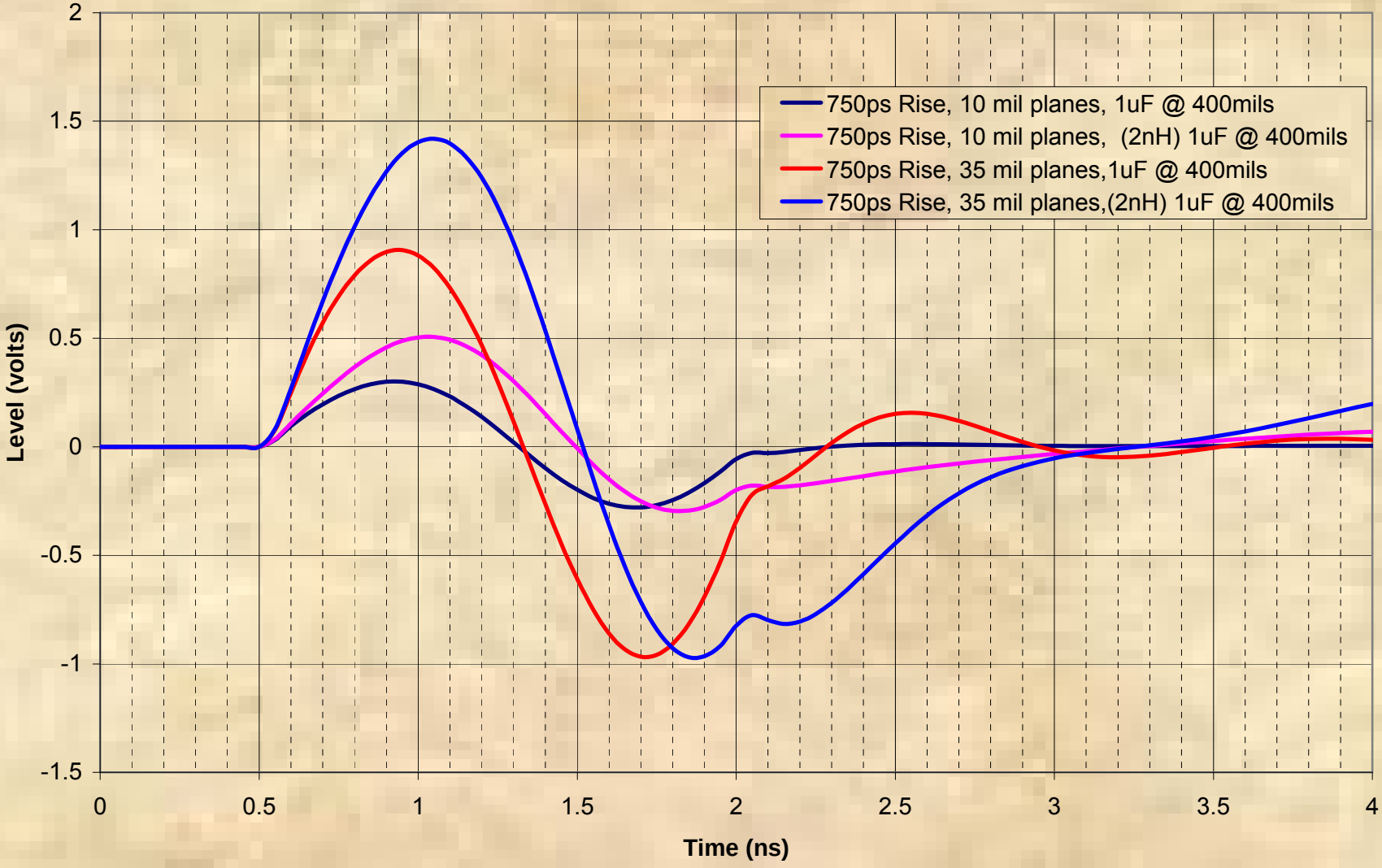



Time Domain Current through Capacitor From Simulated IC Power/GND (1 amp)
Single Capacitor (with no L) at Various Distances
Current (milliamps)
400
200
0
-200
-400
-600
-800
-1000
-1200
0
0.5
1
1.5
2
2.5
3
3.5
4
Time (ns)
750ps Rise, 35 mil planes,1uF @ 10mils
750ps Rise, 35 mil planes,1uF @ 10mils
750ps Rise, 35 mil planes,1uF @ 800mils
750ps Rise, 35 mil planes,1uF @ 1200mils
750ps Rise, 35 mil planes,1uF @ 1600mils

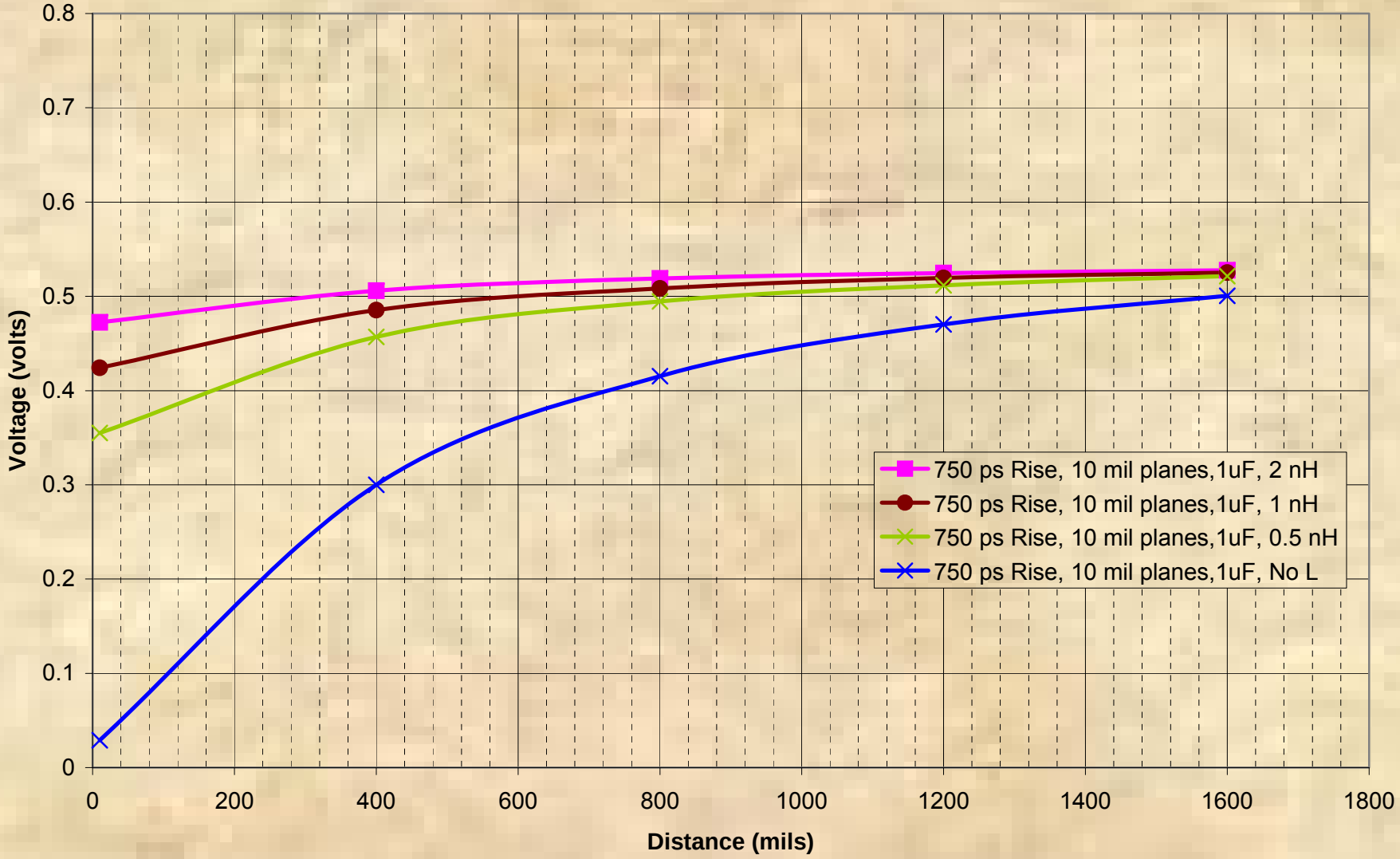
Time Domain Noise Voltage Across Simulated IC Power/GND Pin (1 amp)
Single Capacitor with Various Capacitor Connection Inductance



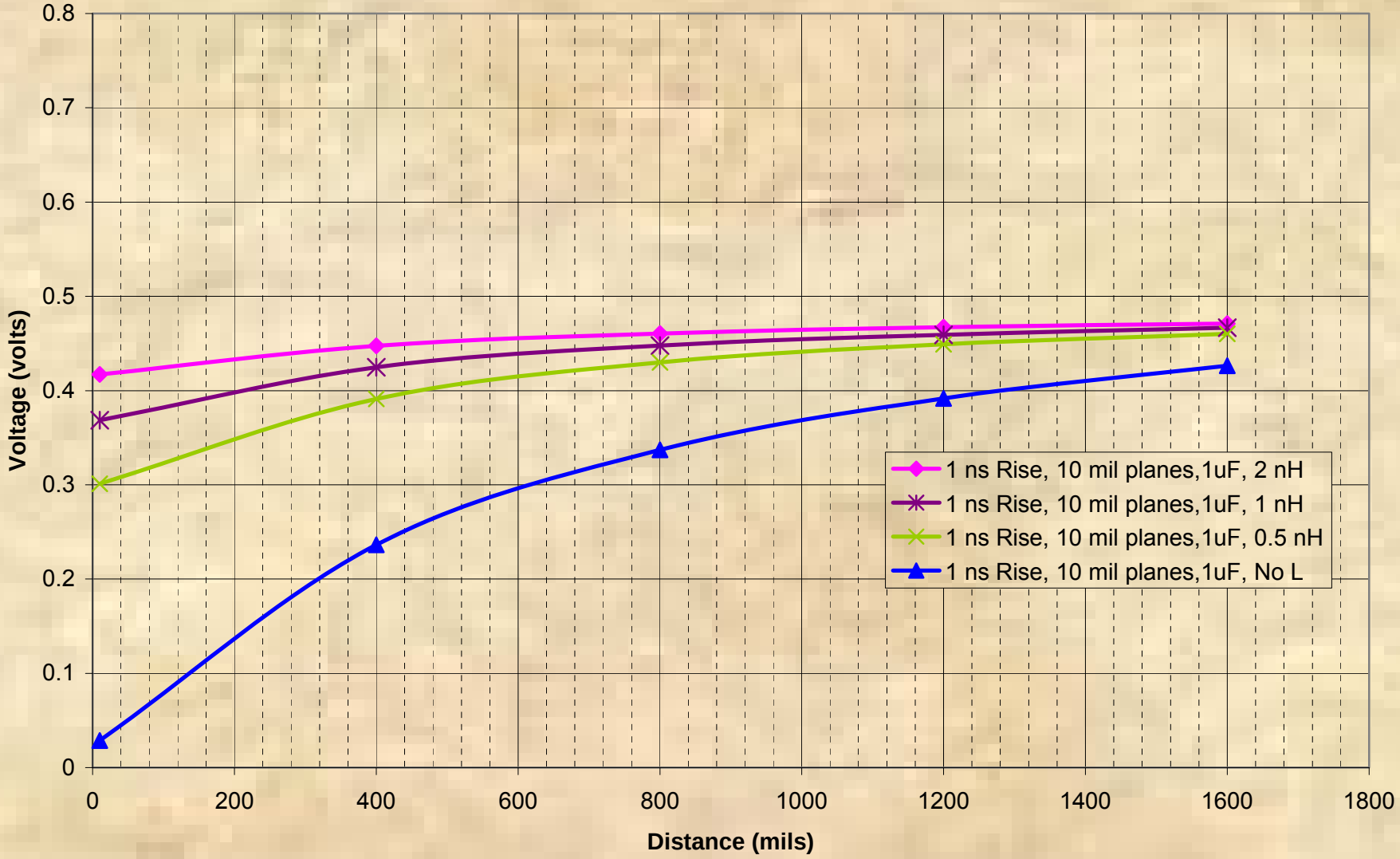
Time Domain Noise Voltage Across Simulated IC Power/GND Pin (1 amp)
Single Capacitor with Various Capacitor Connection Inductance



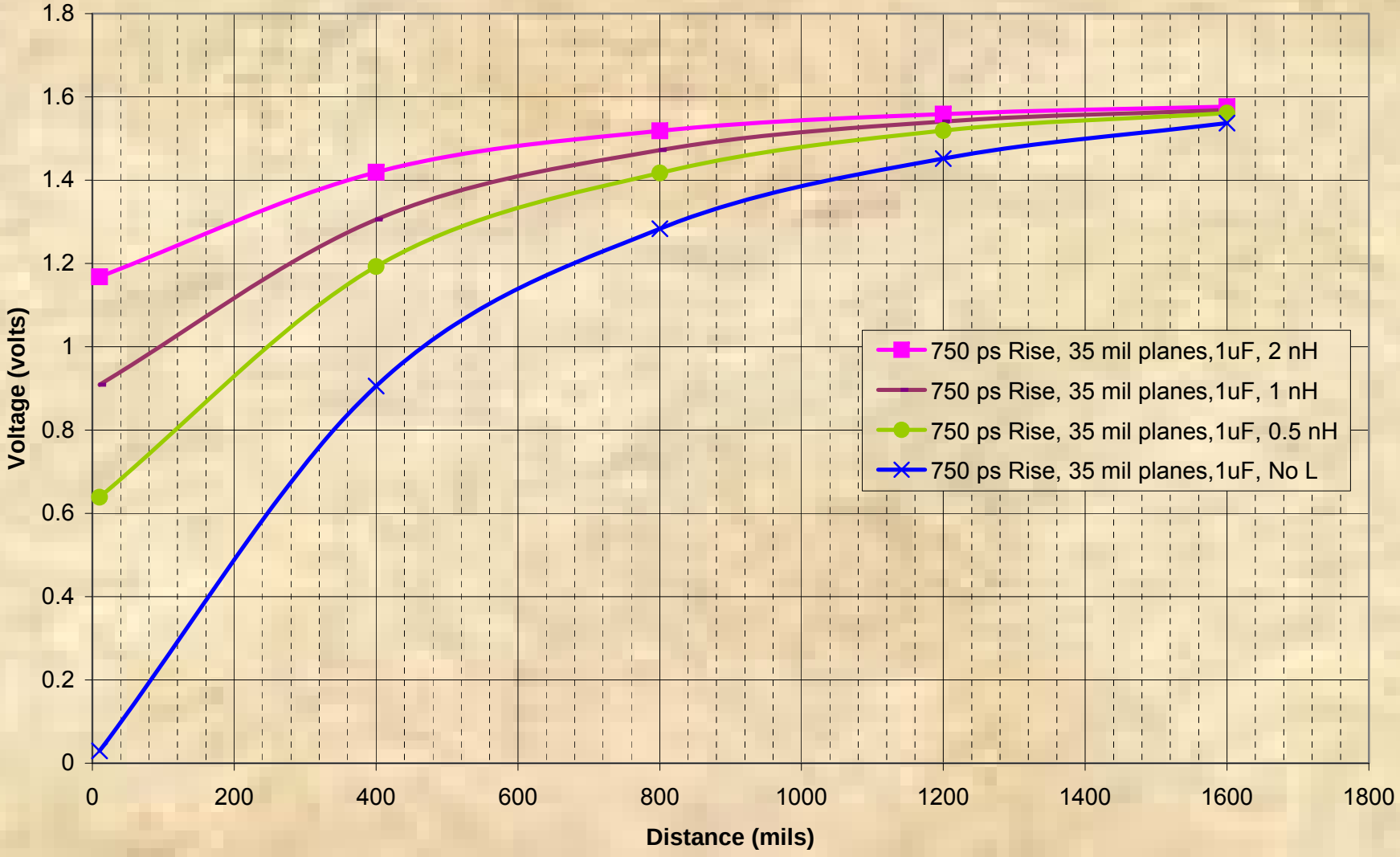
Maximum Time Domain Noise Voltage Across Simulated IC Power/GND Pin Single Capacitor at Various Distances (Fullwave Simulation)

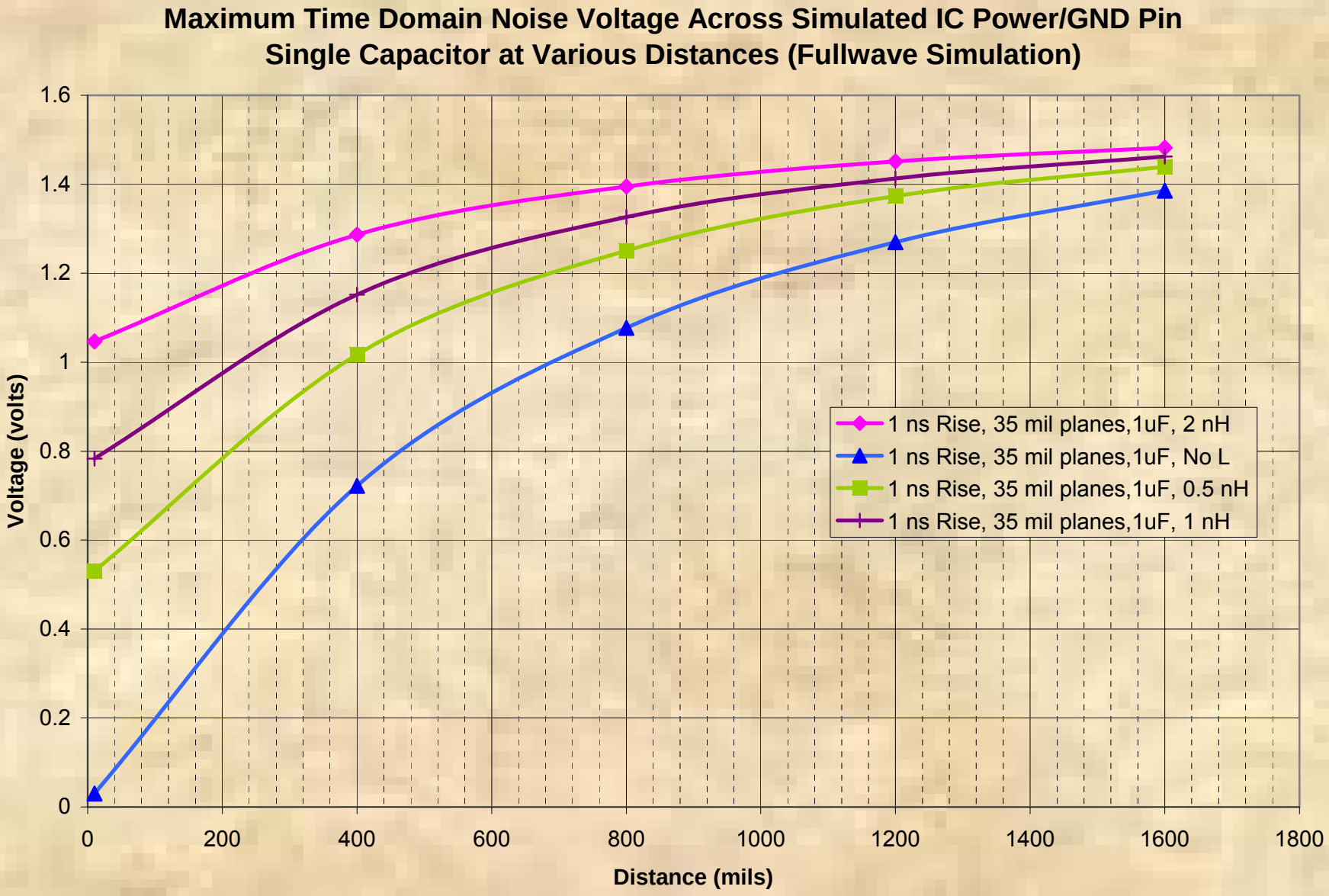


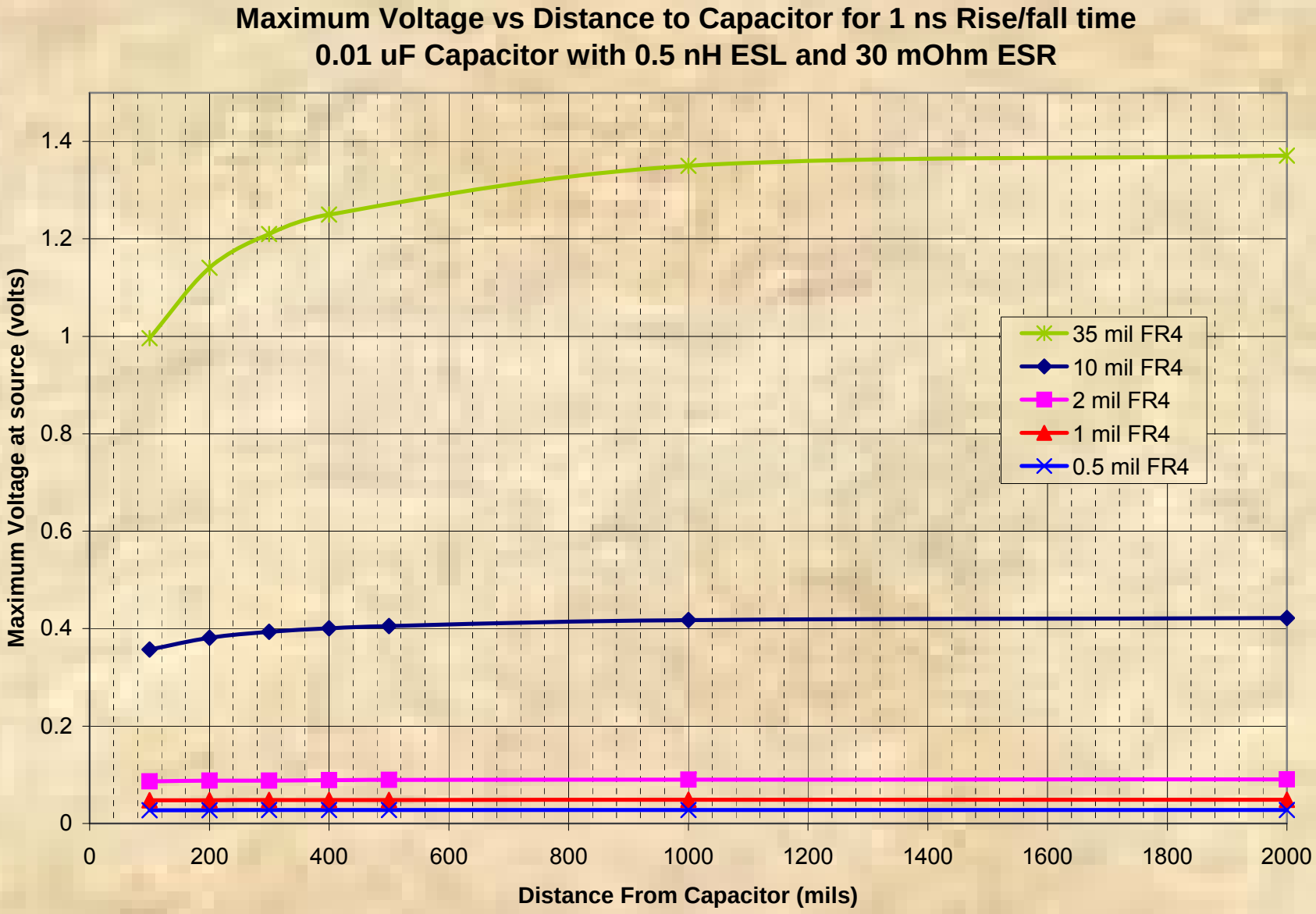
Maximum Time Domain Noise Voltage Across Simulated IC Power/GND Pin
Single Capacitor at Various Distances (Fullwave Simulation)



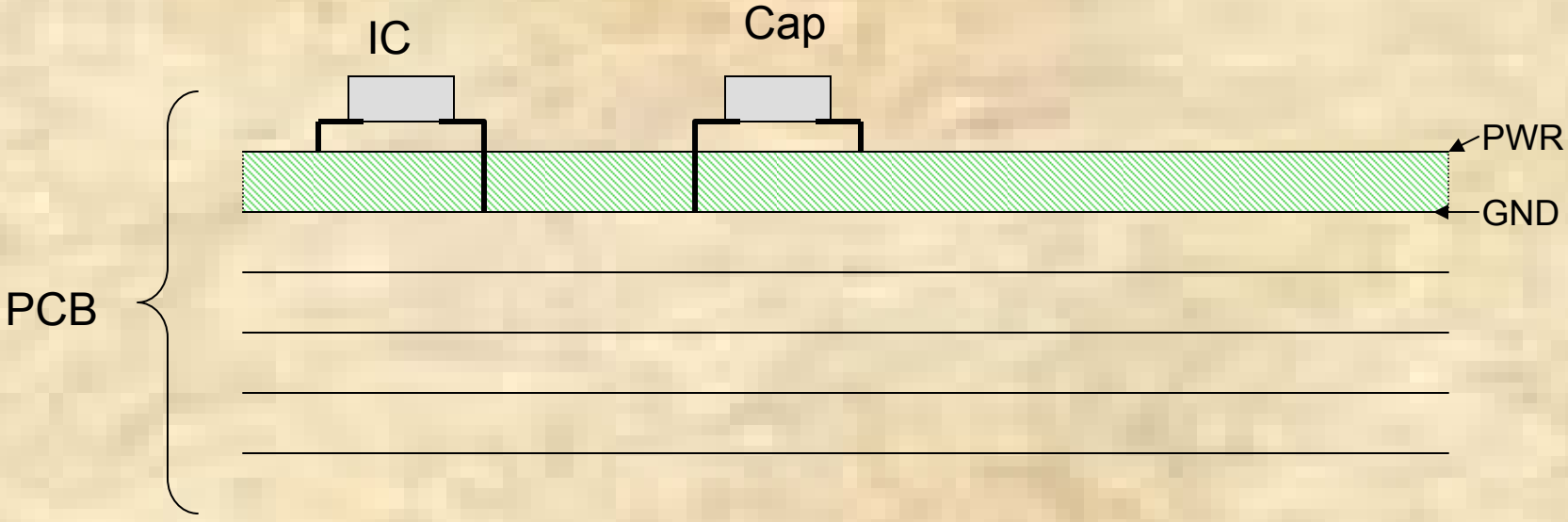
Maximum Time Domain Noise Voltage Across Simulated IC Power/GND Pin
Single Capacitor at Various Distances (Fullwave Simulation)



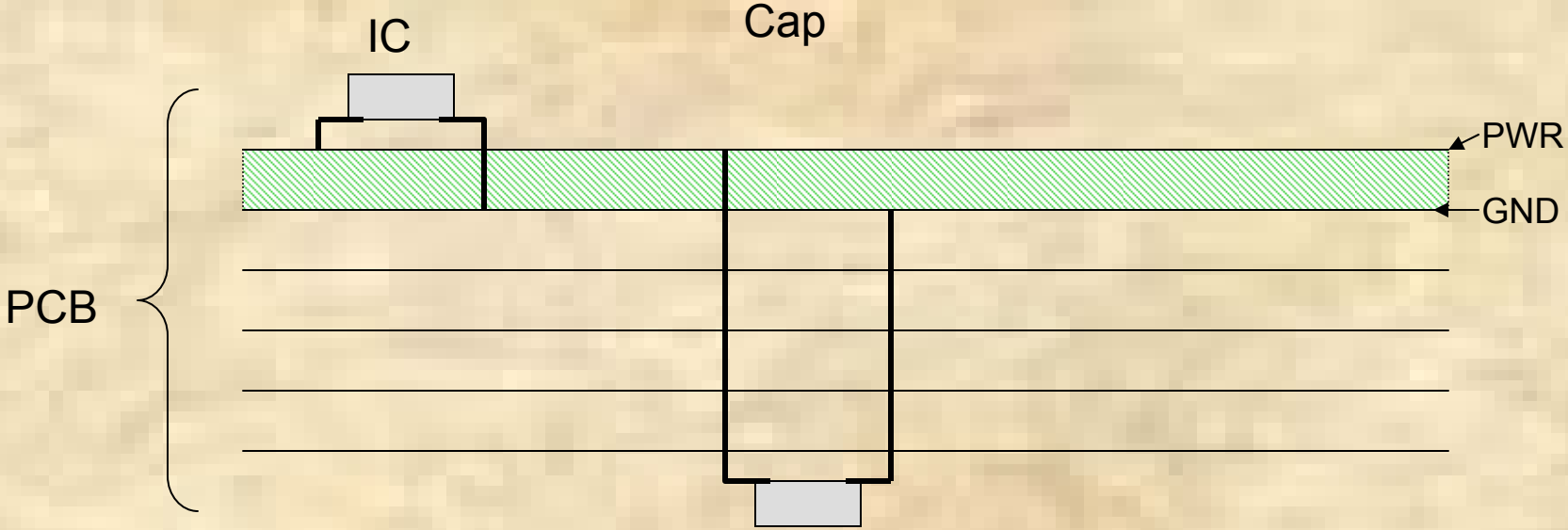

Maximum Time Domain Noise Voltage Across Simulated IC Power/GND Pin
Single Capacitor at Various Distances (Fullwave Simulation)
Voltage (volts)
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
0
200
400
600
800
1000
1200
1400
1600
1800
Distance (mils)
1 ns Rise, 35 mil planes,1uF, 2 nH
1 ns Rise, 35 mil planes,1uF, No L
1 ns Rise, 35 mil planes,1uF, 0.5 nH
1 ns Rise, 35 mil planes,1uF, 1 nH


Maximum Voltage vs Distance to Capacitor for 1 ns Rise/fall time
0.01 uF Capacitor with 0.5 nH ESL and 30 mOhm ESR
Maximum Voltage at source (volts)
1.4
1.2
1
0.8
0.6
0.4
0.2
0
0
200
400
600
800
1000
1200
1400
1600
1800
2000
Distance From Capacitor (mils)
35 mil FR4
10 mil FR4
2 mil FR4
1 mil FR4
0.5 mil FR4

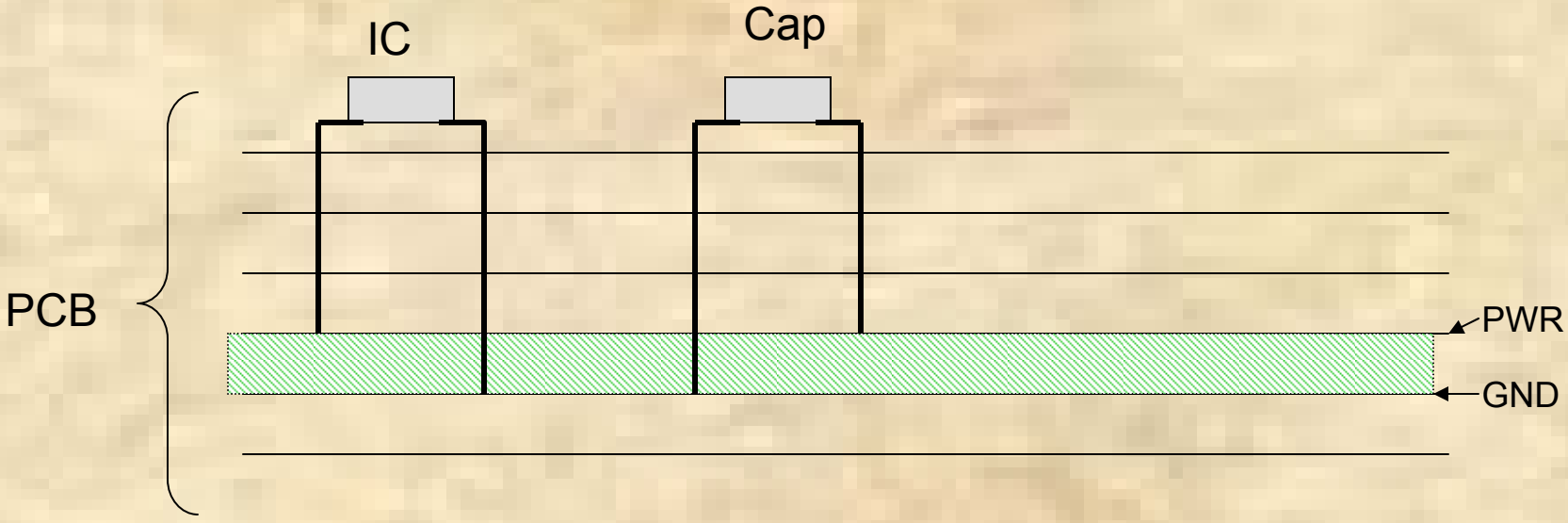
Example #1
Low Cap Connection Inductance



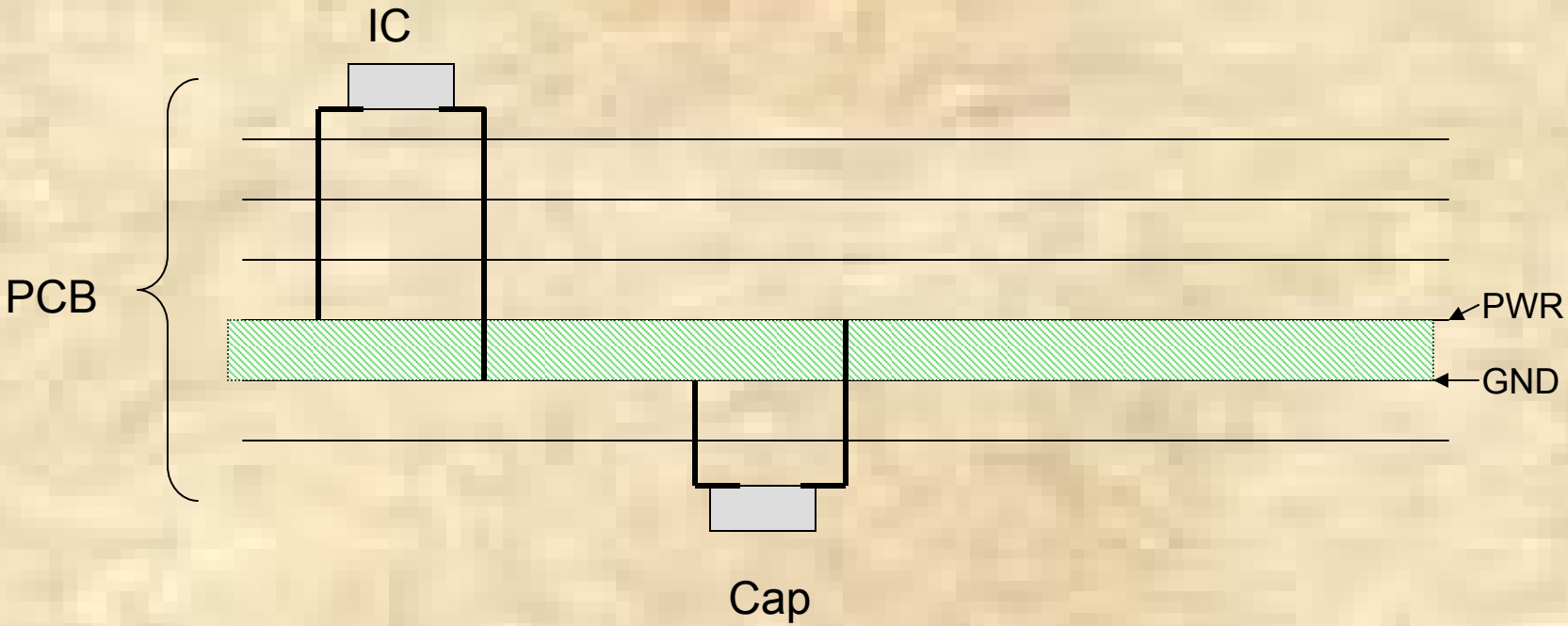
Example #2
High Cap Connection Inductance



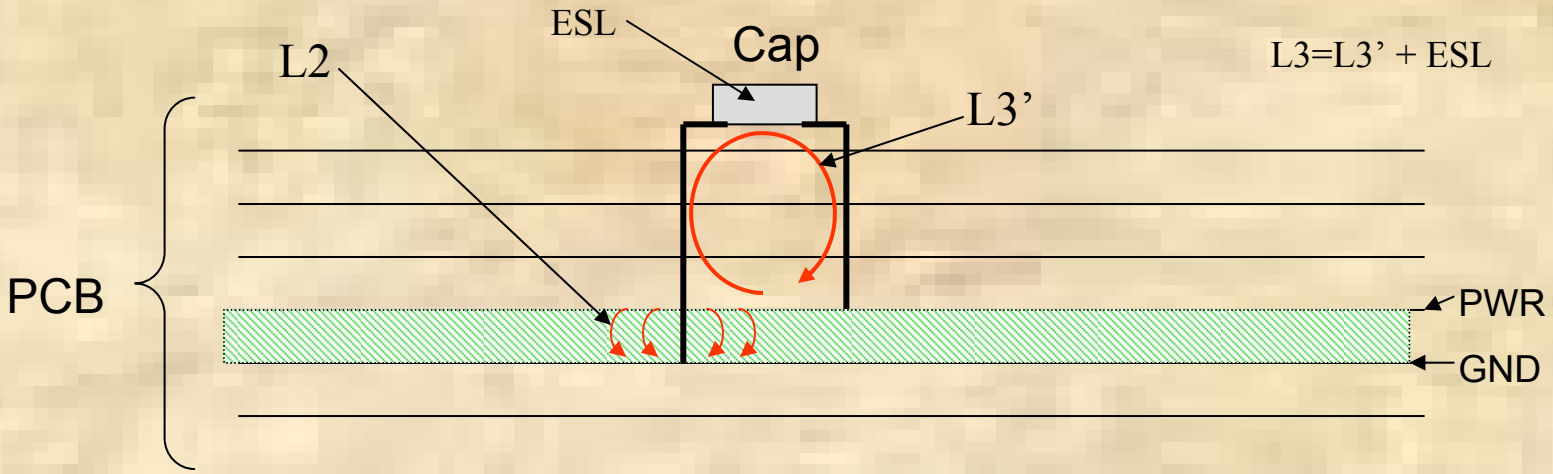
Example #1
Hi Cap Connection Inductance



Example #1
Lower Cap Connection Inductance



Capacitor Connection Inductance Ratio



Power bus thickness, (mils)	via diameter, (mils)	L_2 (nH)
10	10	0.32
10	13	0.304
10	25	0.27
35	10	1.1
35	13	1.07
35	25	0.95

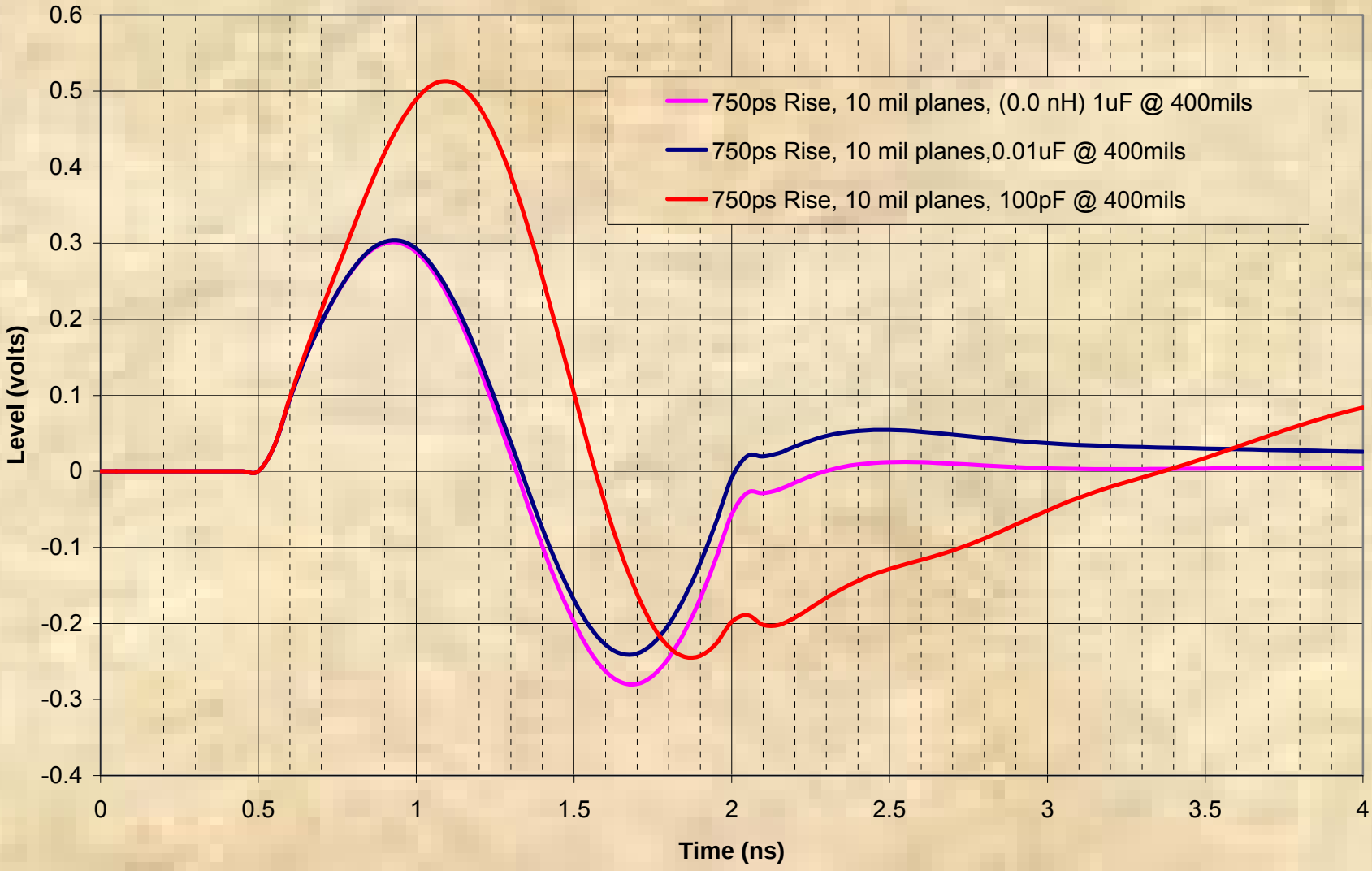
62mil brd centered power bus thickness, mils	0603 SMT L3' (nH)	L3/L2	L3/L2 w/extra 100 mil trace length	L3/L2 w/extra 200 mil trace length	L3/L2 w/extra 300 mil trace length
10	1.66	6.75	9.13	11.50	13.88
35	0.92	1.29	1.98	2.67	3.36

For local decoupling need L3/L2 < 3

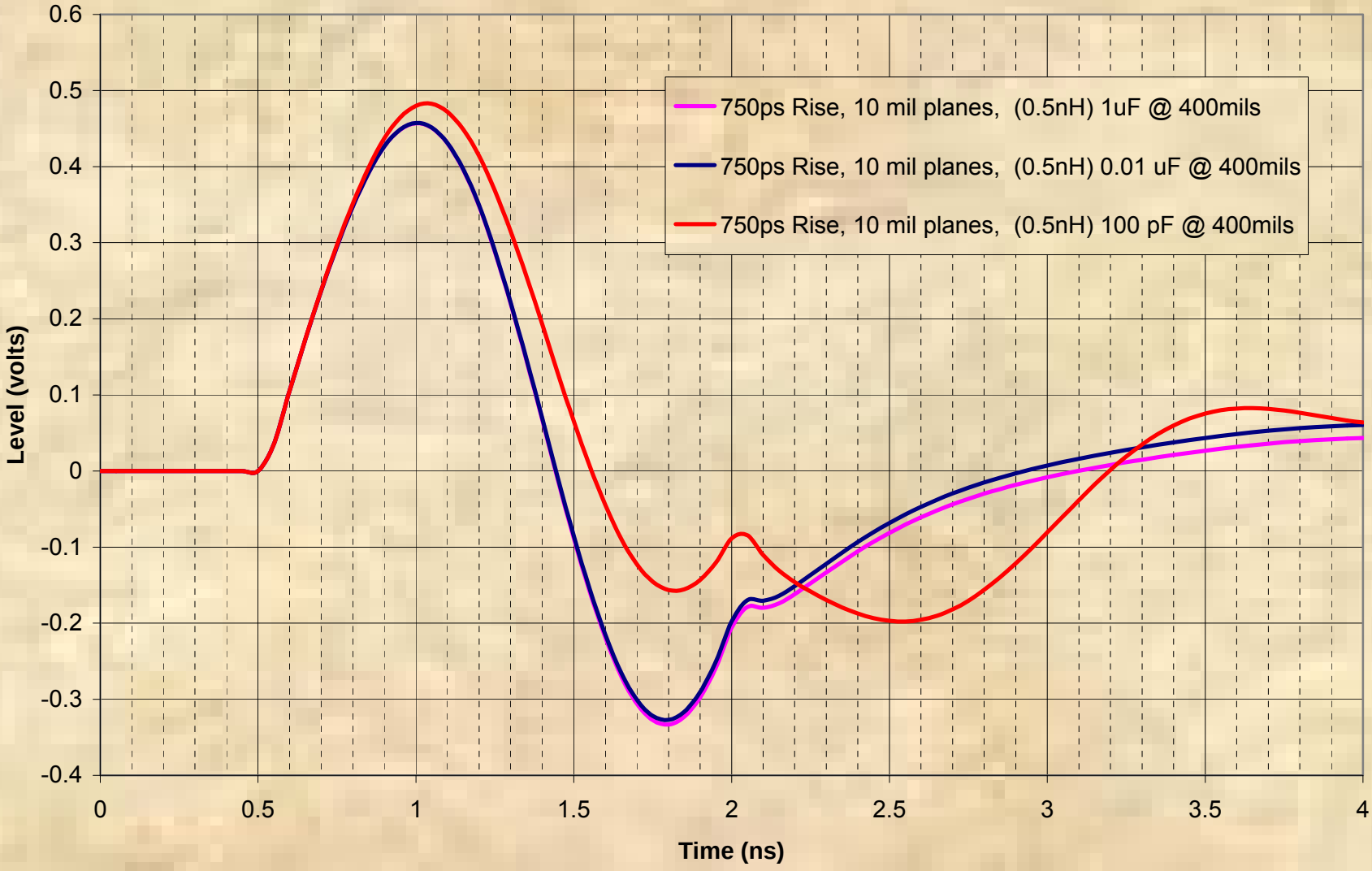
Effect of Capacitor Value??

- Need enough charge to supply need
- Depends on connection inductance

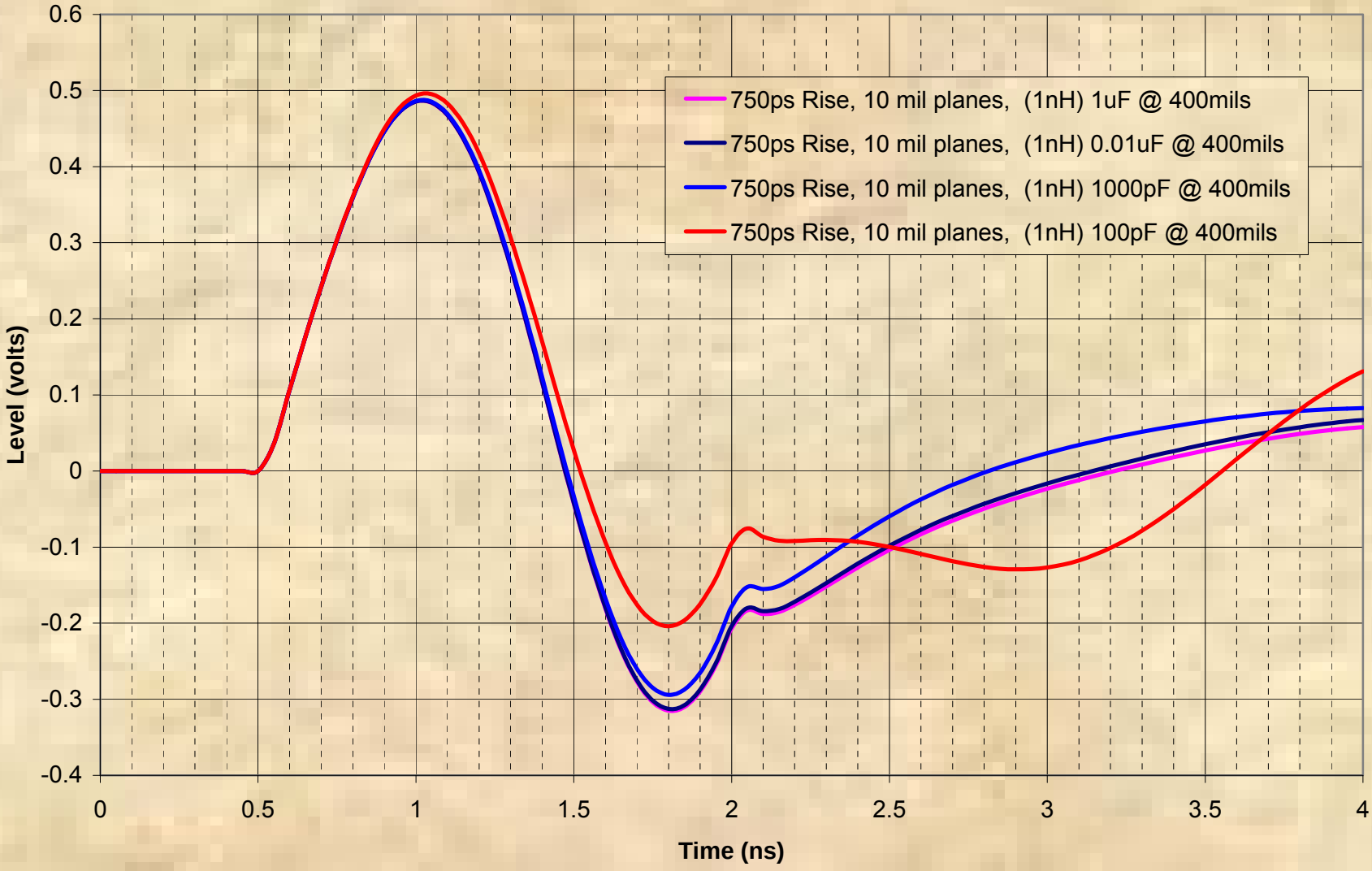
Time Domain Noise Voltage Across Simulated IC Power/GND Pin (1 amp)
Single Capacitor (with No L) with Various Capacitor Values



Time Domain Noise Voltage Across Simulated IC Power/GND Pin (1 amp) Single Capacitor (with 0.5 nH Connection L) with Various Capacitor Values



Time Domain Noise Voltage Across Simulated IC Power/GND Pin (1 amp)
Single Capacitor (with 1 nH Connection L) with Various Capacitor Values



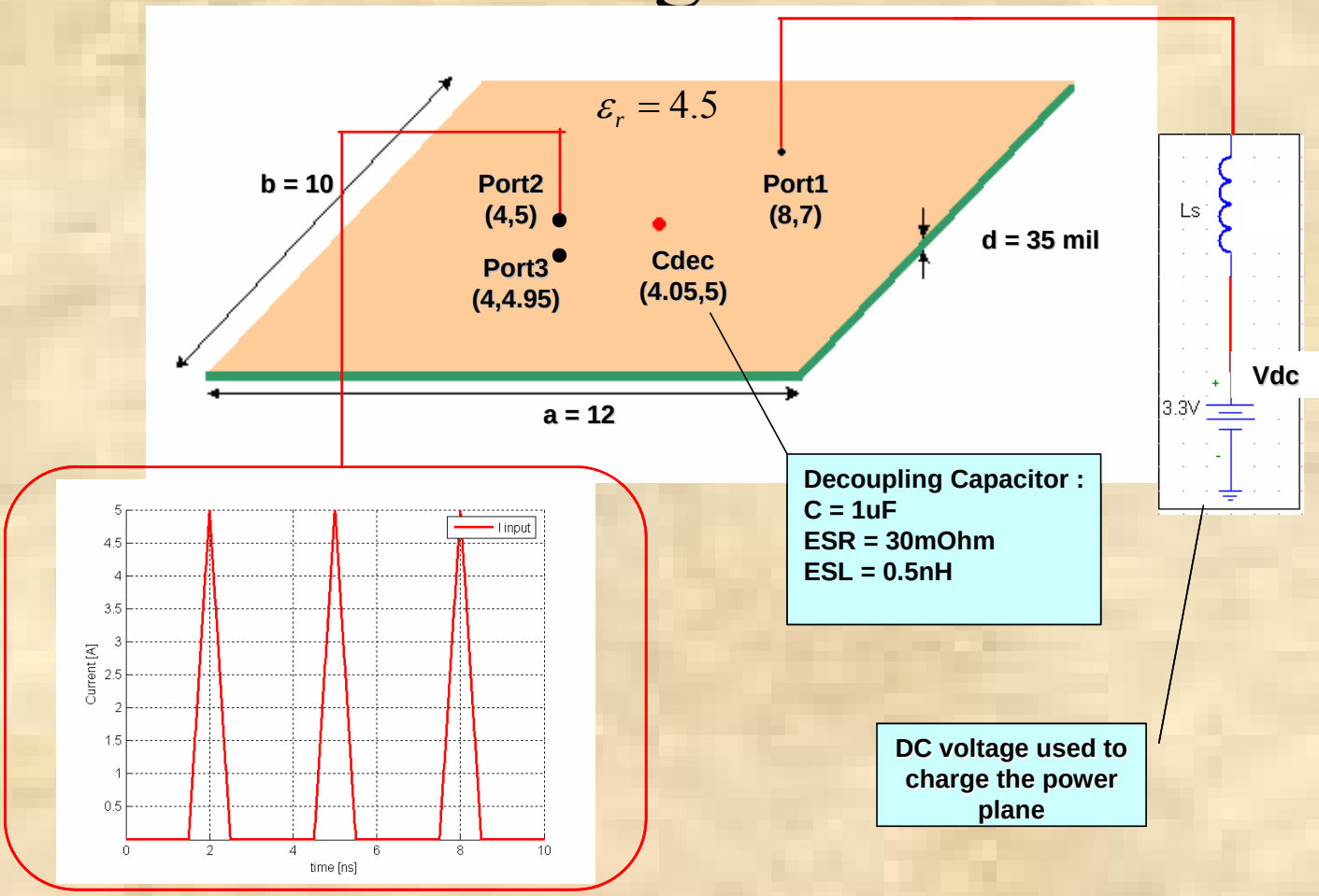
So Far……

- Frequency domain simulations not optimum for charge delivery decoupling calculations (phase not considered)
- Time domain simulations using single pulse of current indicate limited capacitor location effect
  - Connection inductance of capacitor much higher than inductance between planes
  - Charge delivered only from the planes

Charge Depletion

- IC draws charge from planes
- Capacitors will re-charge planes
  - Location ***does*** matter!

Model for Plane Recharge Investigations



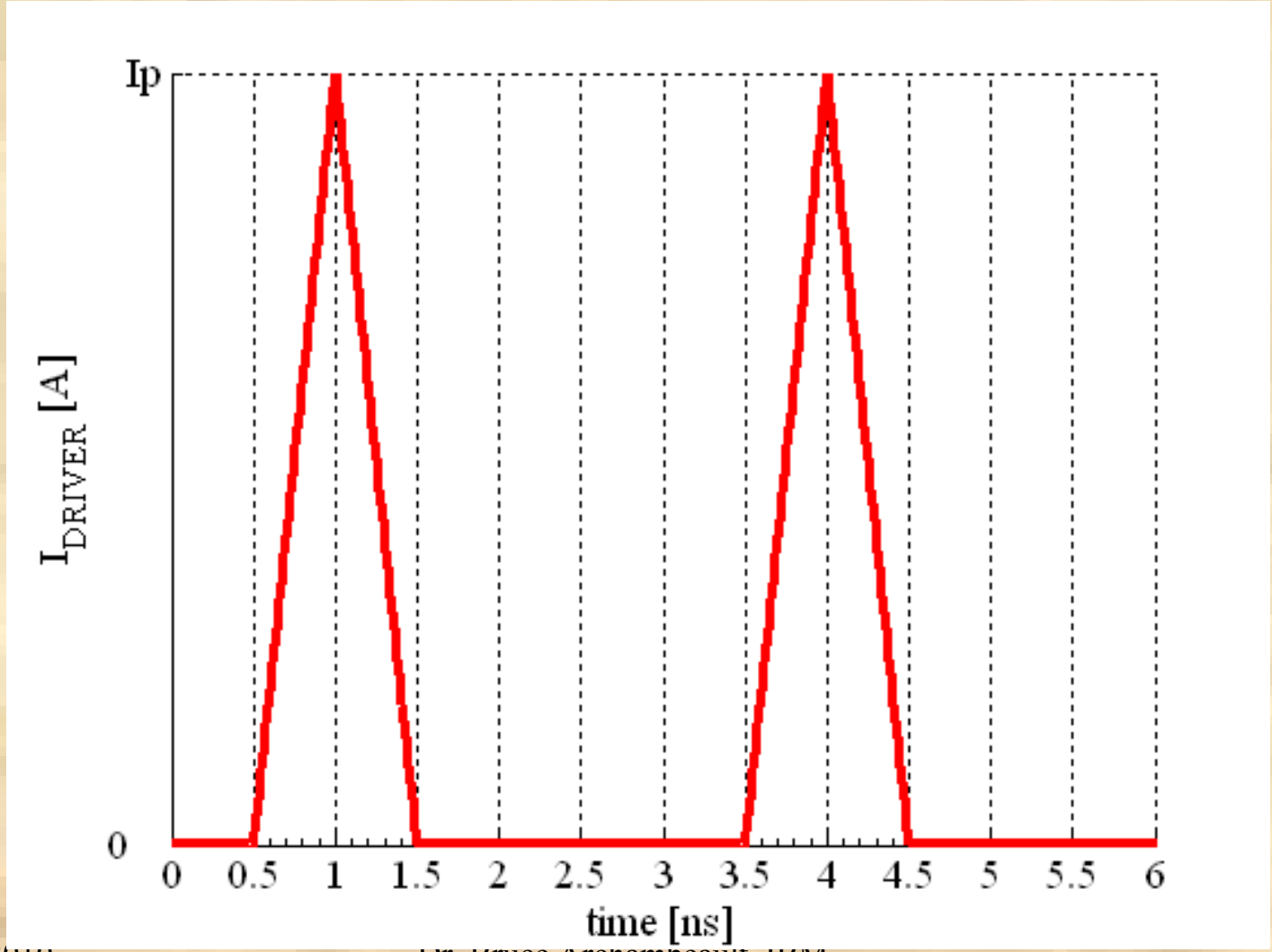
Port 2 represents IC current draw

Charge Between Planes vs.. Charge Drawn by IC

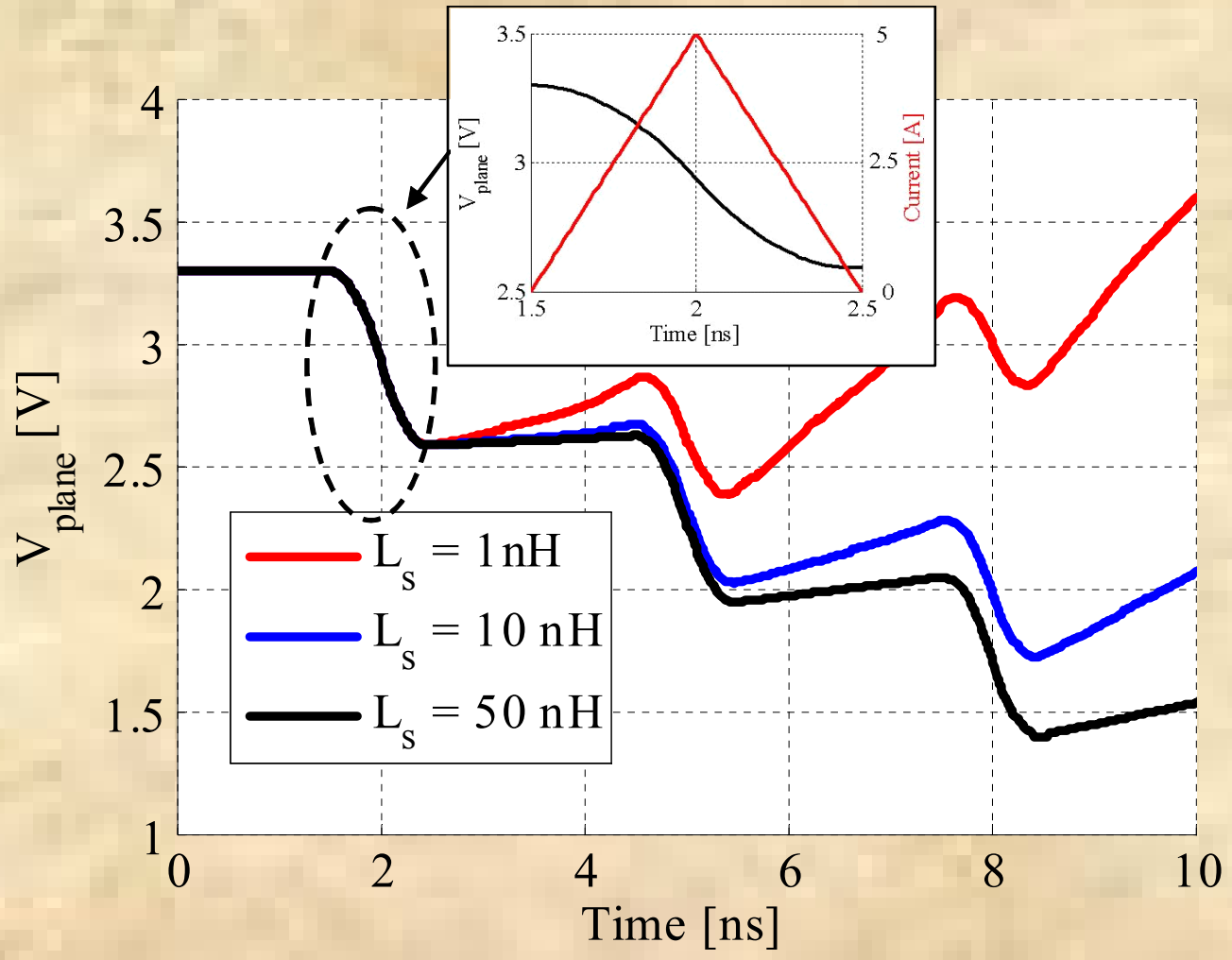
Board total charge : C*V = 3.5nF*3.3V = 11nC

Pulse charge 5A peak : I*dt/2 = (1ns*5A)/2=2.5nC

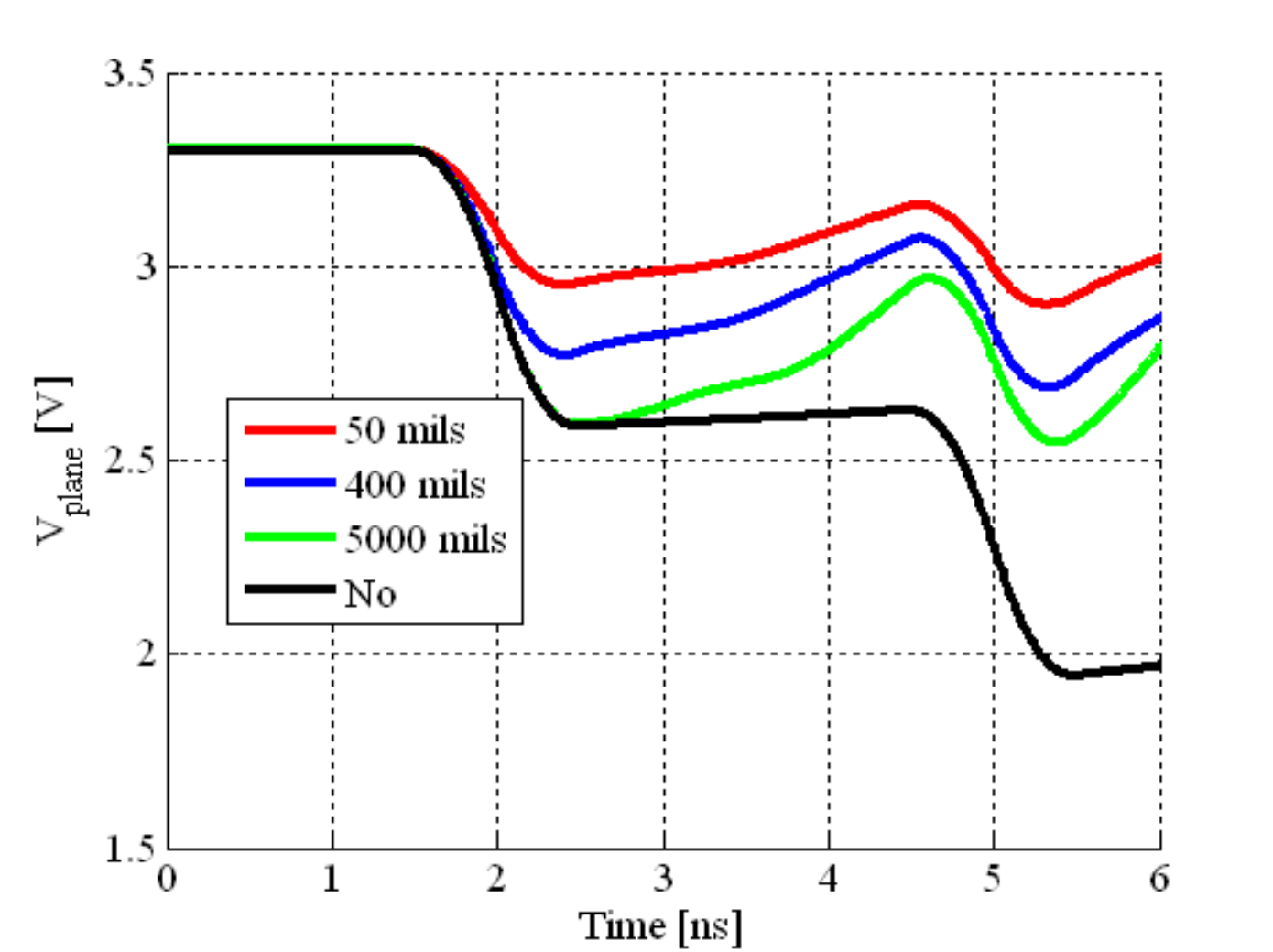
Triangular pulses (5 Amps Peak)



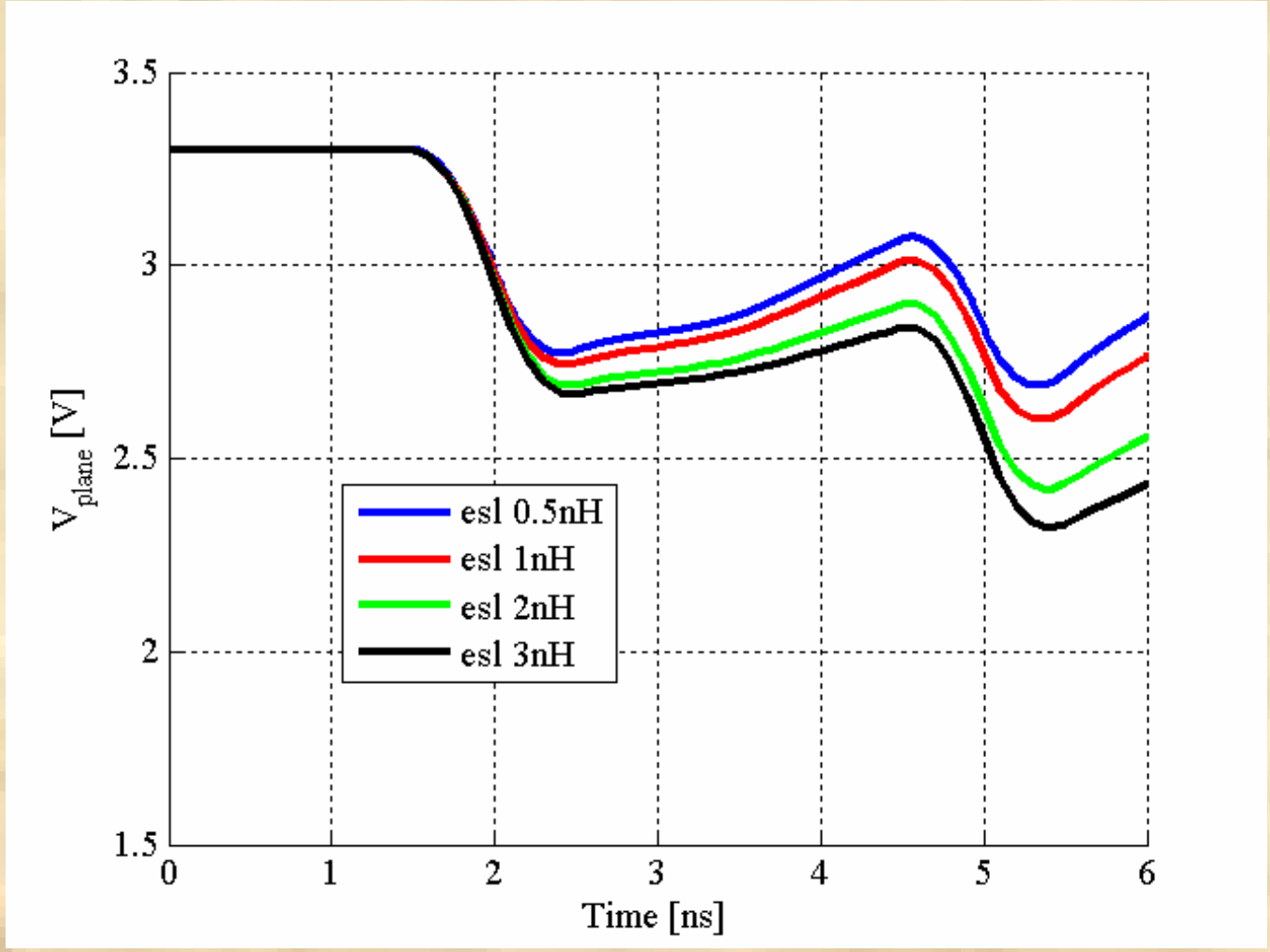
Charge Depletion → Voltage Drop



Charge Depletion vs. Capacitor Distance



Charge Depletion for Capacitor @ 400 mils for Various connection Inductance

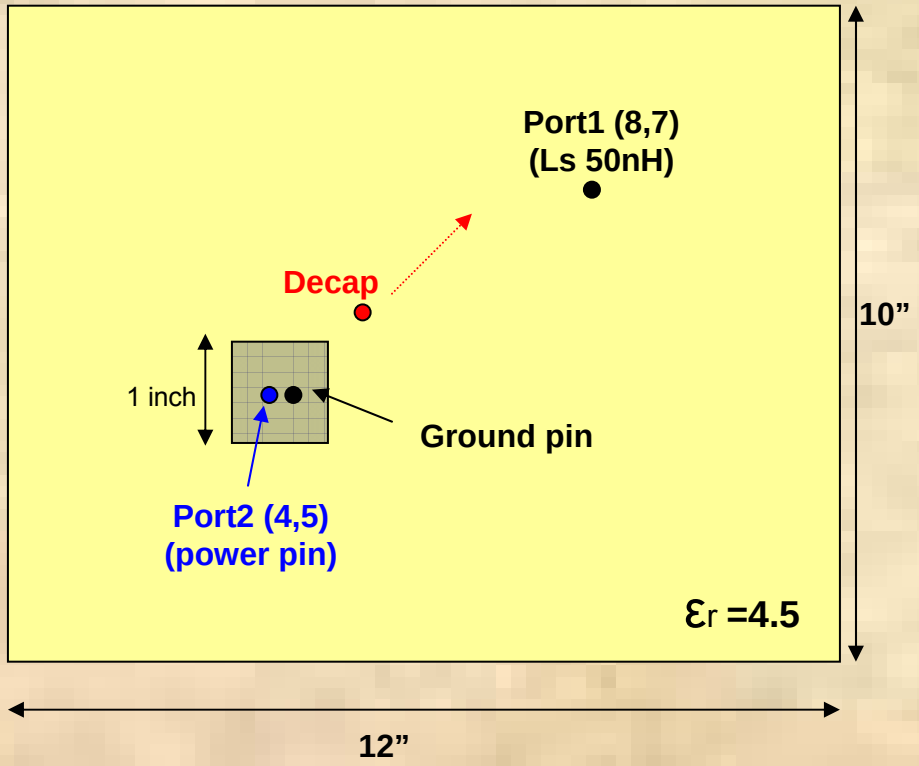


Effect of Multiple Capacitors While Keeping Total Capacitance Constant

The decap locations are 800mils, 1200mils, 2700mils from the power pin

(power-ground pins at IC center)

- C=1uF
- ESL=0.5nH
- ESR=1Ω

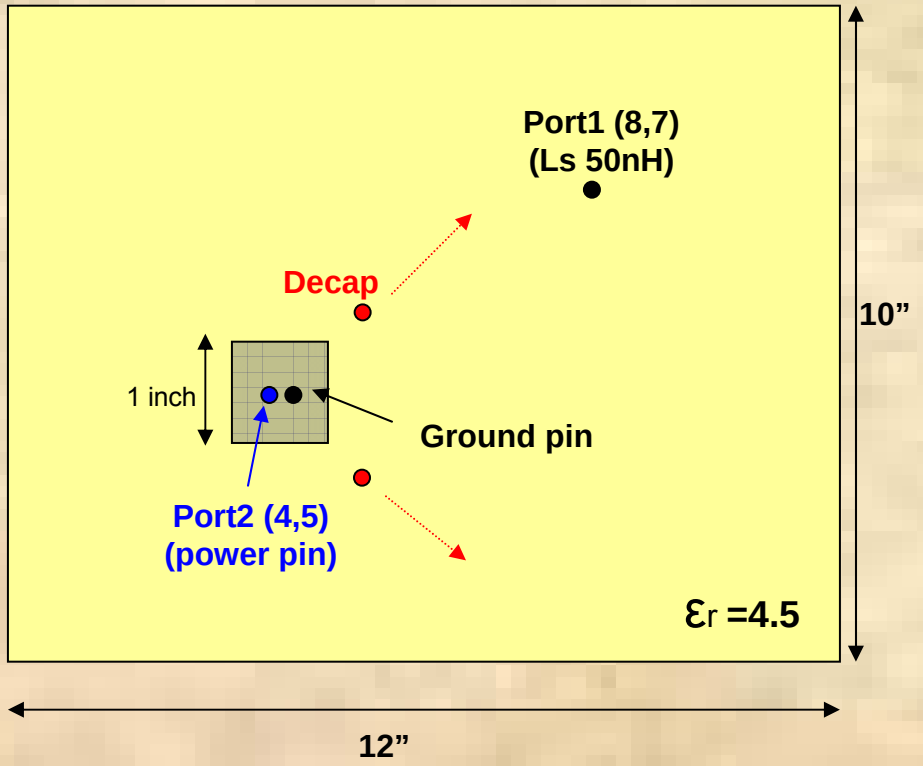


Effect of Multiple Capacitors While Keeping Total Capacitance Constant

The decap locations are 800mils, 1200mils, 2700mils from the power pin

(power-ground pins at IC center)

- C=0.5uF
- ESL=0.5nH
- ESR=1Ω

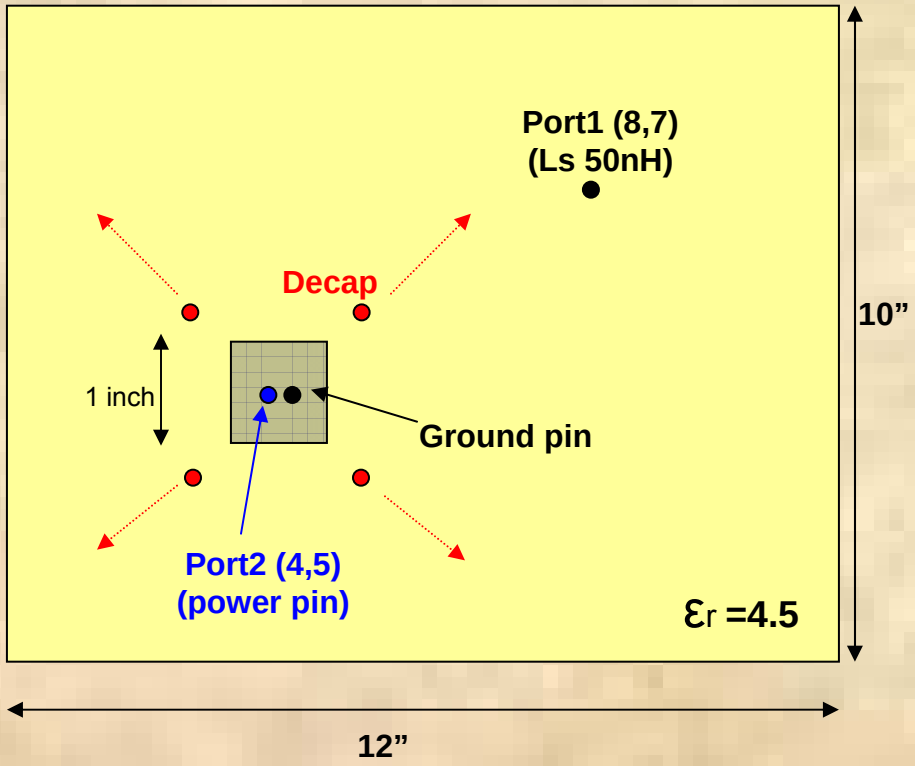


Effect of Multiple Capacitors While Keeping Total Capacitance Constant

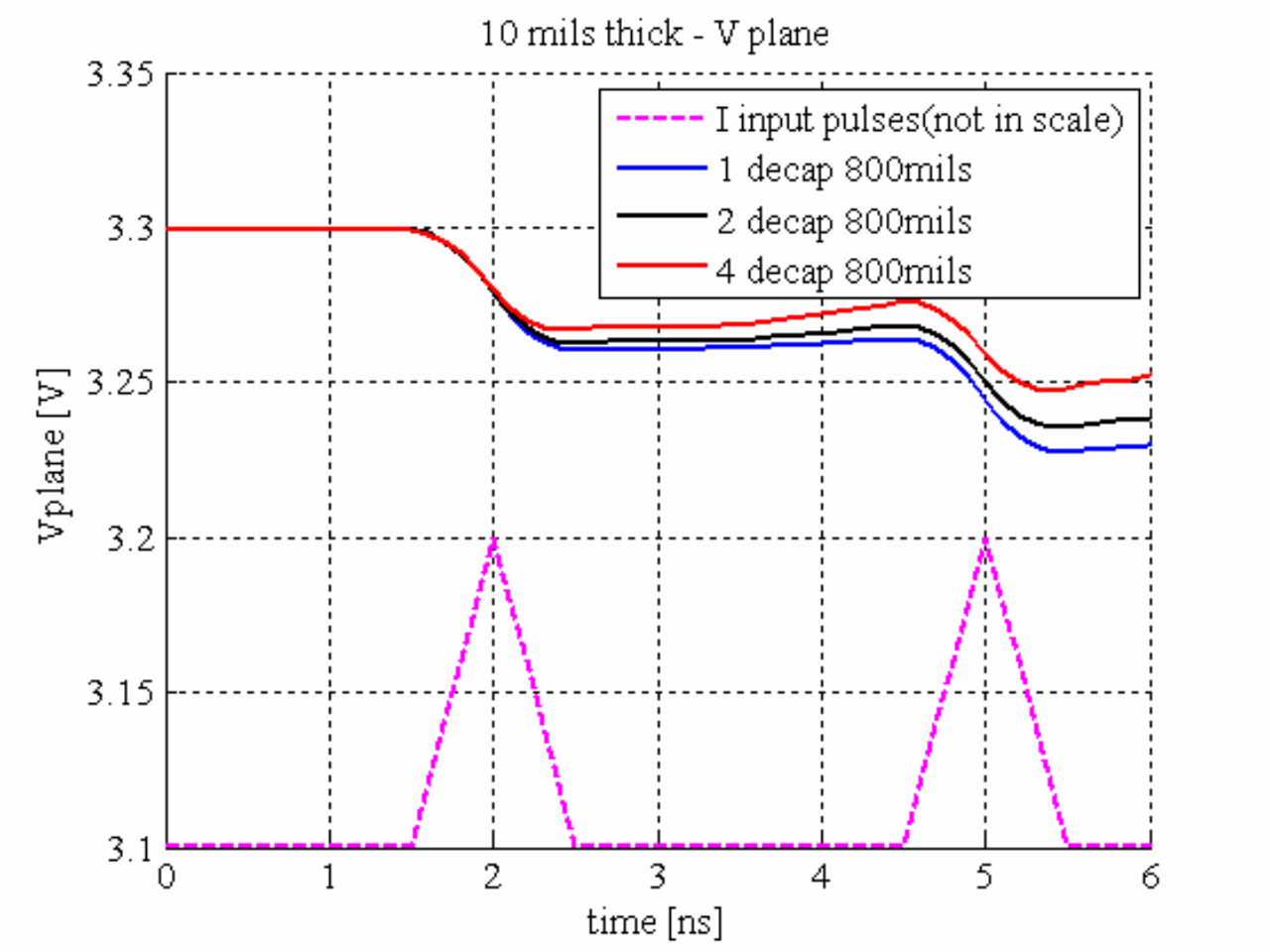
The decap locations are 800mils, 1200mils, 2700mils from the power pin

(power-ground pins at IC center)

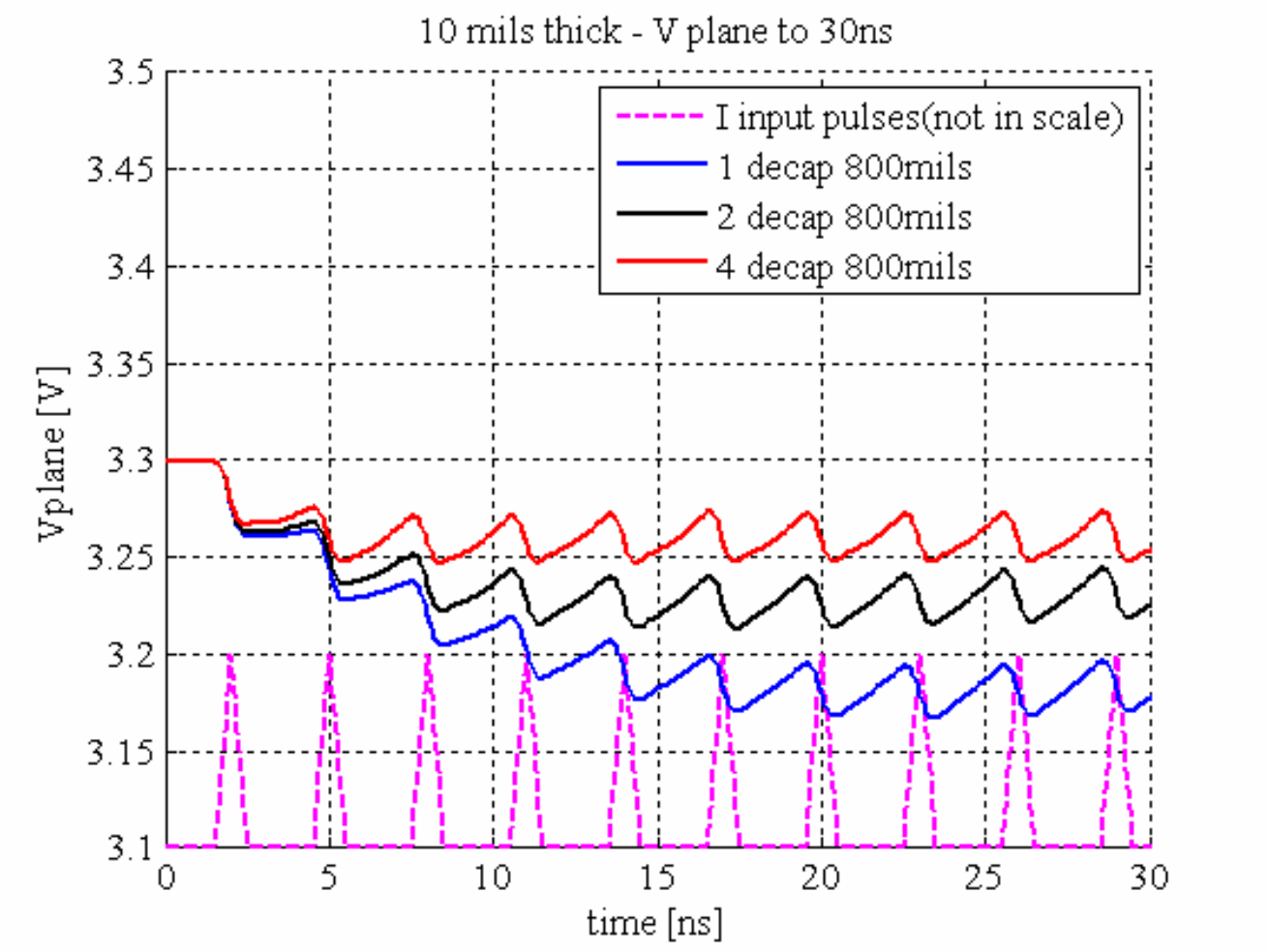
- C=0.25uF
- ESL=0.5nH
- ESR=1Ω



Constant Capacitance 800 mil Distance



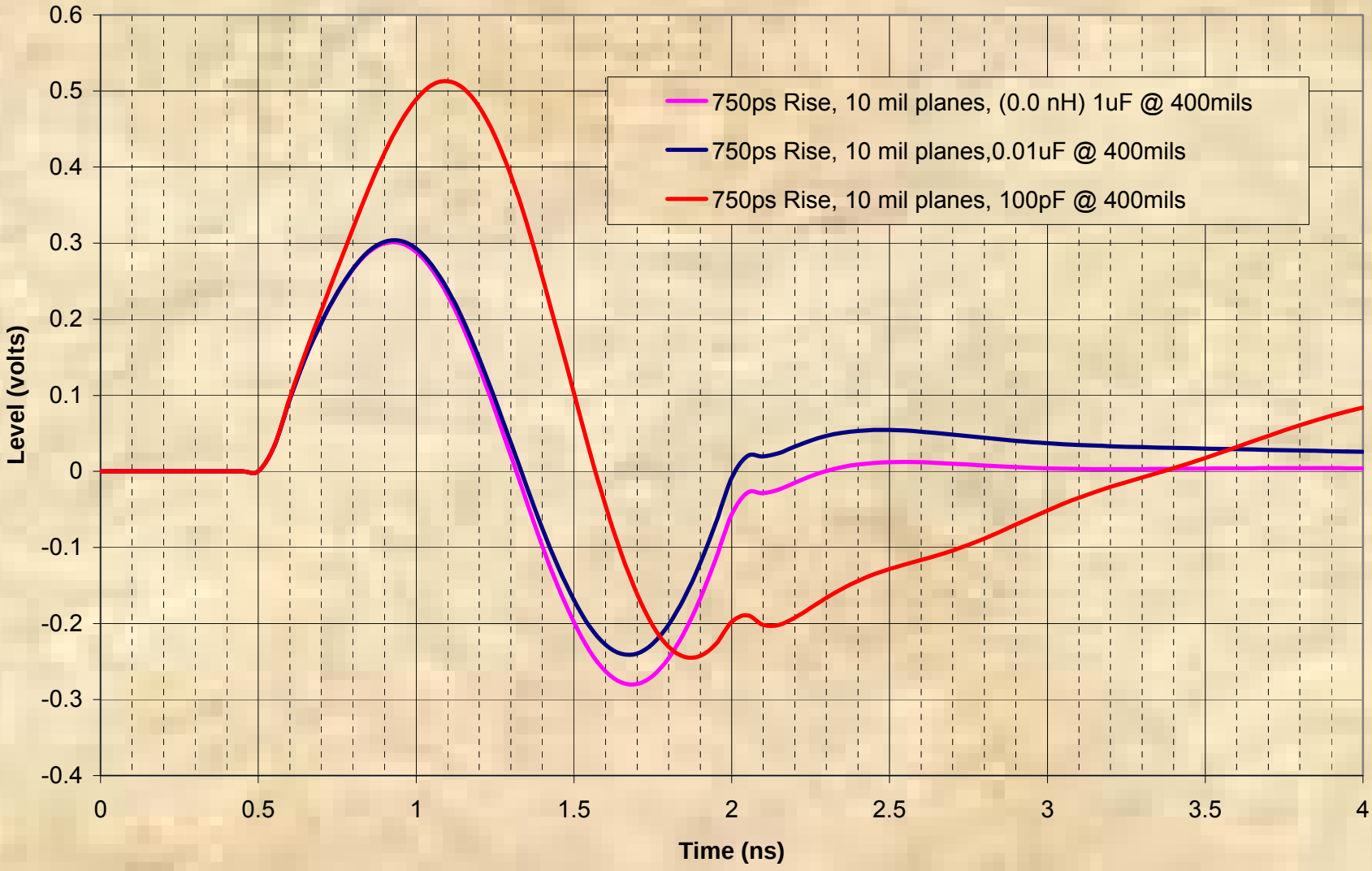
Constant Capacitance
800 mil Distance



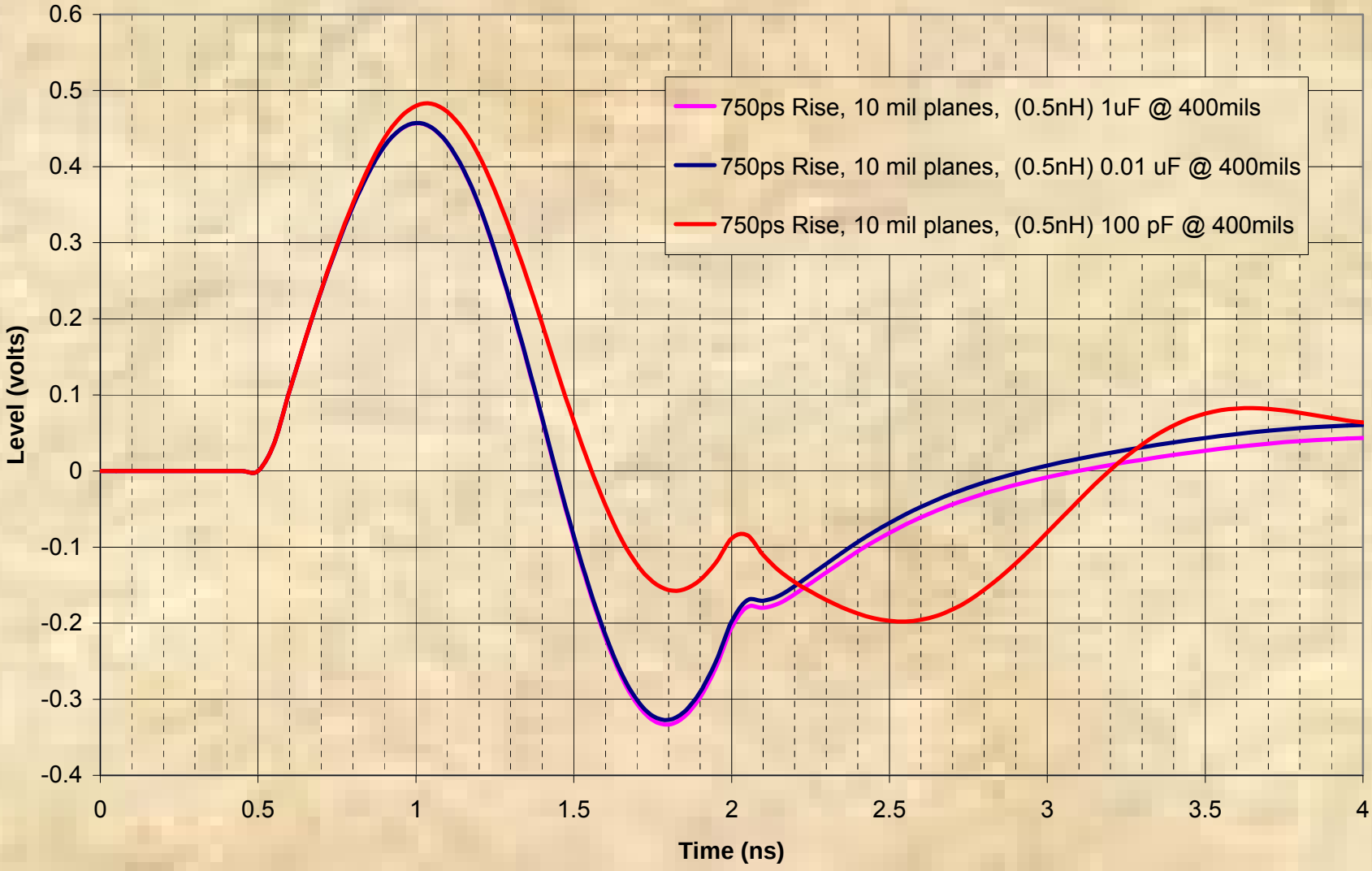
Effect of Capacitor Value??

- Need enough charge to supply need
- Depends on connection inductance

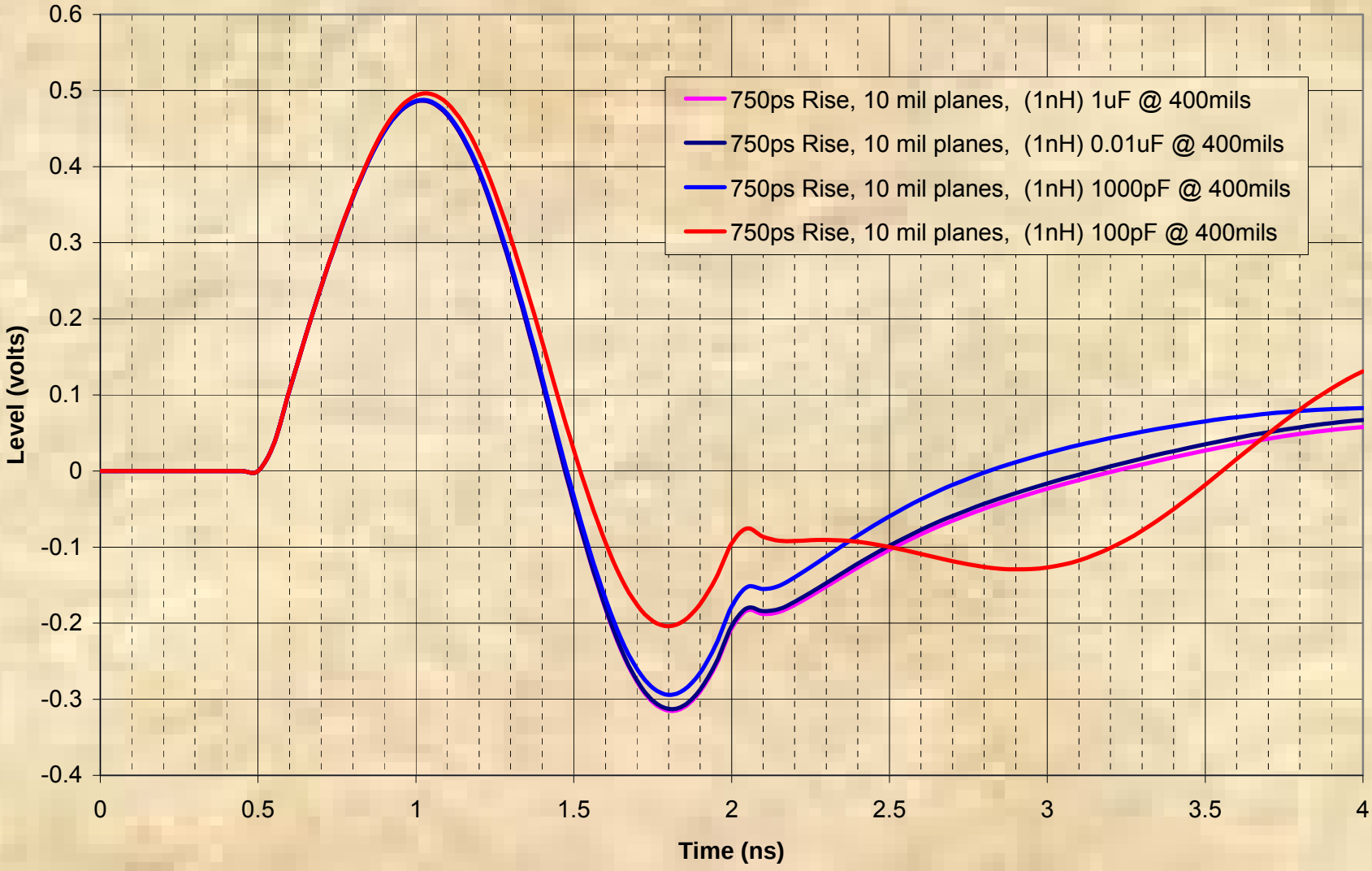
Time Domain Noise Voltage Across Simulated IC Power/GND Pin (1 amp)
Single Capacitor (with No L) with Various Capacitor Values



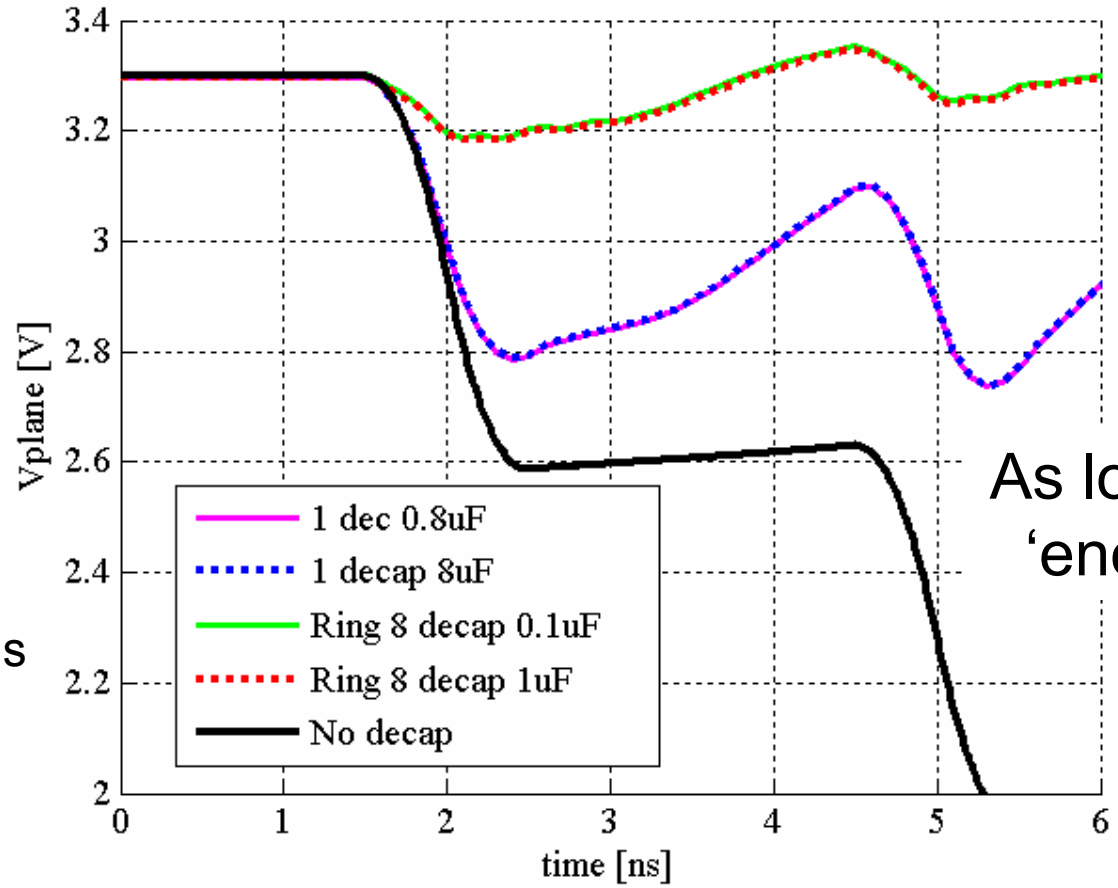
Time Domain Noise Voltage Across Simulated IC Power/GND Pin (1 amp)
Single Capacitor (with 0.5 nH Connection L) with Various Capacitor Values



Time Domain Noise Voltage Across Simulated IC Power/GND Pin (1 amp)
Single Capacitor (with 1 nH Connection L) with Various Capacitor Values



Noise Voltage is INDEPENDENT of Amount of Capacitance!



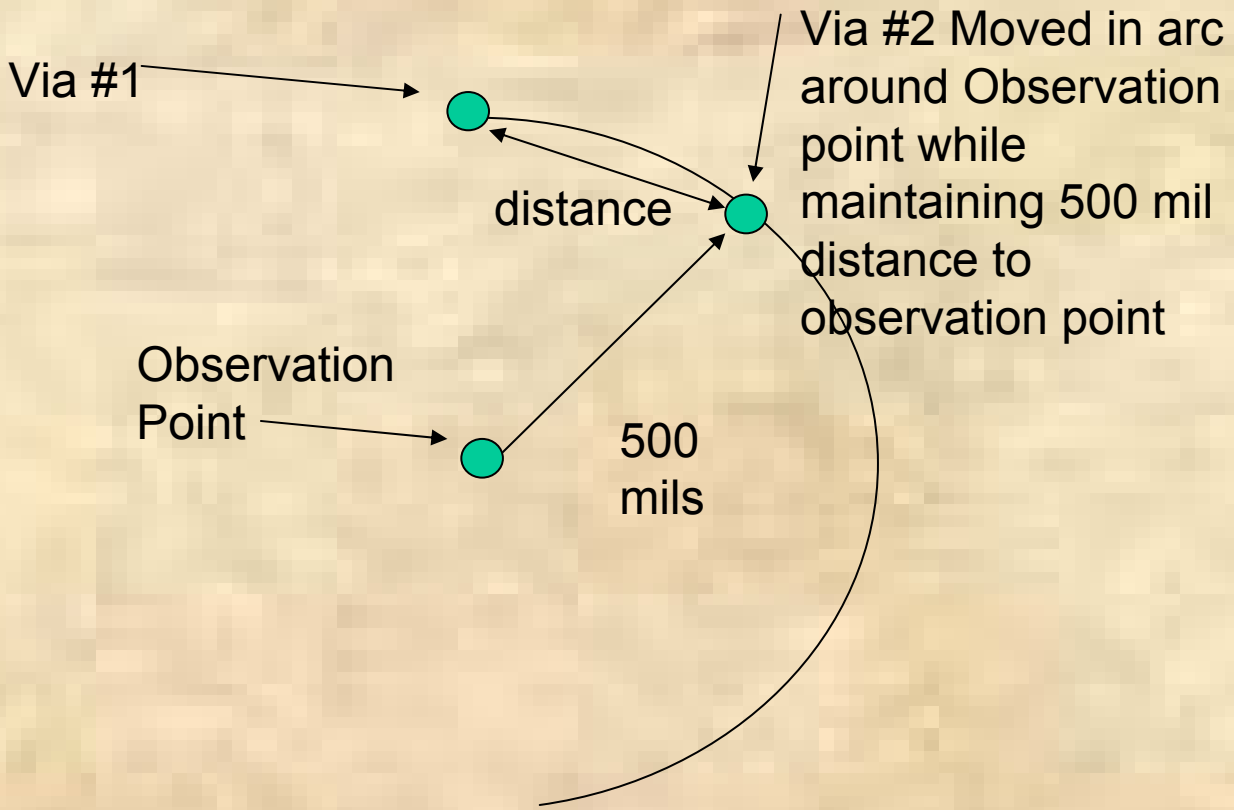
Dist=400 mils

ESR=30mOhms

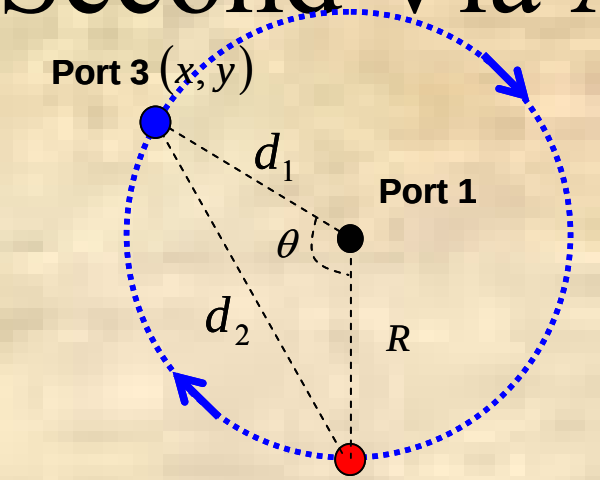
ESL=0.5nH

As long as there is 'enough' charge

What Happens if a 2nd Decoupling Capacitor is placed near the First Capacitor?



Second Via Around a circle



$d_1 = R$

$d_2 = 2R\sin\frac{\theta}{2}$

R: distance between Port 1 and Port 2 in mil

r: radius for all ports in mil

d: thickness of dielectric layer in mil

d1: distance between Port 3 and Port 1 in mil

d2: distance between Port 2 and Port 3 in mil

theta: angle as shown in the figure in degree

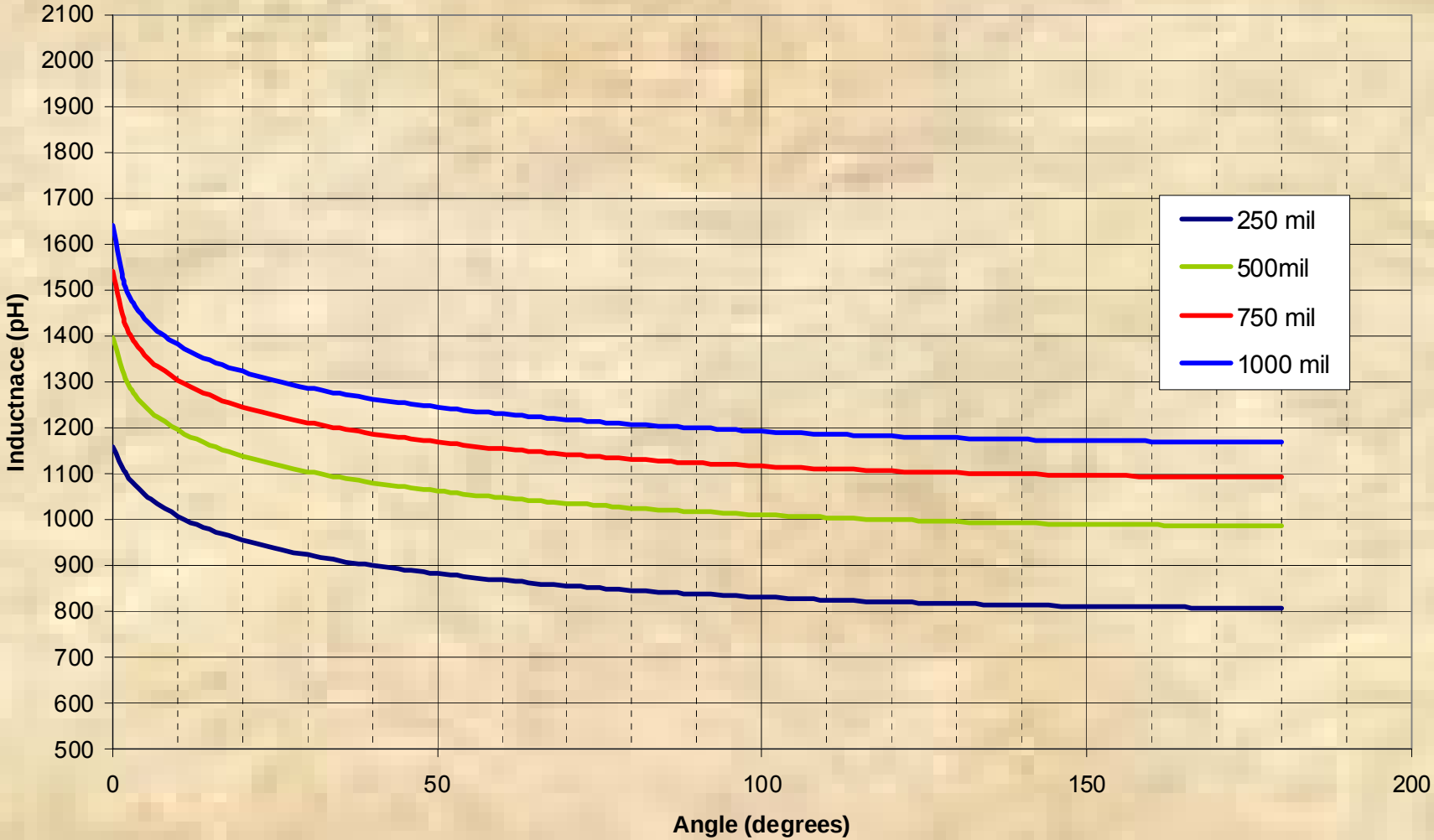
$$\frac{\mu d}{4\pi}\ln\left(\frac{(R+r)^2(d_1+r)^2}{r^3(d_2+r)}\right)-\frac{\mu d}{4\pi}\frac{\ln^2\left(\frac{d_1+r}{R+r}\right)}{\ln\left(\frac{d_2+r}{r}\right)}$$

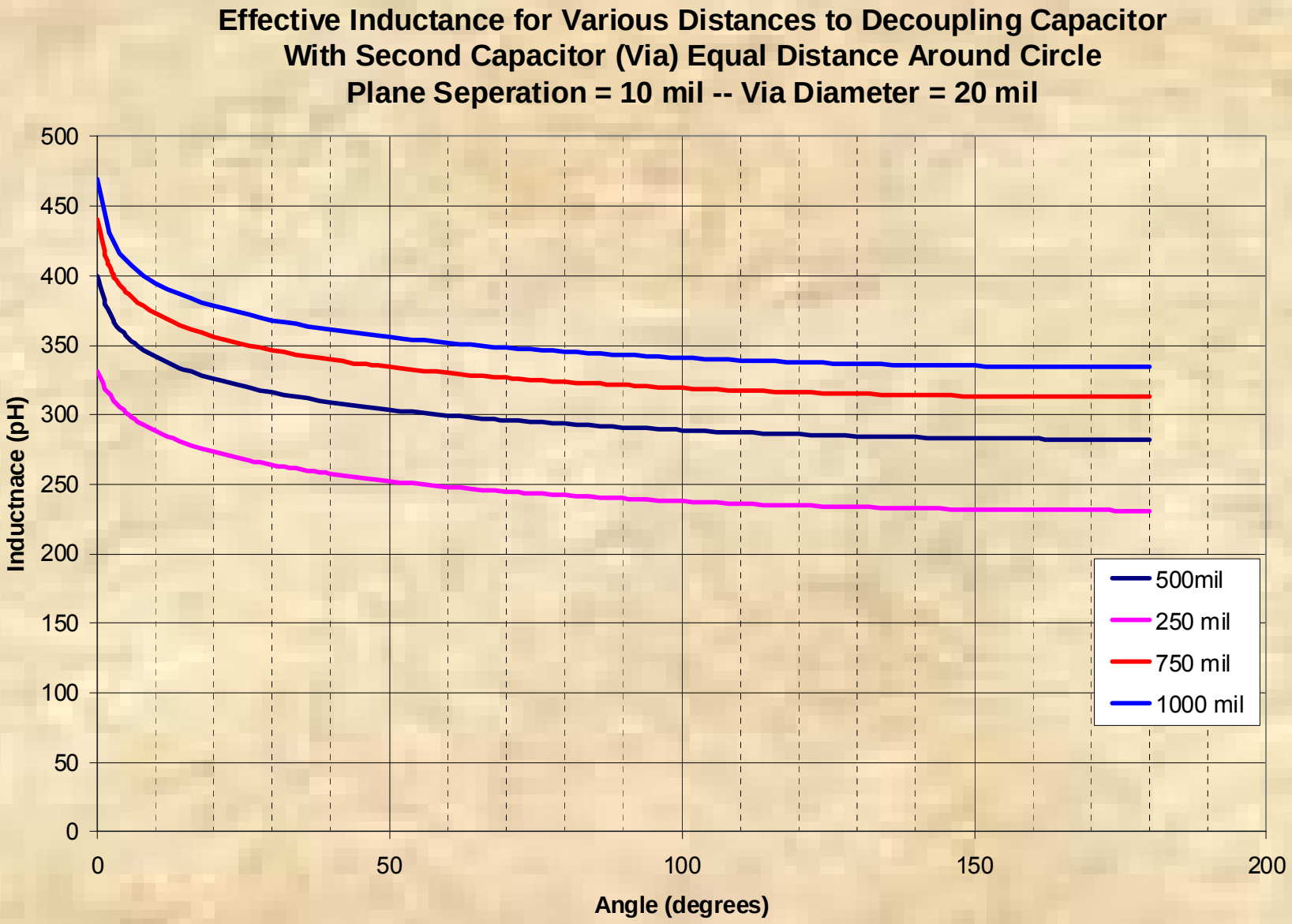
$$=\frac{\mu d}{4\pi}\ln\left(\frac{(R+r)^4}{(2R\sin(\theta/2)+r)r^3}\right)$$

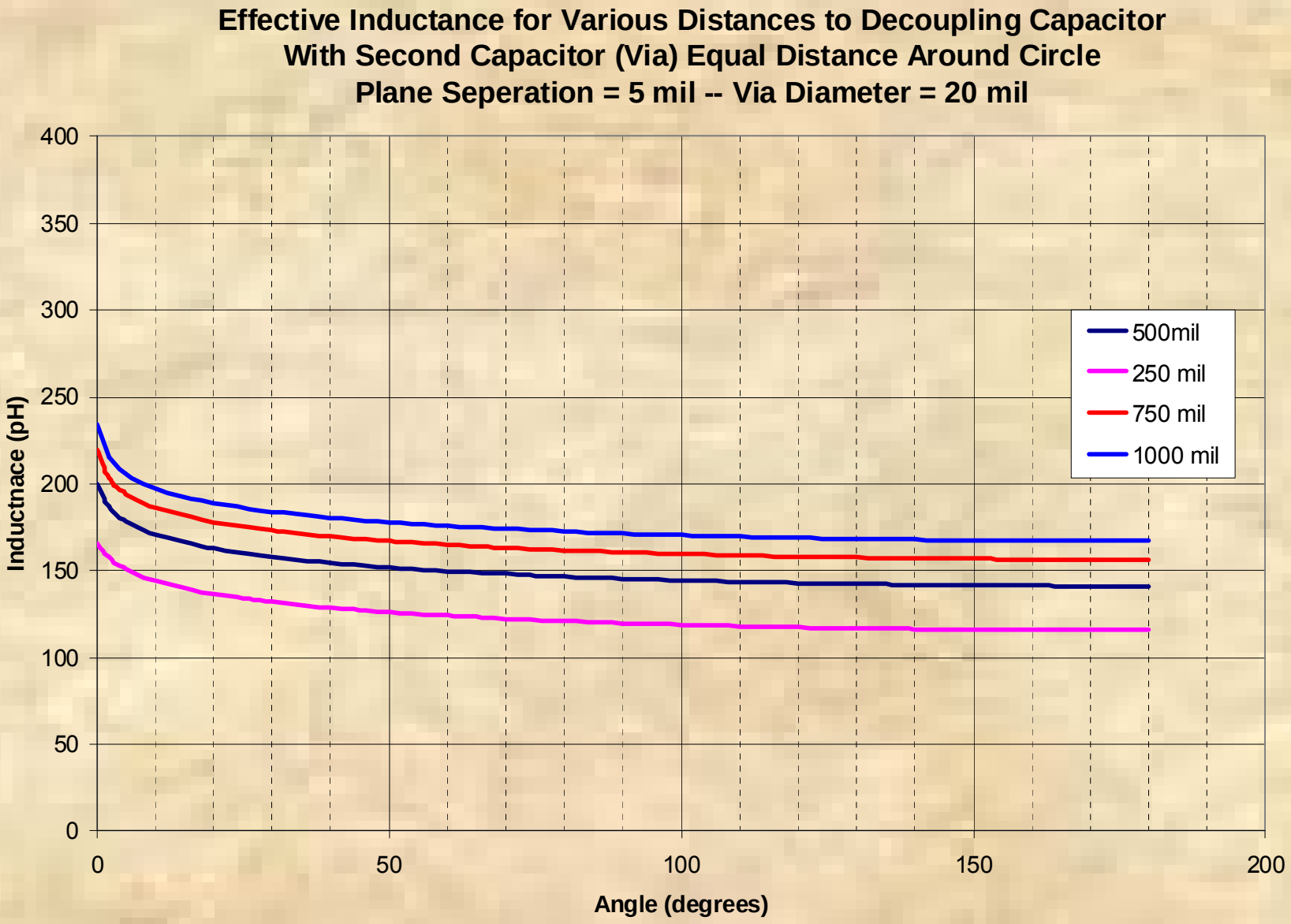
Courtesy of Jingook Kim, Jun Fan, Jim Drewniak

Missouri University of Science and Technology

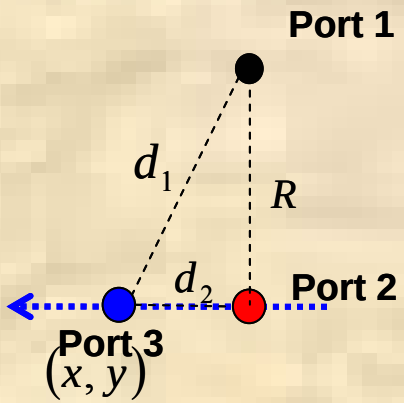
Effective Inductance for Various Distances to Decoupling Capacitor
With Second Capacitor (Via) Equal Distance Around Circle
Plane Seperation = 35 mil -- Via Diameter = 20 mil




Effective Inductance for Various Distances to Decoupling Capacitor
With Second Capacitor (Via) Equal Distance Around Circle
Plane Seperation = 10 mil -- Via Diameter = 20 mil
Inductnace (pH)
500
450
400
350
300
250
200
150
100
50
0
0
50
100
150
200
Angle (degrees)
500mil
250 mil
750 mil
1000 mil


Effective Inductance for Various Distances to Decoupling Capacitor
With Second Capacitor (Via) Equal Distance Around Circle
Plane Seperation = 5 mil -- Via Diameter = 20 mil
Inductnace (pH)
400
350
300
250
200
150
100
50
0
0
50
100
150
200
Angle (degrees)
500mil
250 mil
750 mil
1000 mil

Second Via Along Side



$$d_1 = \sqrt{R^2 + {d_2}^2}$$

R: distance between Port 1 and Port 2 in mil

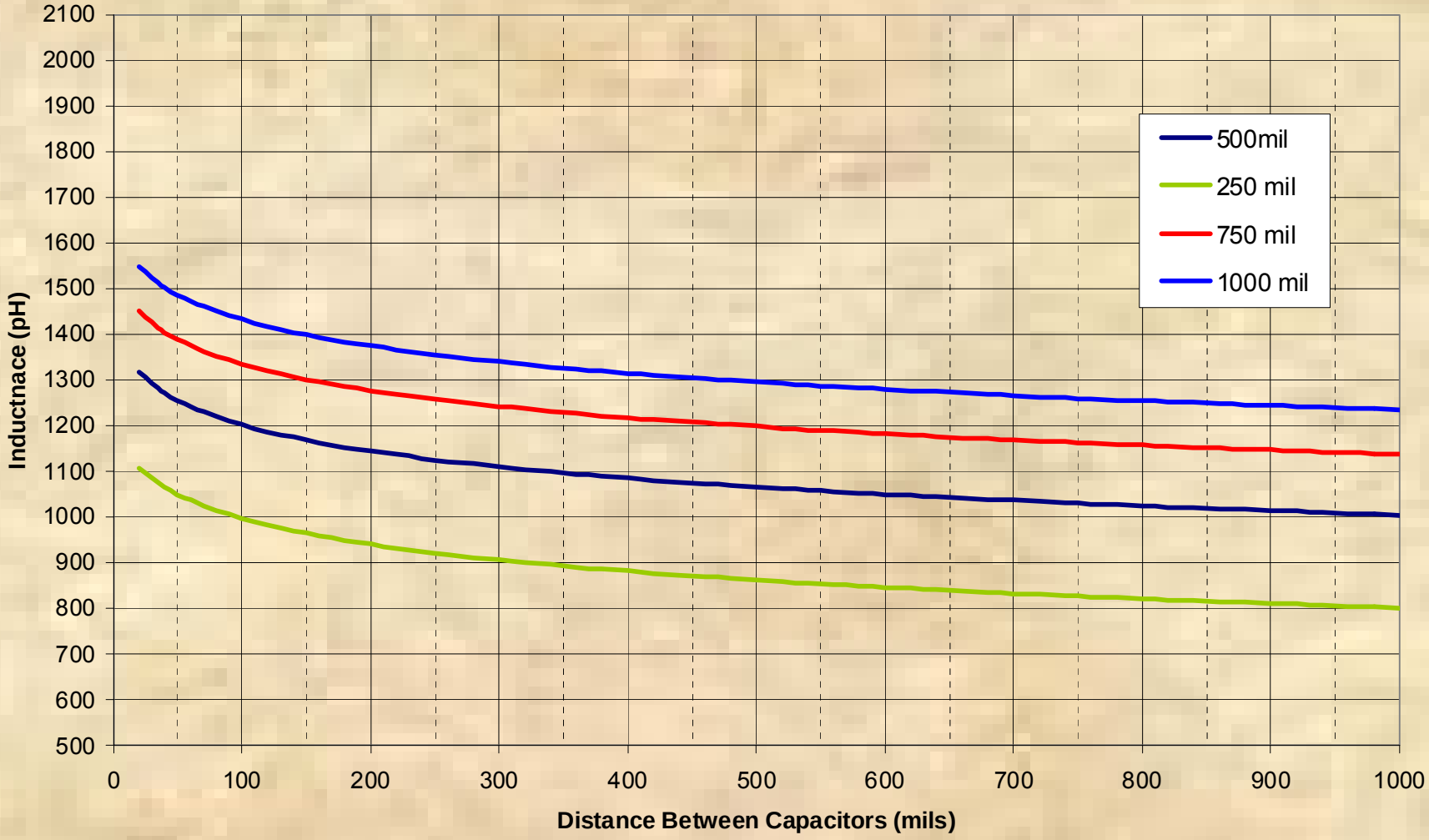
r: radius for all ports in mil

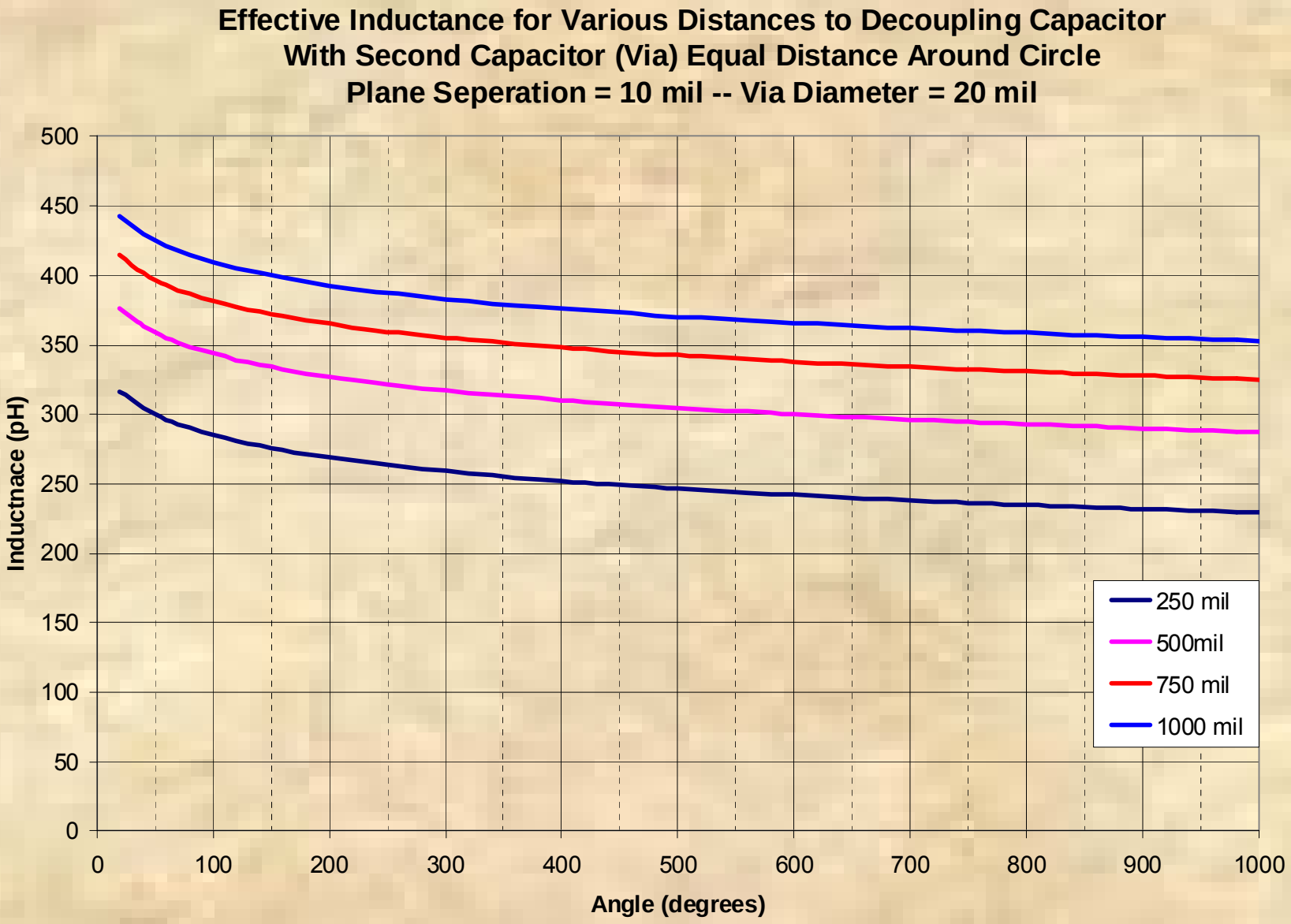
d: thickness of dielectric layer in mil

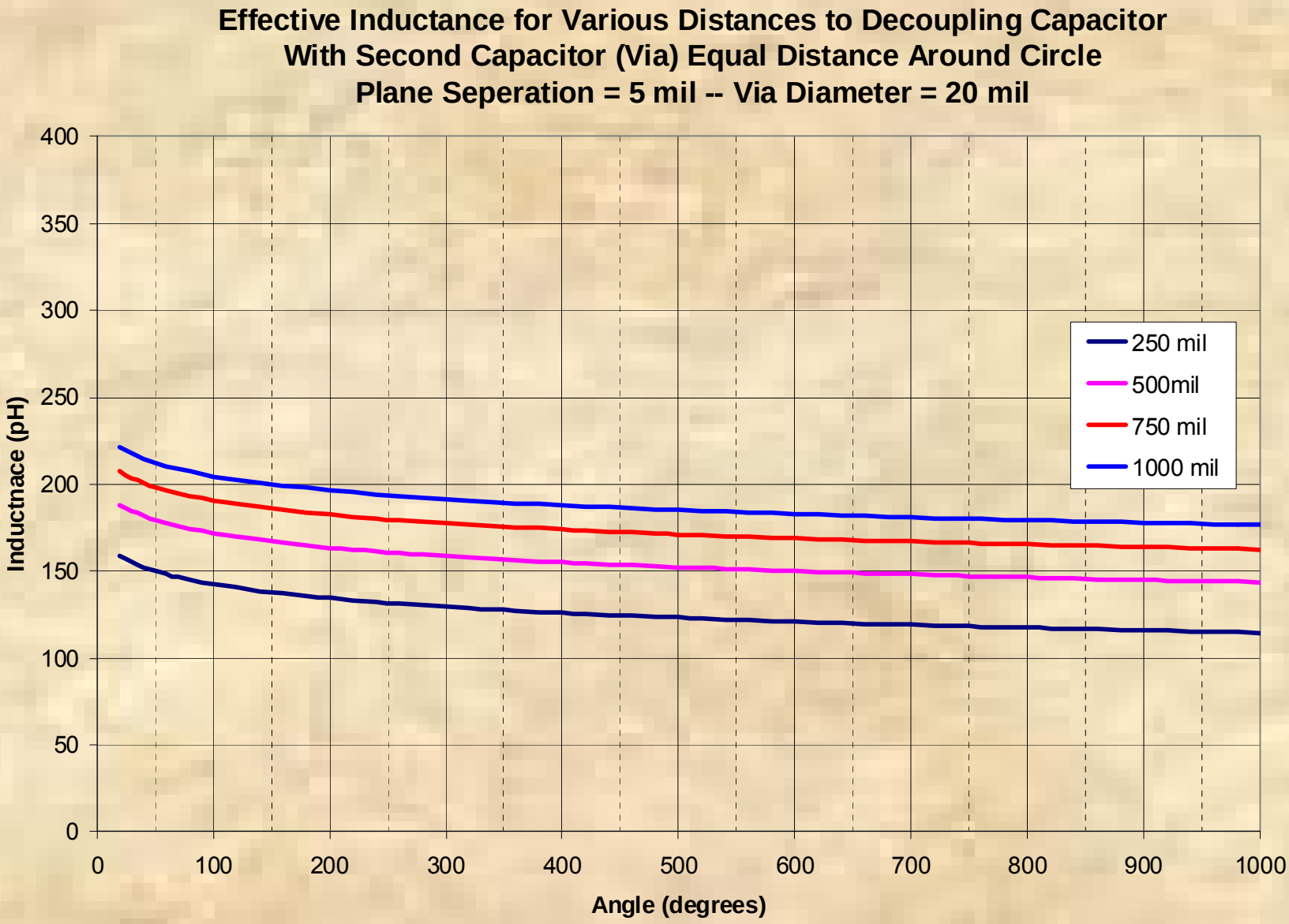
d1: distance between Port 3 and Port 1 in mil

d2: distance between Port 2 and Port 3 in mil

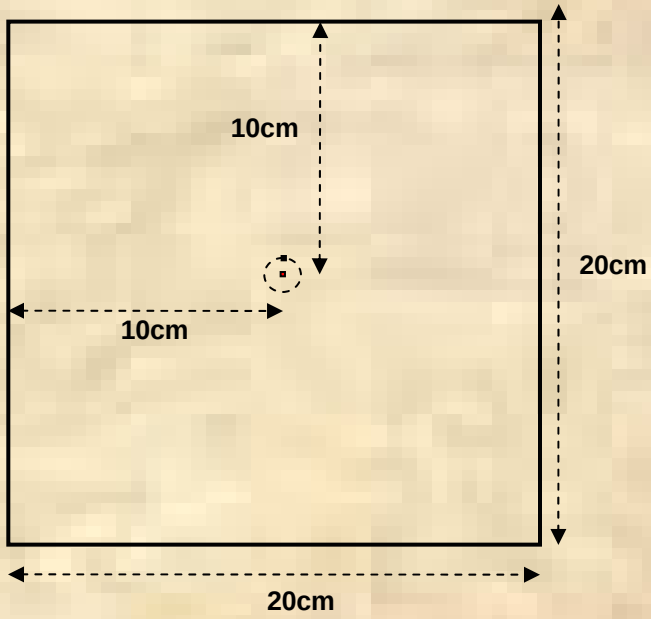
Effective Inductance for Various Distances to Decoupling Capacitor With Second Capacitor (Via) Positioned Adjacent to First Capacitor Plane Seperation = 35 mil -- Via Diameter = 20 mil



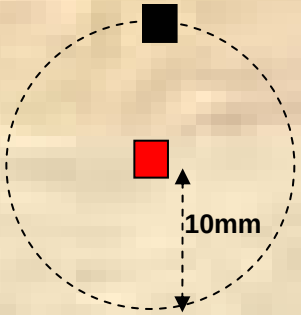

Effective Inductance for Various Distances to Decoupling Capacitor
With Second Capacitor (Via) Equal Distance Around Circle
Plane Seperation = 10 mil -- Via Diameter = 20 mil
Inductnace (pH)
500
450
400
350
300
250
200
150
100
50
0
0
100
200
300
400
500
600
700
800
900
1000
Angle (degrees)
250 mil
500mil
750 mil
1000 mil


Effective Inductance for Various Distances to Decoupling Capacitor
With Second Capacitor (Via) Equal Distance Around Circle
Plane Seperation = 5 mil -- Via Diameter = 20 mil
Inductnace (pH)
400
350
300
250
200
150
100
50
0
0
100
200
300
400
500
600
700
800
900
1000
Angle (degrees)
250 mil
500mil
750 mil
1000 mil

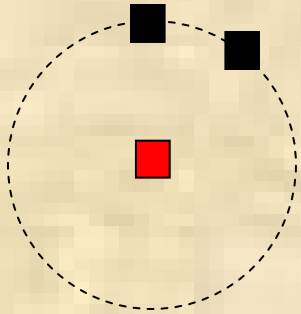
Understanding Inductance Effects and Proximity



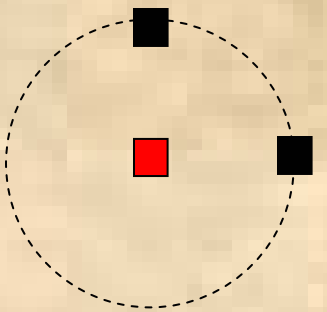
1 via



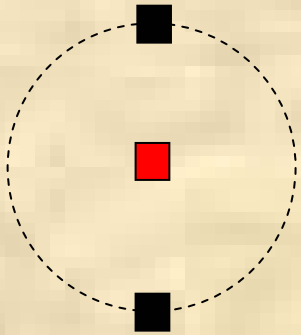
2 via with degree 30°



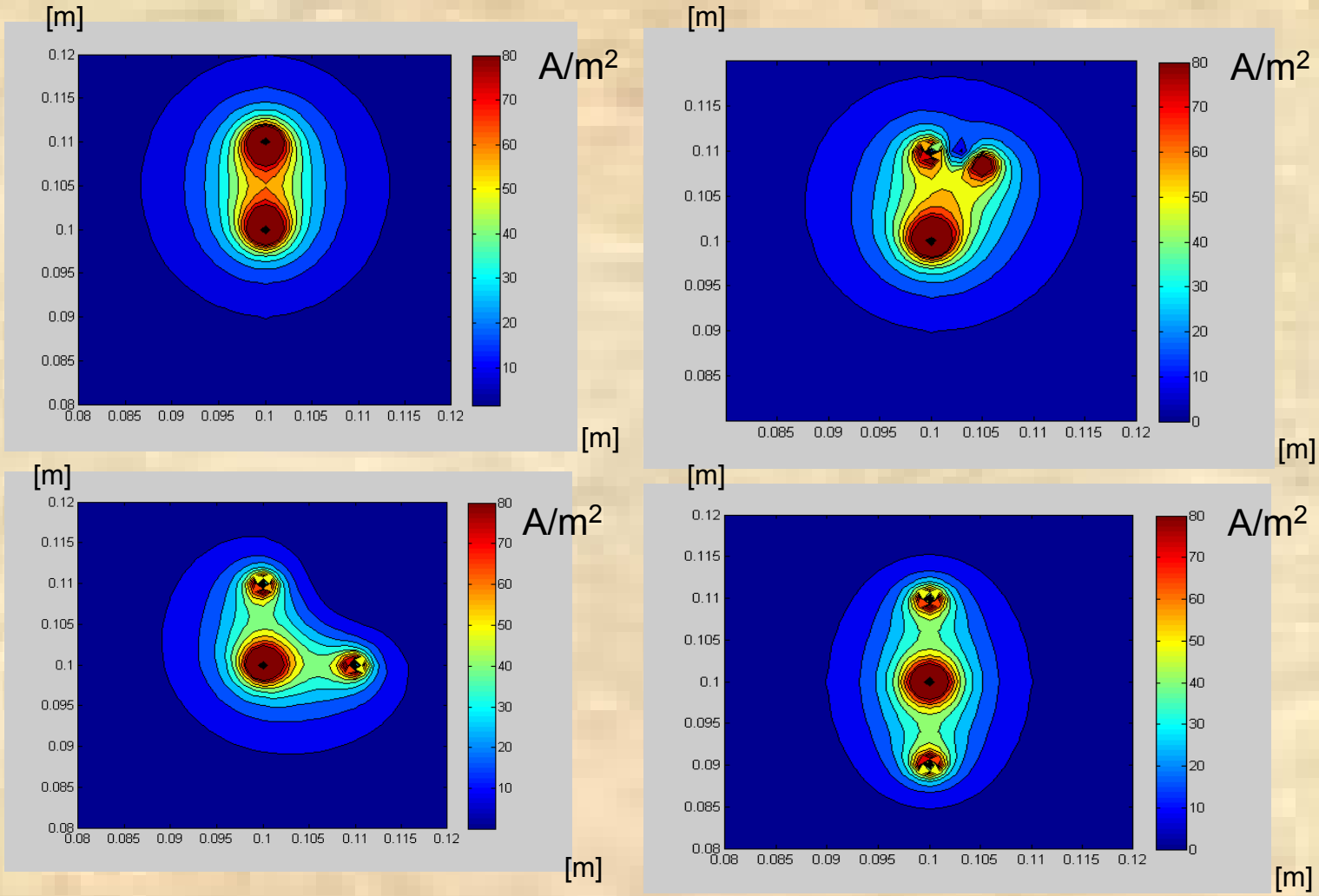
2 via with degree 90°



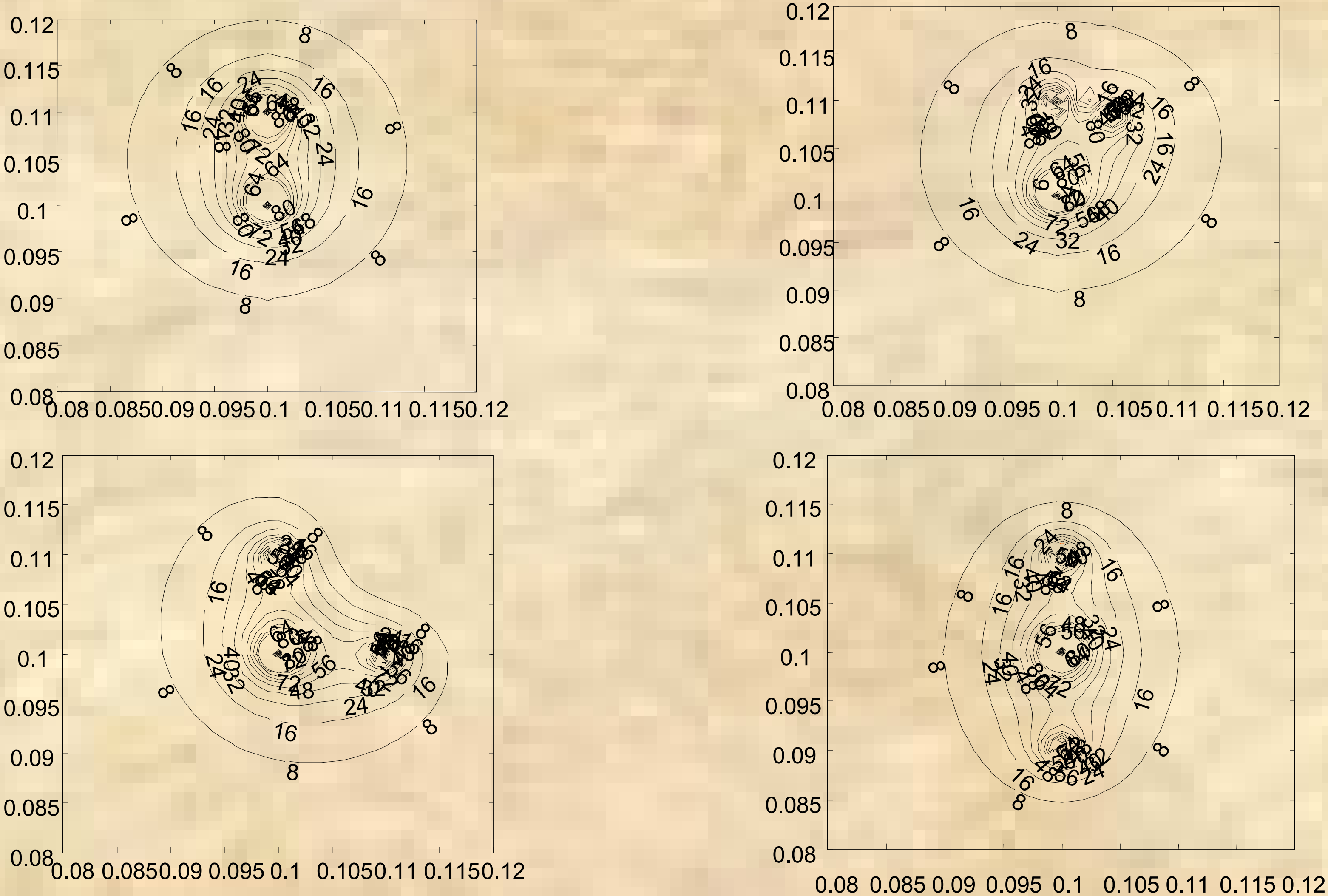
2 via with degree 180°



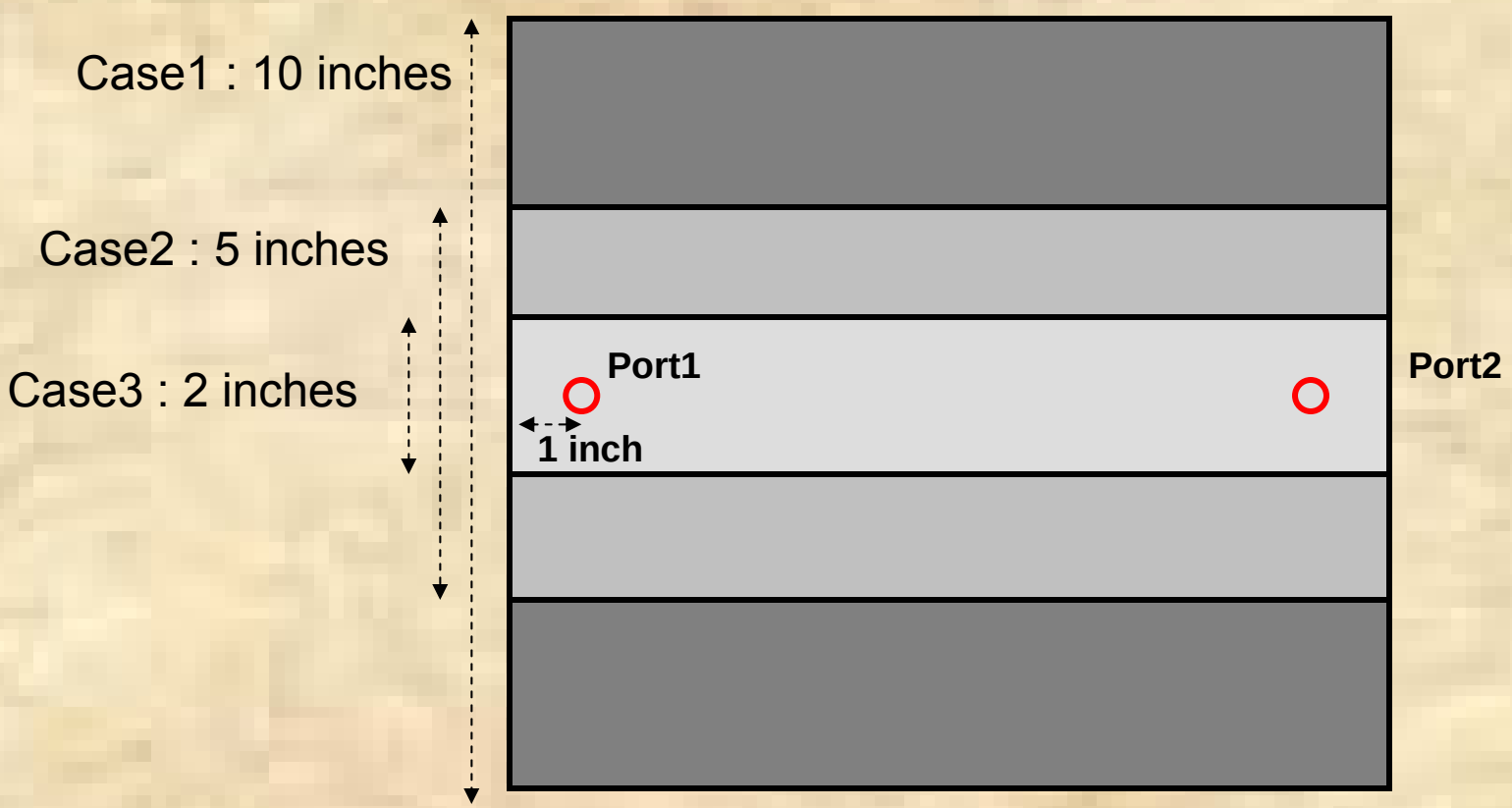
Current Density



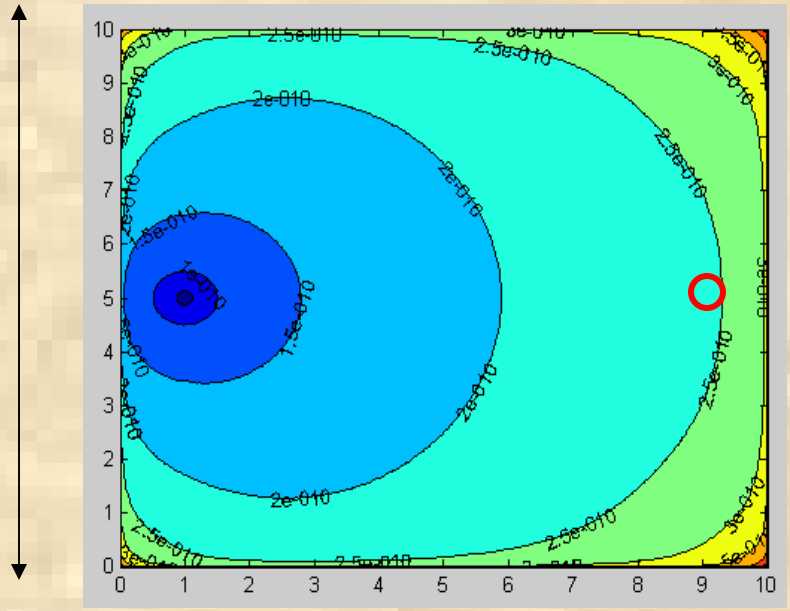
Current Density in Planes



Effect of Plane width on Inductance

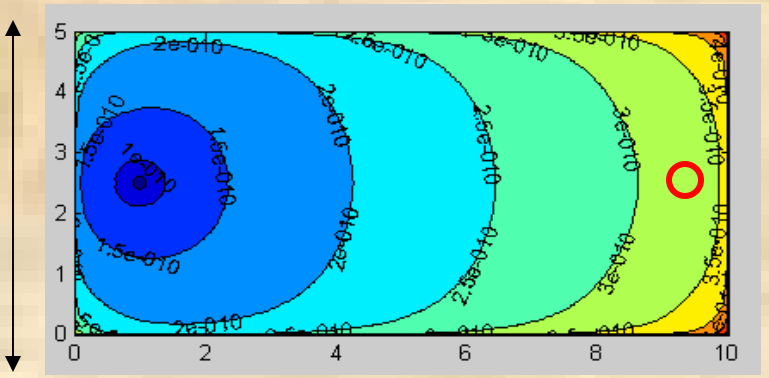


Case1 : 10 inches



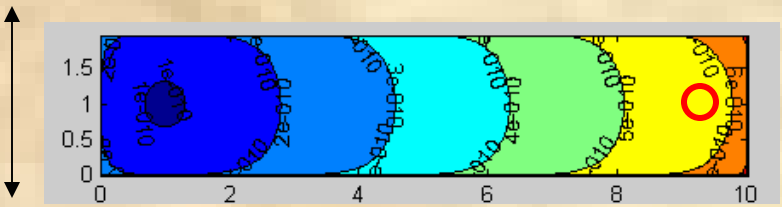
~ 250pH

Case2 : 5 inches



~ 330pH

Case2 : 2 inches



~ 560pH

Observations

- Added via (capacitor) does not lower effective inductance to 70-75% of original single via case
- Thicker dielectric results in higher inductance
- Normalizing inductance to single via case gives same curve for all dielectric thicknesses

Decoupling Analysis Summary

- EMC Frequency Domain analysis
  - Steady-state conditions
  - Transfer function across the board
  - Measurements and simulations agree well
  - Distance of capacitors from ASIC load does not change steady-state impedance
- Charge Delivery Time-Limited analysis
  - Using equivalent SPICE circuit from simulations
  - Current from capacitors change significantly as capacitor moves further away from ASIC
  - Noise at ASIC pins increase significantly as capacitor moves further away from ASIC
  - Steady-state frequency domain analysis not sufficient for charge delivery design of decoupling capacitors

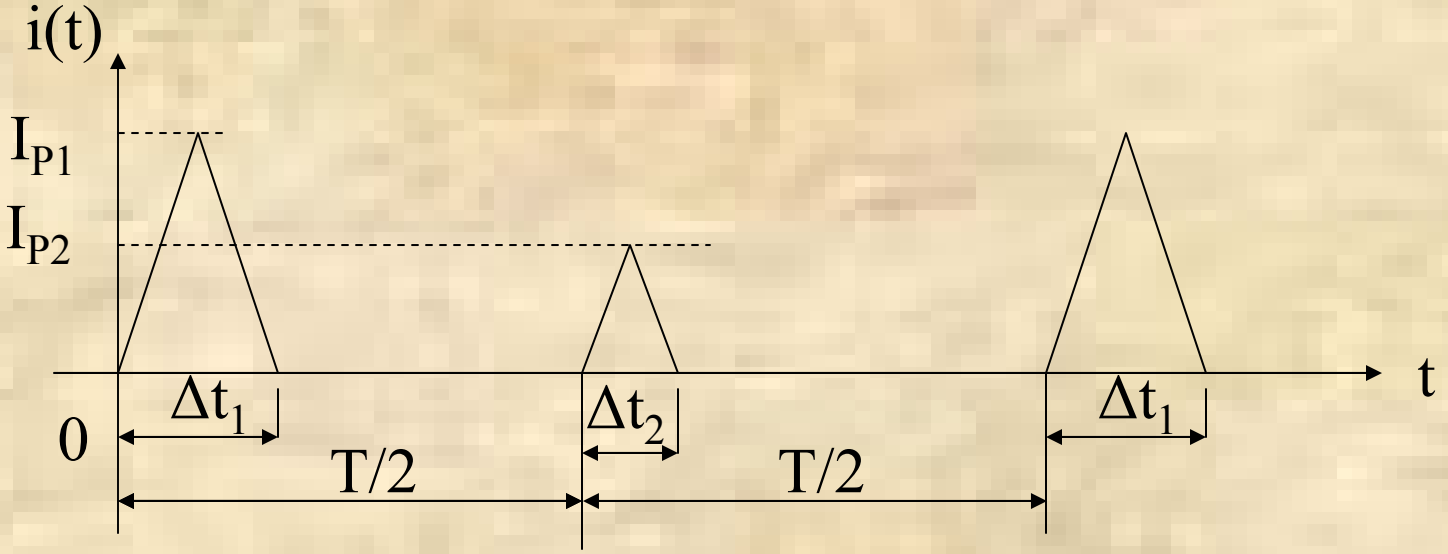
Two Major Questions

- ✓How will structure respond?
- What is the source of the noise?
  - CURRENT!

Predicting the Source of Decoupling Noise

- What is the source?
- ICs need two types of current
  - Current for the I/O drivers
  - "Core" current
    - Current that does not go out the I/O drivers
- On-going research with Prof Jim Drewniak at UMR

Modeling the Power Current Waveform For Clock Buffer/Driver



- I_{p2} = shoot through current
- I_{p1} = I/O current + core current

Core Current

$$I_{p2} = \frac{C_{pd} * m * V_{cc}}{\Delta t_2}$$

- C_{pd} is specified for Clock drivers/buffers
- m is number of I/O drivers
- $\Delta t_2 = t_r + t_f$

I/O Driver Current

- Simple Capacitive Load method
- C_L = 10 pF is typical
- n = number of loads
- $\Delta t = t_r$

$$I_L = \frac{C_L n V_{cc}}{\Delta t / 2}$$

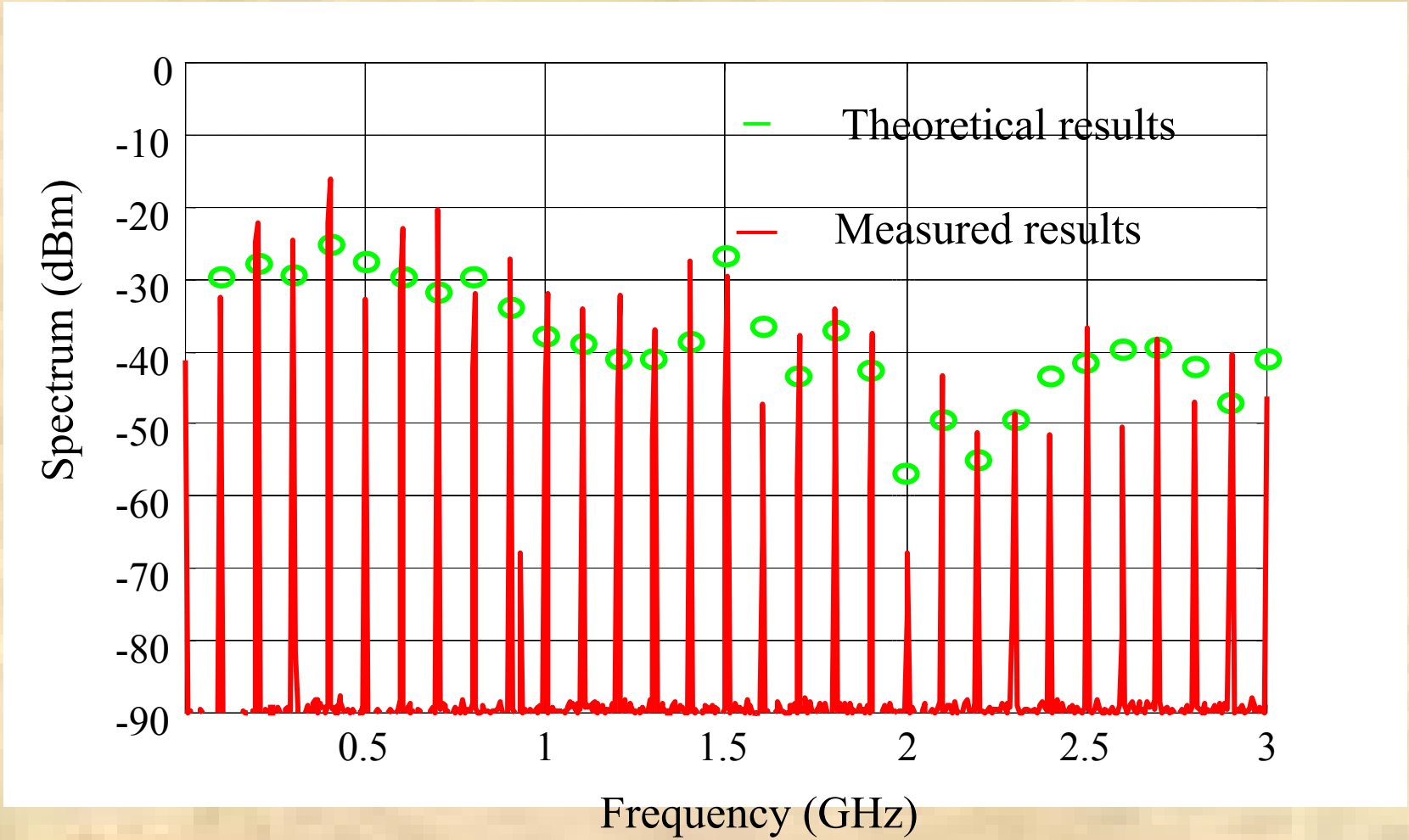
More Accurate I/O Driver Current

- Use Signal Integrity tools to find *current* waveform
  - Hyperlynx
  - Spectraquest
  - SPICE

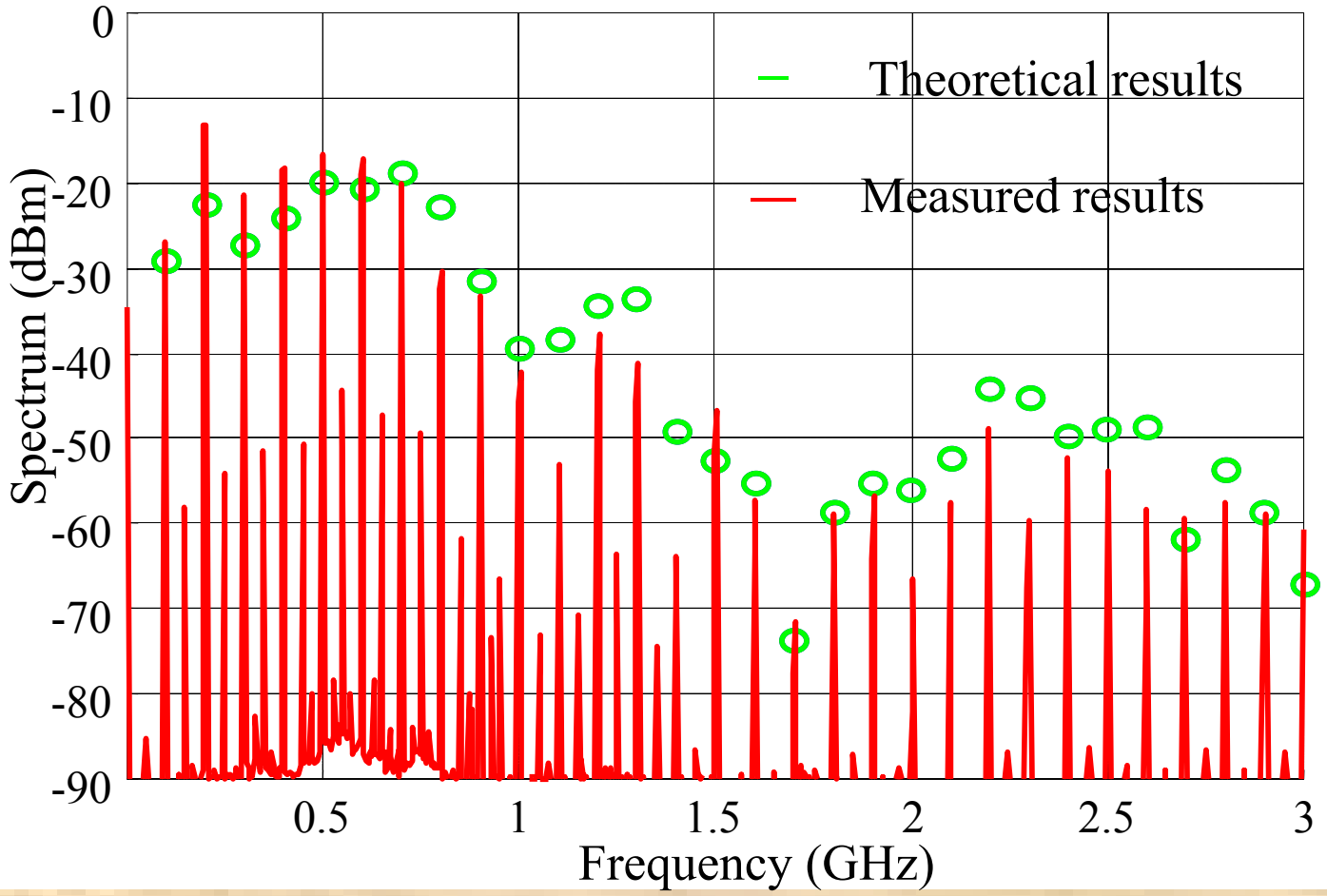
Example for Clock Buffers

	MPC905	MPC946	CDC208
C_{PD}	19.5 pF per output	25 pF per output	96 pF per bank(enable) or 12 pF per bank(disable)
V_{CC}	3.3 V	3.3 V	5 V
m (number of outputs)	6	10	8 or 4
n (number of loads)	6	8	8 or 4
f (operating frequency)	100 MHz	100 MHz	60 MHz
t_r(MAX)	4 V/nS	1.0 nS	10 nS/V

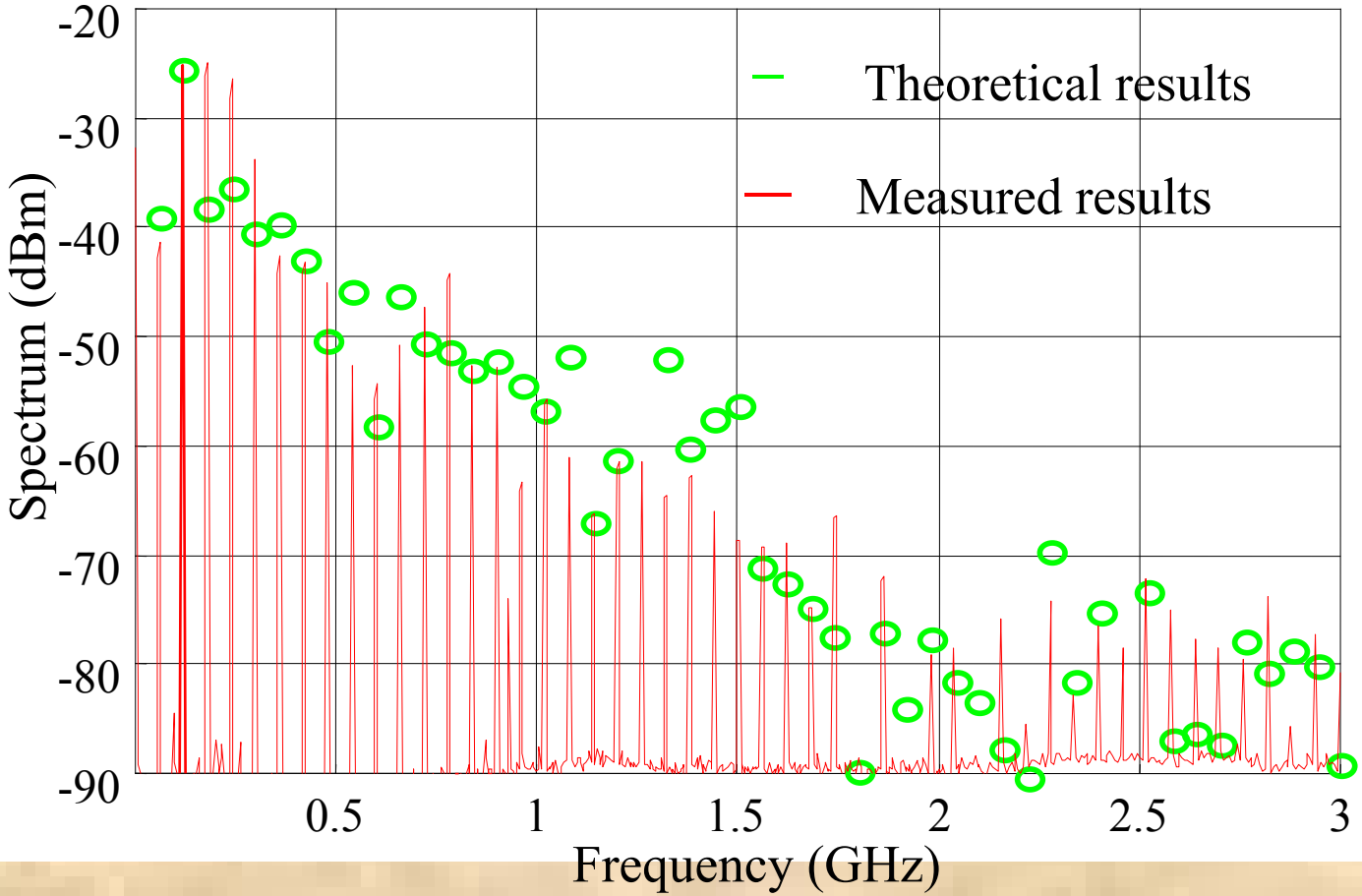
Motorola MPC905 Results



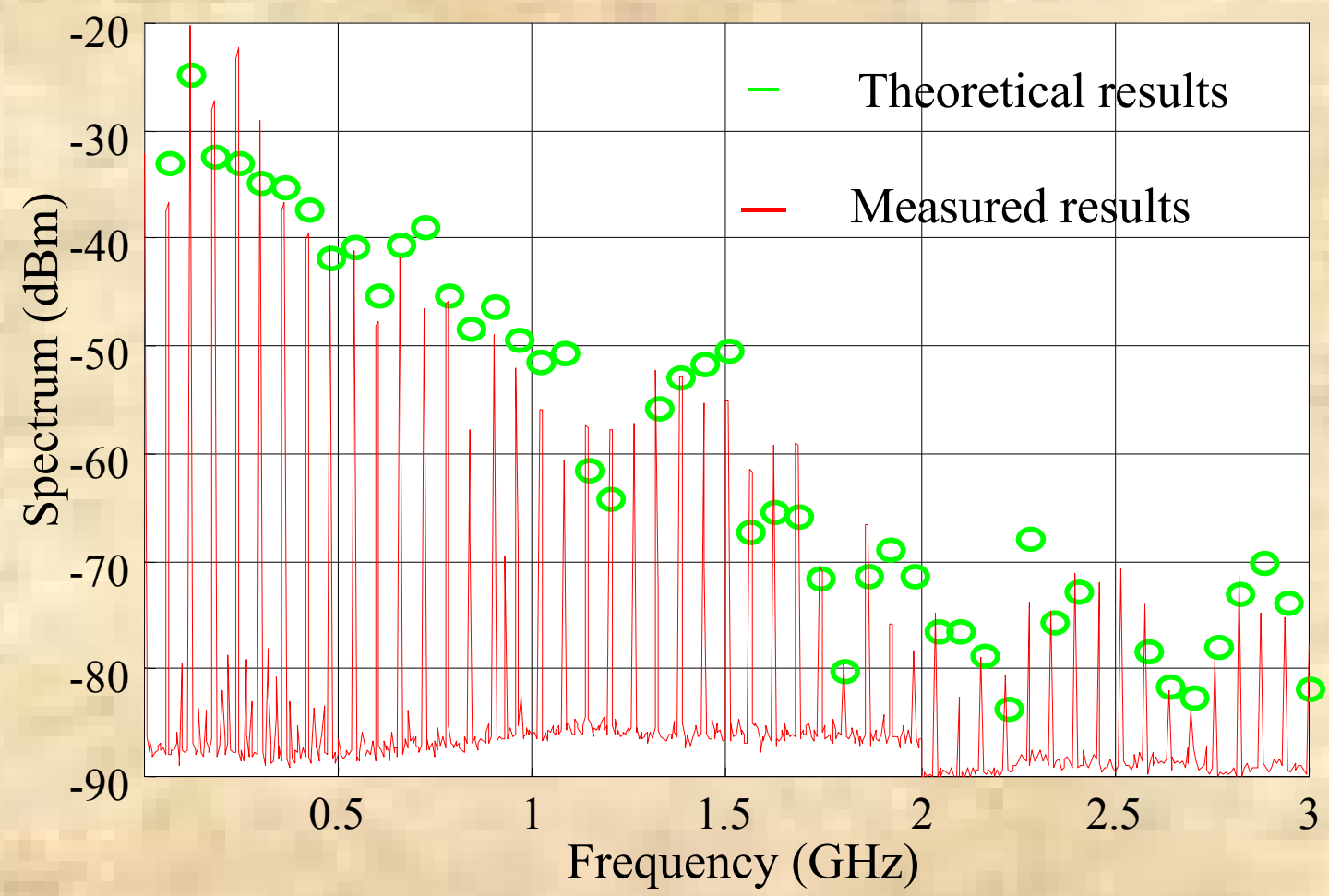
Motorola MPC946 Results



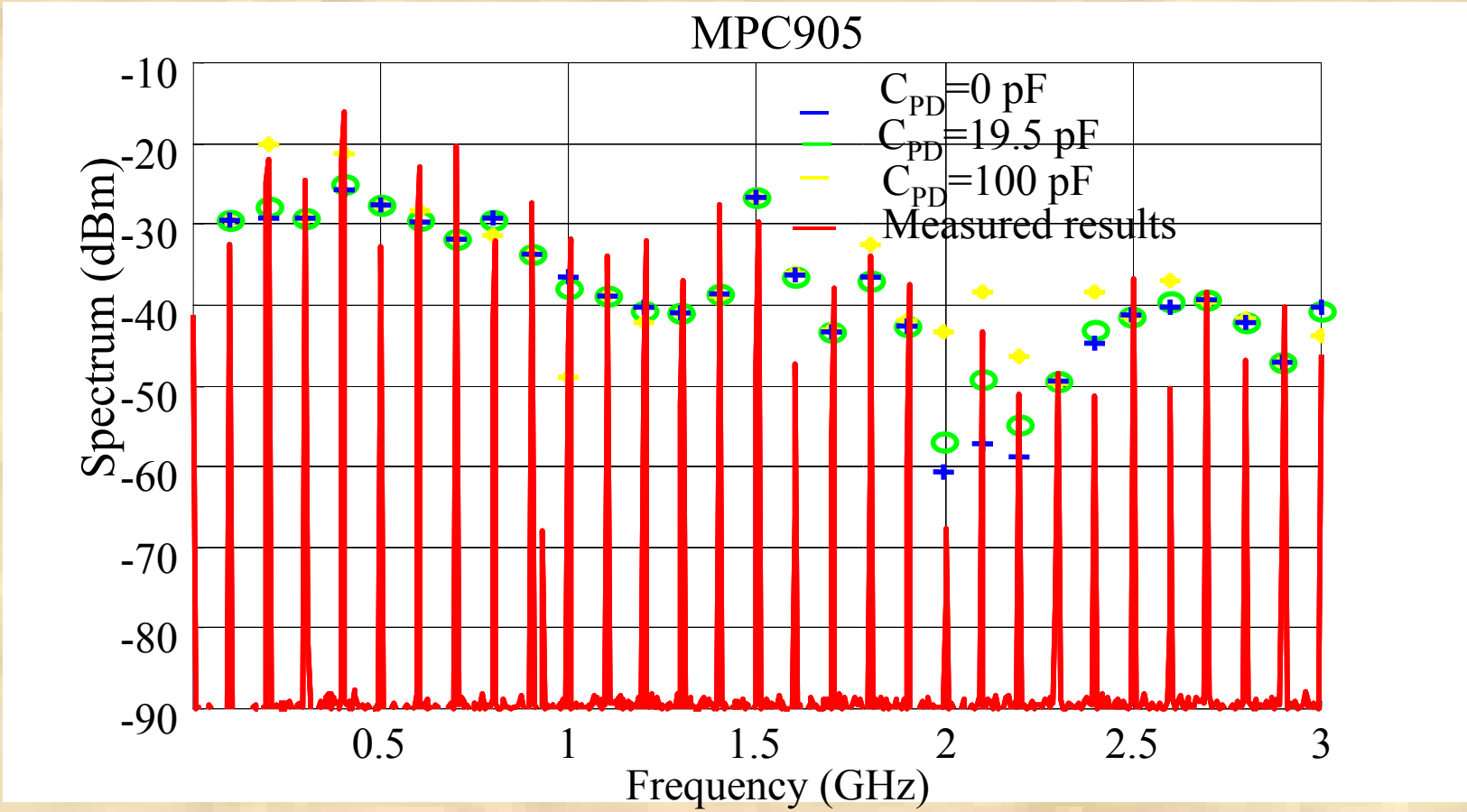
CDC208 (4 loads)



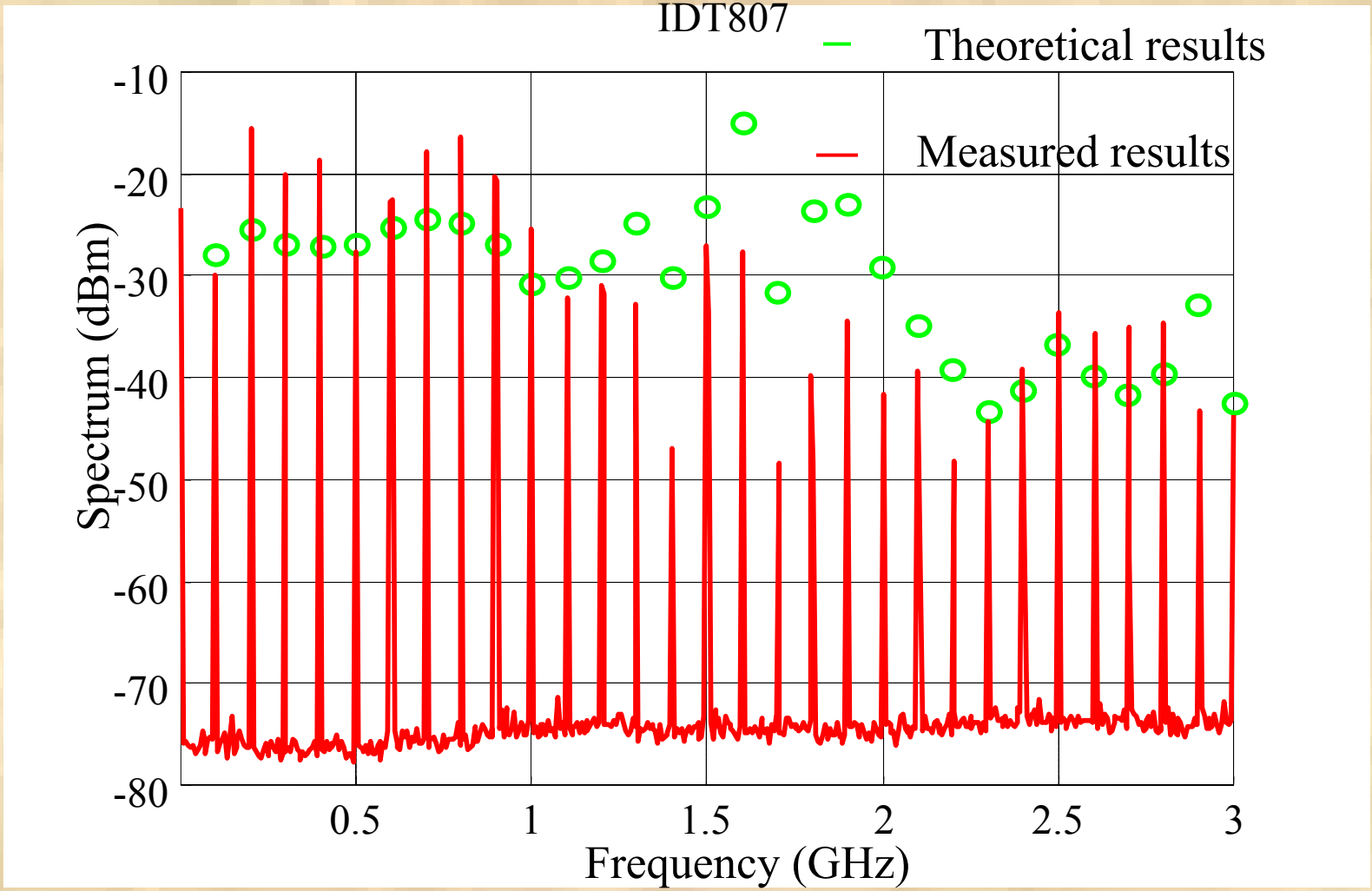
CDC208 (8 loads)



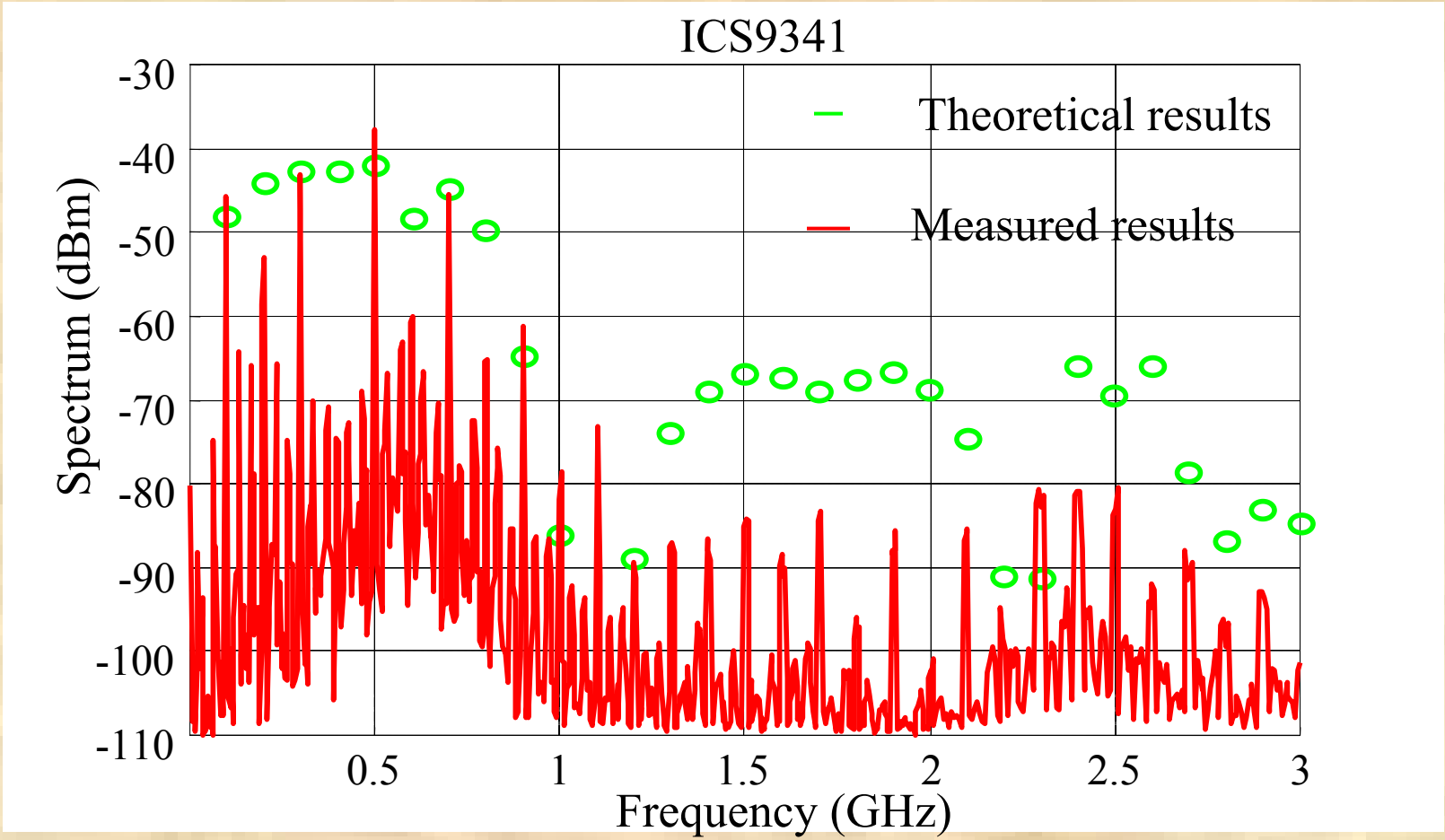
Modeling results with different C_{PD}



Modeling results for IDT807 (load C only)



Modeling results for ICS9341 (load C only)

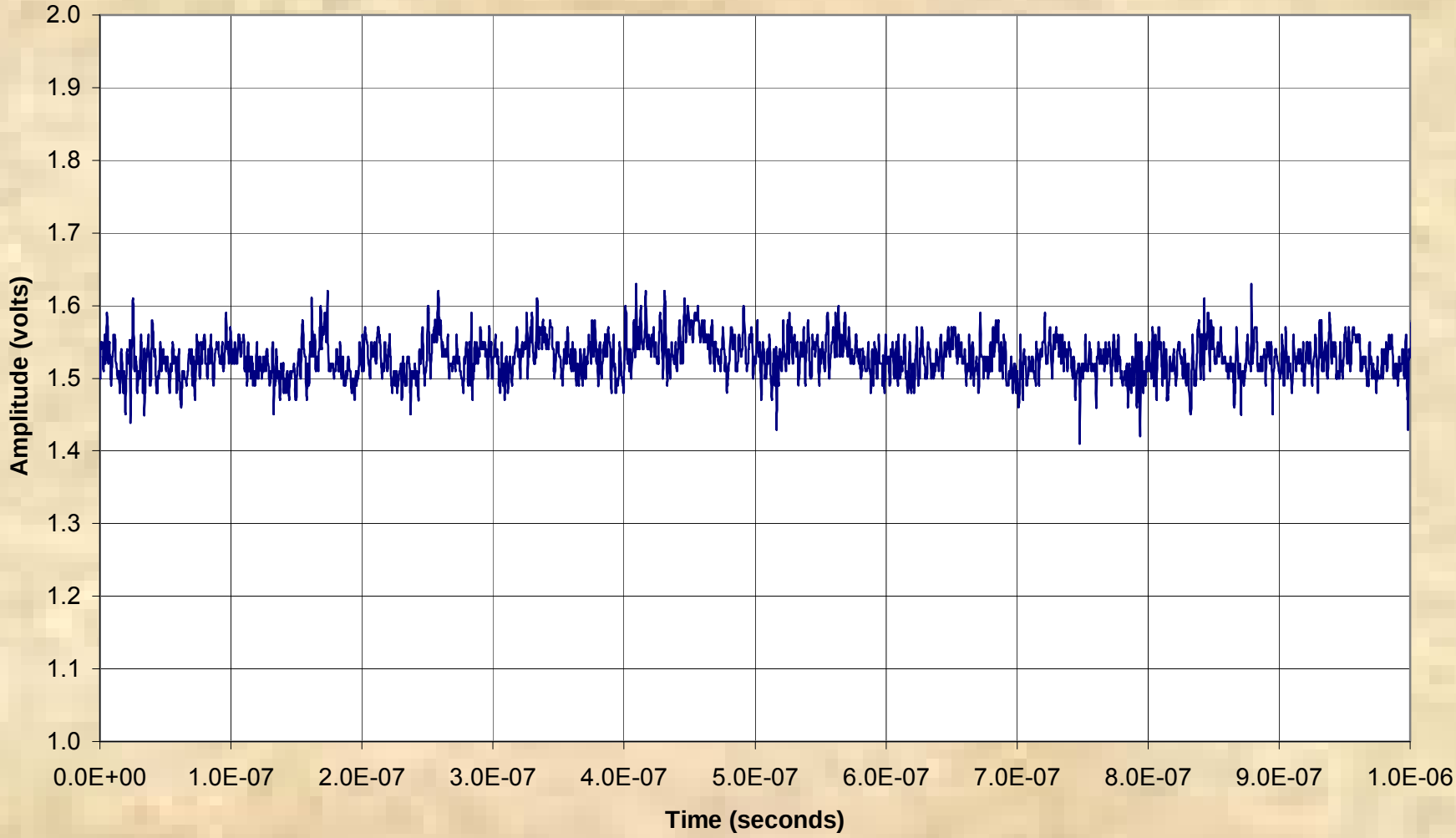


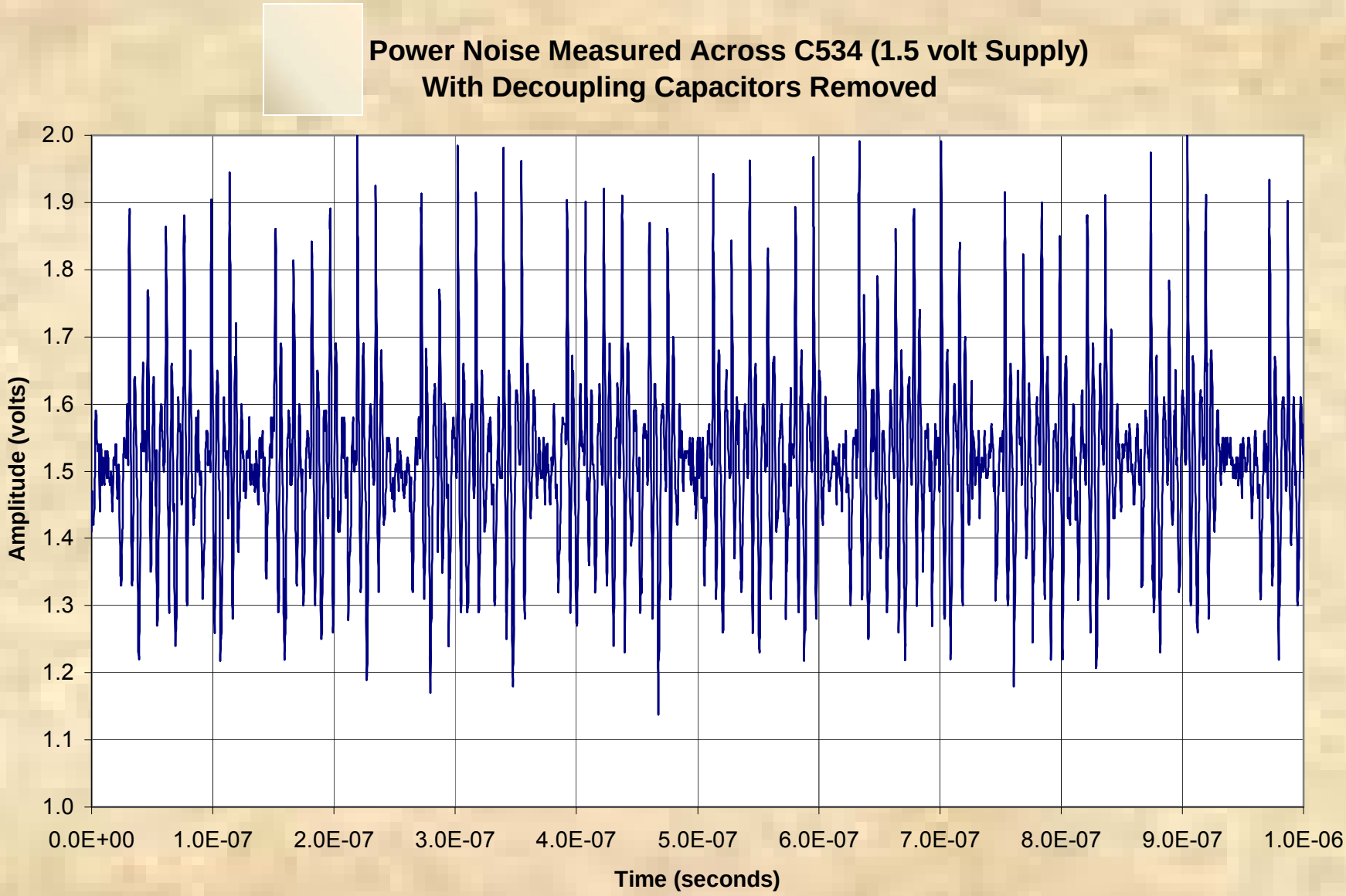
Note: The chip has a lot of different clocks: 8 CPU (133 MHz), 8 PCI (33.3 MHz), 2 USB (64 MHz and 32 MHz) and 2 REF (14.318 MHz).

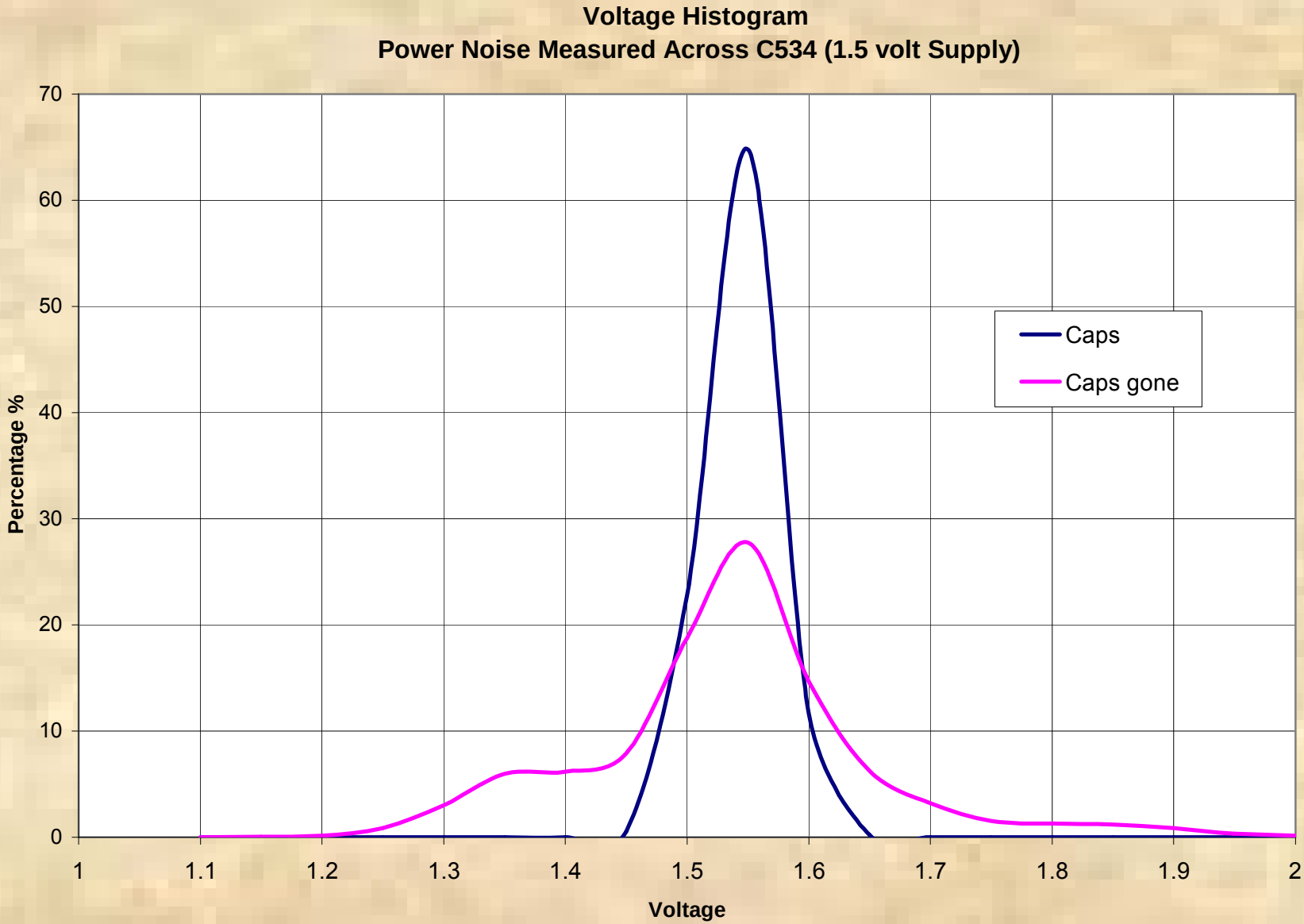
Other Sources on Active Board

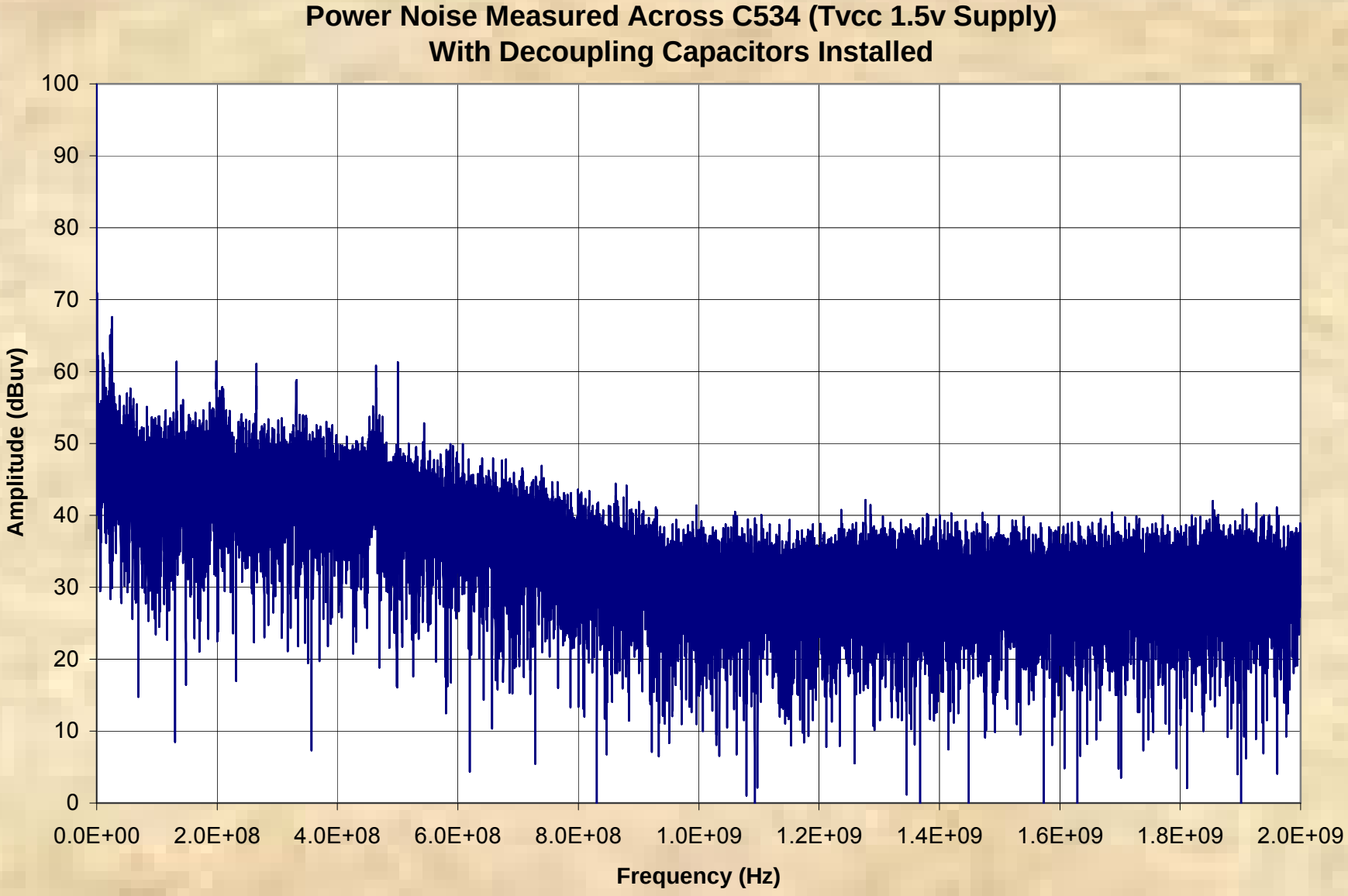
- Large ASICs do not specify C_{pd}
- Measured power/ground plane noise for large ASIC with and without decoupling capacitors installed
- Circuits operating with exerciser software
- Examples for 1.5 volt and 2.5 volt supplies

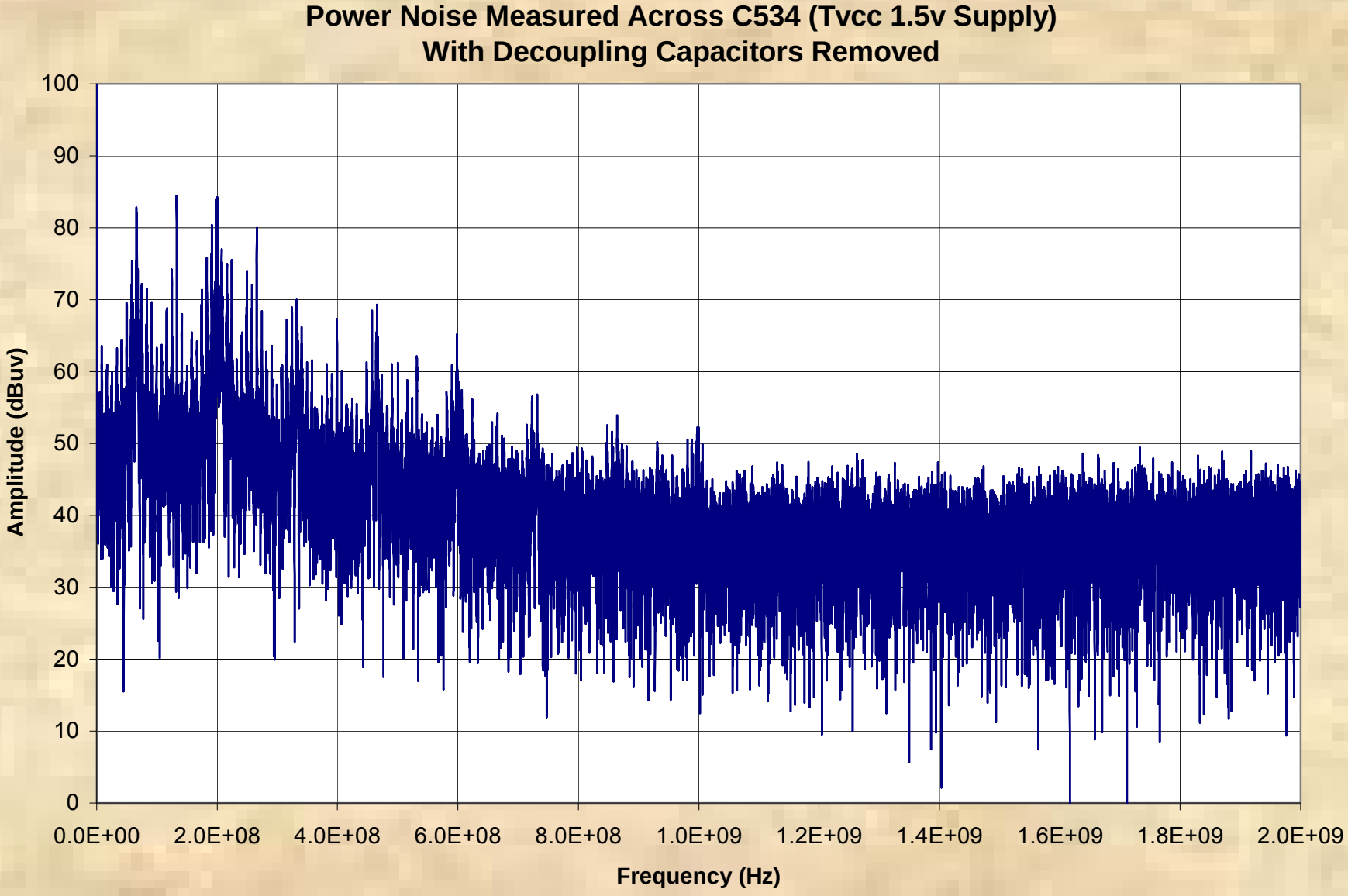
Power Noise Measured Across C534 (1.5 volt Supply) With Decoupling Capacitors Installed



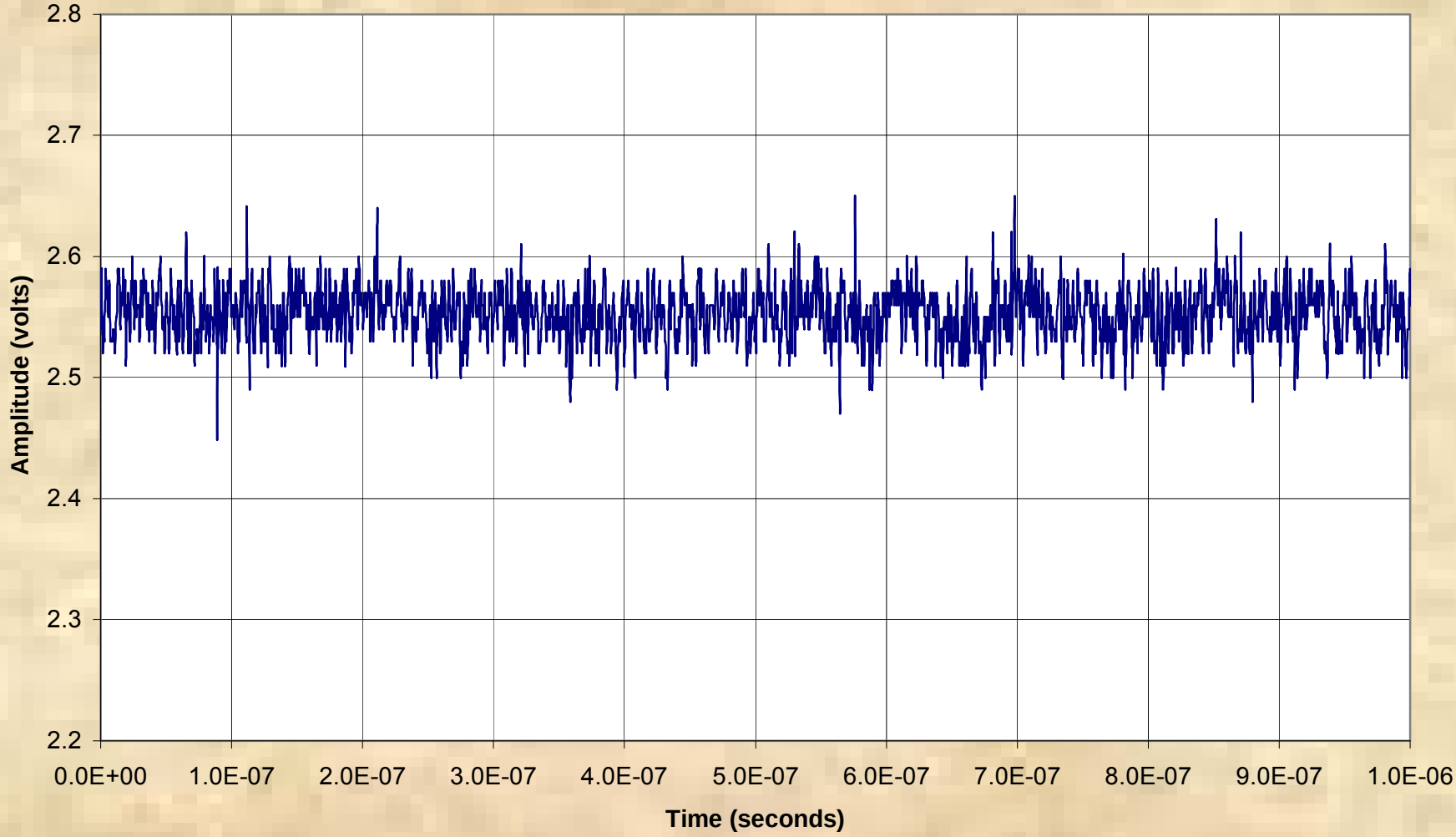

Power Noise Measured Across C534 (1.5 volt Supply)
With Decoupling Capacitors Removed
Amplitude (volts)
2.0
1.9
1.8
1.7
1.6
1.5
1.4
1.3
1.2
1.1
1.0
0.0E+00
1.0E-07
2.0E-07
3.0E-07
4.0E-07
5.0E-07
6.0E-07
7.0E-07
8.0E-07
9.0E-07
1.0E-06
Time (seconds)

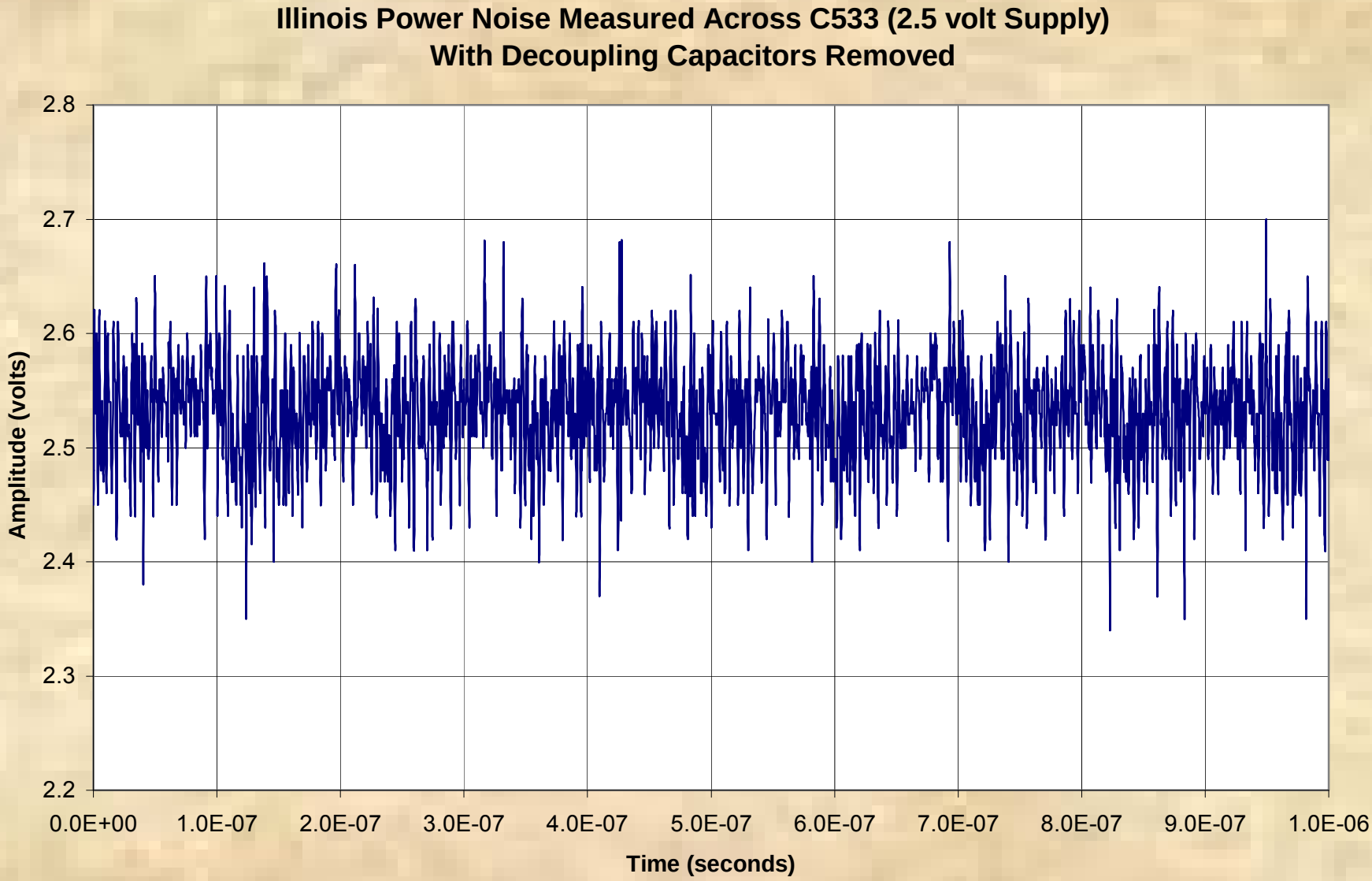

Voltage Histogram
Power Noise Measured Across C534 (1.5 volt Supply)
Percentage %
70
60
50
40
30
20
10
0
1
1.1
1.2
1.3
1.4
1.5
1.6
1.7
1.8
1.9
2
Voltage
Caps
Caps gone

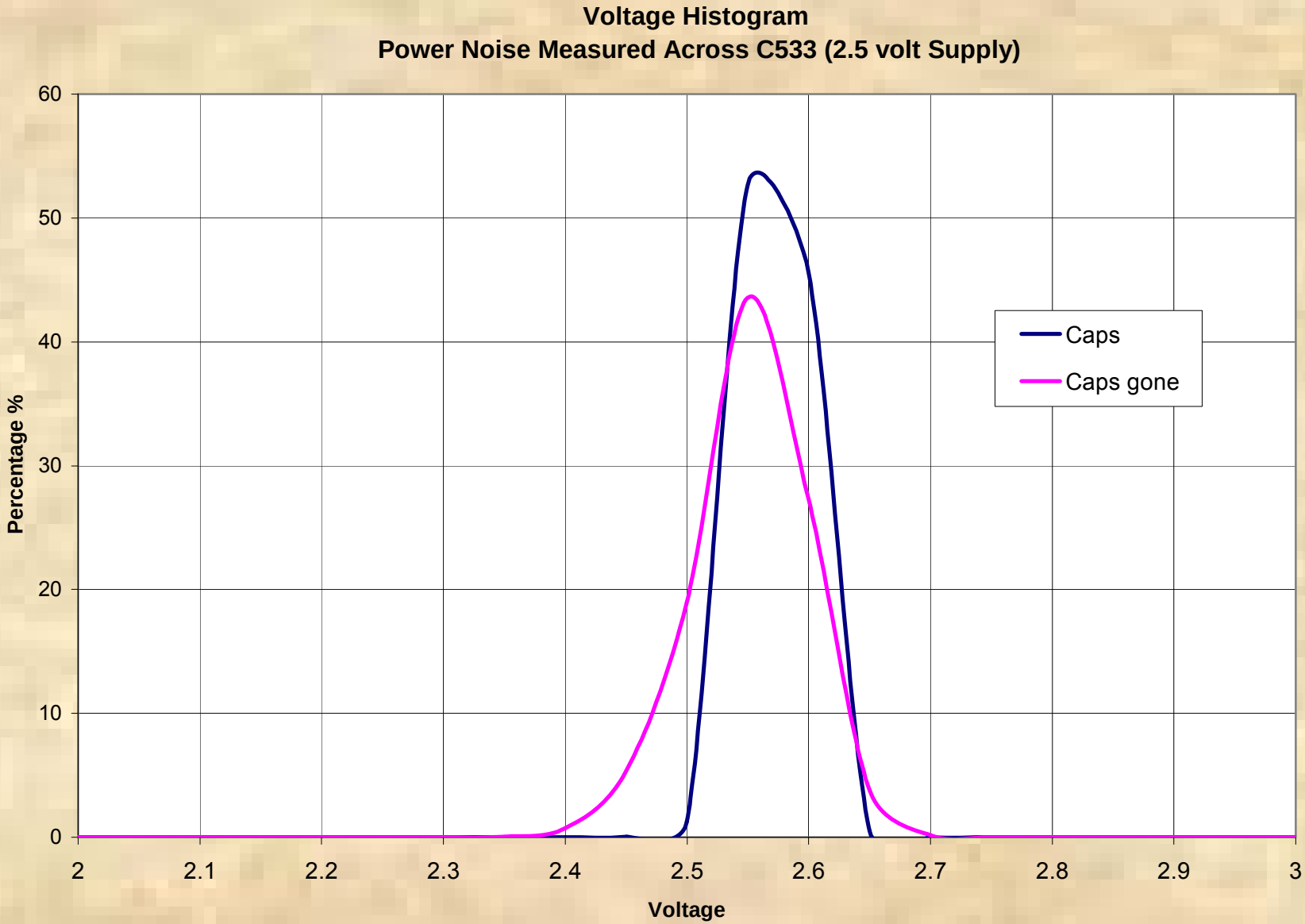

Power Noise Measured Across C534 (Tvcc 1.5v Supply)
With Decoupling Capacitors Installed
Amplitude (dBuv)
100
90
80
70
60
50
40
30
20
10
0
0.0E+00
2.0E+08
4.0E+08
6.0E+08
8.0E+08
1.0E+09
1.2E+09
1.4E+09
1.6E+09
1.8E+09
2.0E+09
Frequency (Hz)

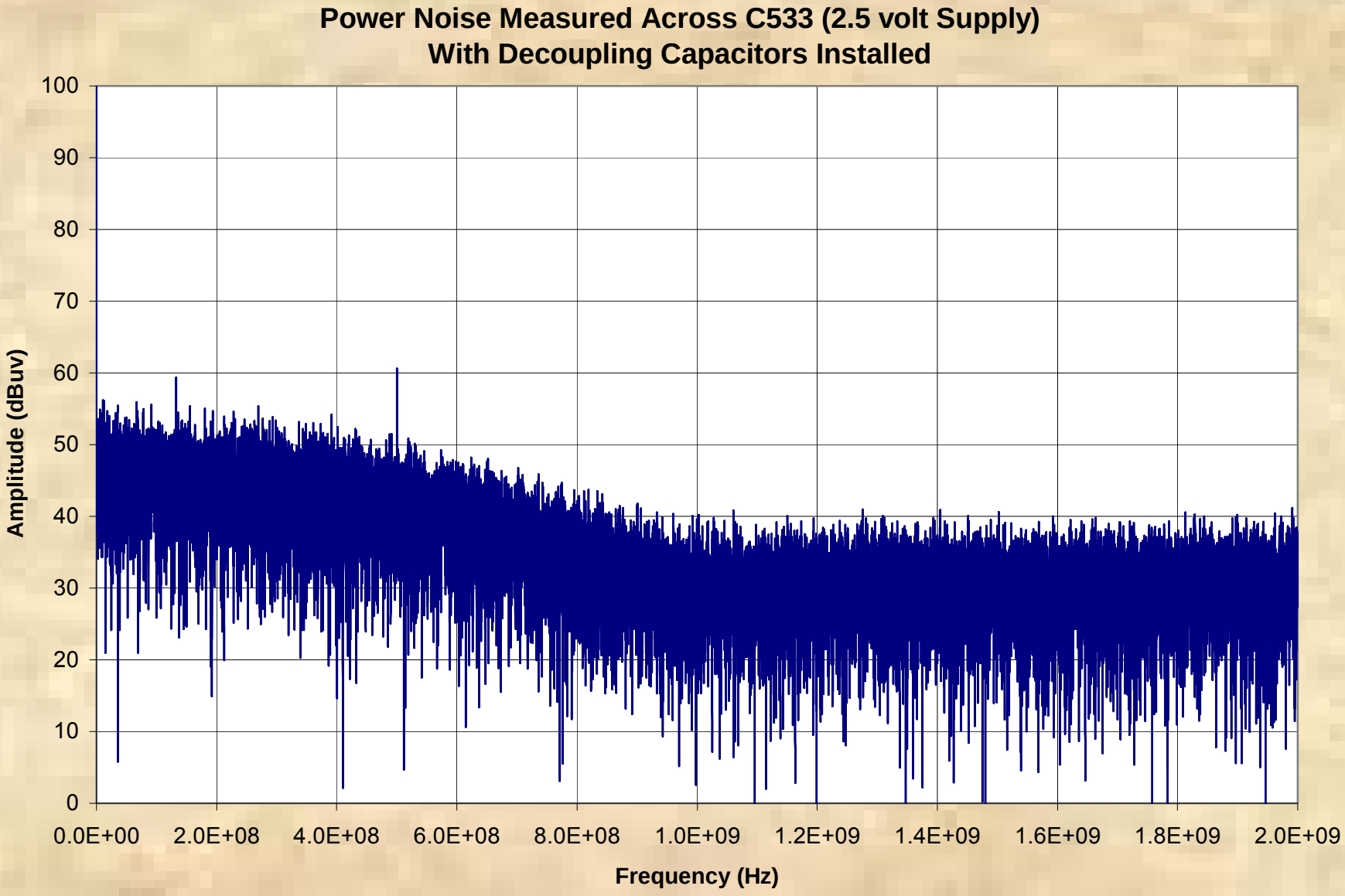

Power Noise Measured Across C534 (Tvcc 1.5v Supply)
With Decoupling Capacitors Removed
Amplitude (dBuv)
100
90
80
70
60
50
40
30
20
10
0
0.0E+00
2.0E+08
4.0E+08
6.0E+08
8.0E+08
1.0E+09
1.2E+09
1.4E+09
1.6E+09
1.8E+09
2.0E+09
Frequency (Hz)

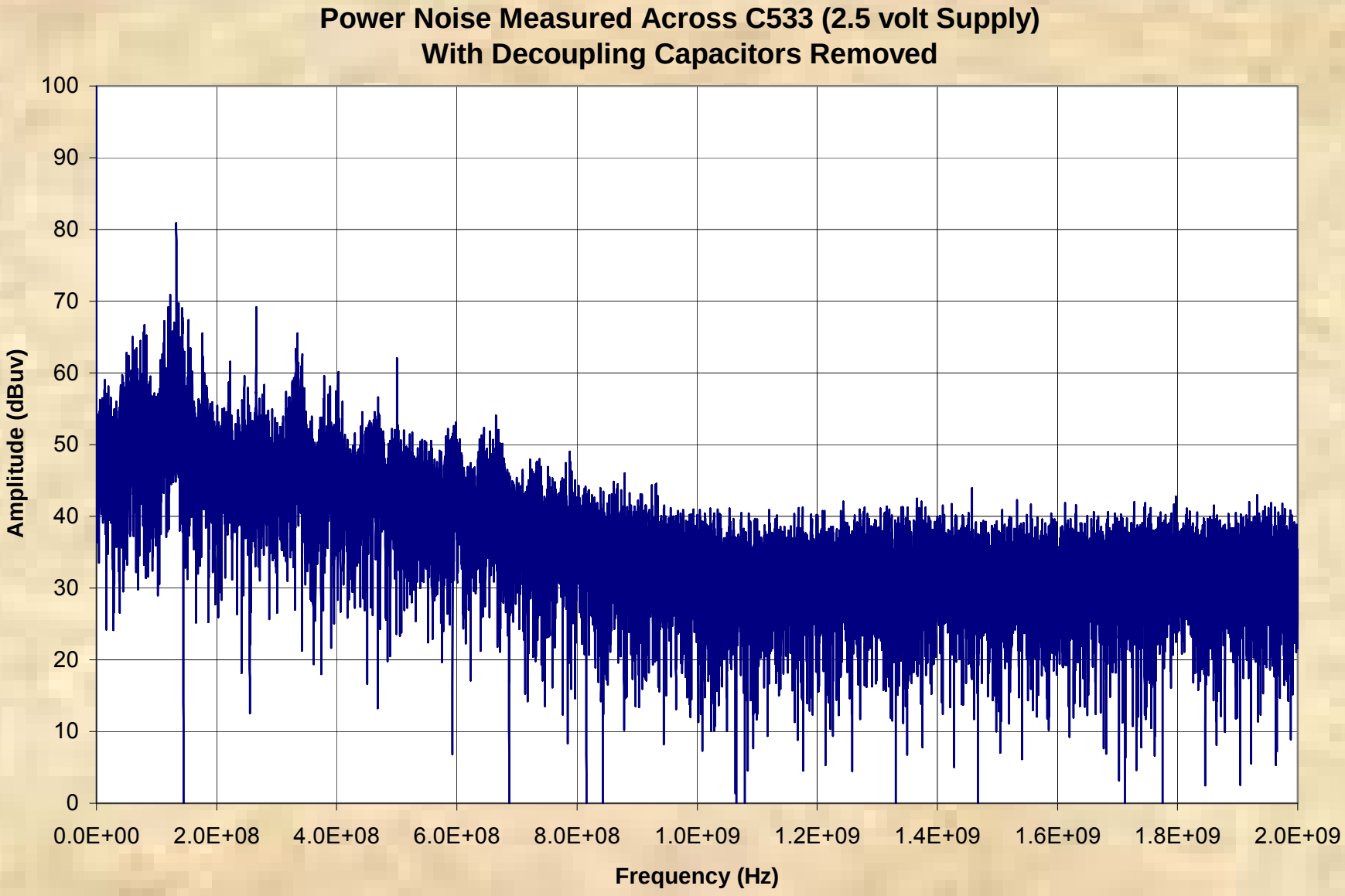
Illinois Power Noise Measured Across C533 (2.5 volt Supply) With Decoupling Capacitors Installed




Illinois Power Noise Measured Across C533 (2.5 volt Supply)
With Decoupling Capacitors Removed
Amplitude (volts)
2.8
2.7
2.6
2.5
2.4
2.3
2.2
0.0E+00
1.0E-07
2.0E-07
3.0E-07
4.0E-07
5.0E-07
6.0E-07
7.0E-07
8.0E-07
9.0E-07
1.0E-06
Time (seconds)


Voltage Histogram
Power Noise Measured Across C533 (2.5 volt Supply)
Percentage %
60
50
40
30
20
10
0
2
2.1
2.2
2.3
2.4
2.5
2.6
2.7
2.8
2.9
3
Voltage
Caps
Caps gone


Power Noise Measured Across C533 (2.5 volt Supply)
With Decoupling Capacitors Installed
Amplitude (dBuv)
100
90
80
70
60
50
40
30
20
10
0
0.0E+00
2.0E+08
4.0E+08
6.0E+08
8.0E+08
1.0E+09
1.2E+09
1.4E+09
1.6E+09
1.8E+09
2.0E+09
Frequency (Hz)


Power Noise Measured Across C533 (2.5 volt Supply)
With Decoupling Capacitors Removed
Amplitude (dBuv)
100
90
80
70
60
50
40
30
20
10
0
0.0E+00
2.0E+08
4.0E+08
6.0E+08
8.0E+08
1.0E+09
1.2E+09
1.4E+09
1.6E+09
1.8E+09
2.0E+09
Frequency (Hz)

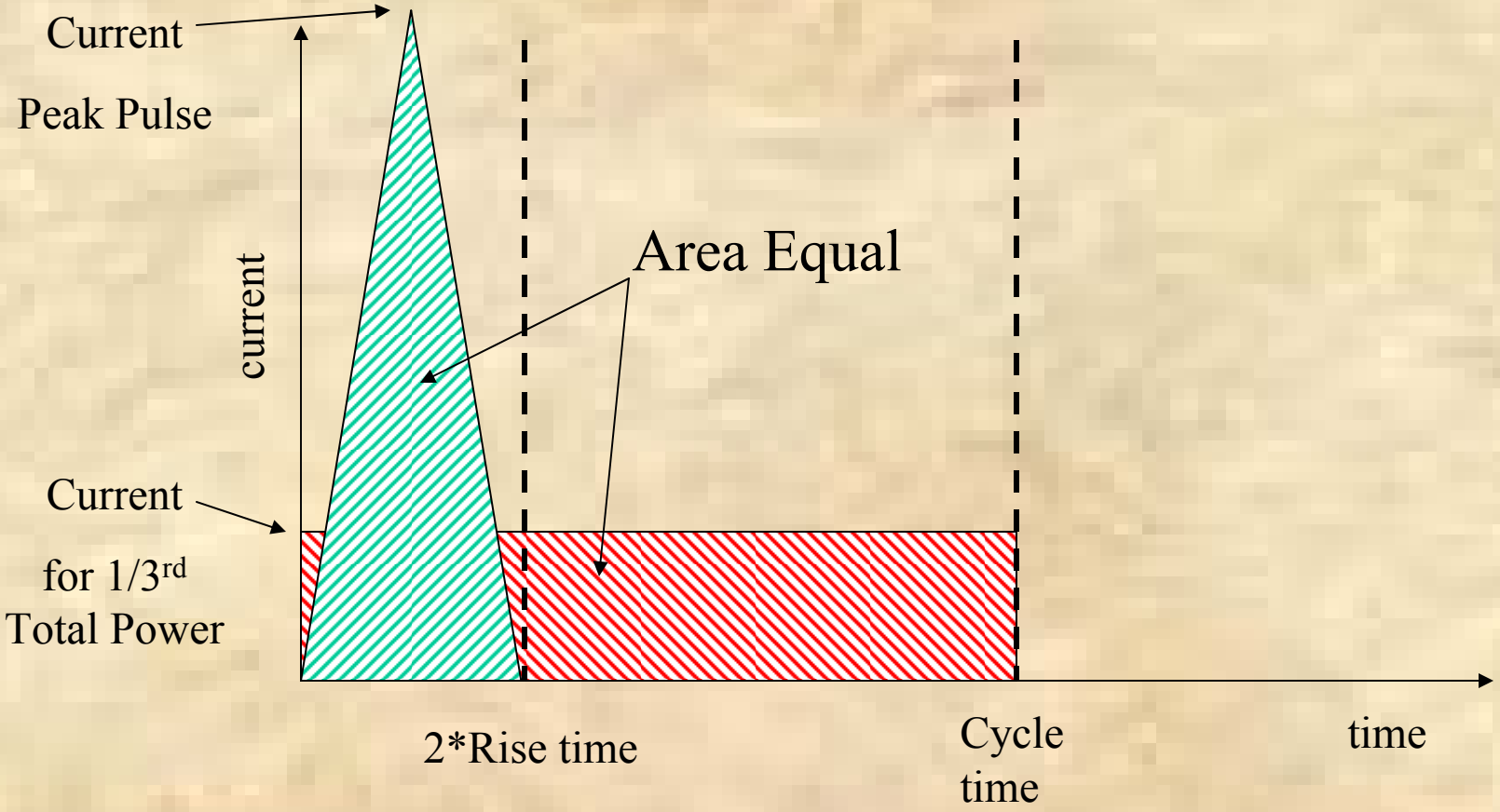
Preliminary Results for Large ASICs/ICs

- Core current smoothes out to DC due to package inductance
- I/O current dominates for EMC
- Pseudo-random data
- Statistical analysis indicates half of data bus at ‘1’ state most of the time
- Statistical analysis indicates 1 – 2 data lines switch high vs. low

ASIC Rough Estimation Time Varying Current in Power

- Use 1/3rd Specified power for time varying power
- Use 2*t_r for width of current pulse
- Find height of current pulse to meet time varying power
  - Use supply voltage

ASIC Rough Estimation Time
Varying Current in Power



To prevent/Reduce Unintentional Signal -- Power Plane Bounce

- ✓ Distribute Decoupling Capacitors evenly Across entire Board
- ✓ Capacitor Value not Especially Important!
  - .01 uF or .1 uF the same!
  - Use the largest value of capacitor in the selected SMT Package
- ✓ Adding 'high frequency' capacitors does ***NOT*** help, and may ***HURT*** at low frequencies!

To prevent/Reduce Unintentional Signal Power Plane Bounce

- ✓ Provide capacitors near ALL IC power pins for functionality
  - Distance from IC critical
- ✓ Avoid routing critical nets through vias
  - This effect requires decoupling between all planes
- ✓ Consider Alternative Solutions
  - Lossy Decoupling
  - Closely spaced Planes (Increased distributed capacitance)

Power Decoupling Summary

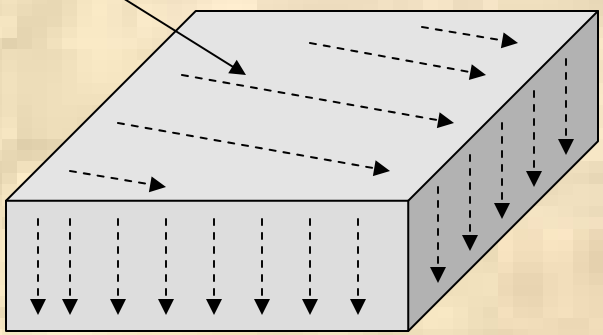
- Two different types of decoupling analysis required
  - Transient analysis for functionality
    - Apparent inductance must be included
  - Steady state analysis for EMC
    - Resonance effects important
- Source of power/ground-reference plane noise
  - ***Current***

Shielding

- Basic requirement is for tangential electric fields to equal zero at perfect conductors
  - Induces current in conductor to meet this requirement
- Most shields are close enough to perfect
- Most shields are thicker than effective skin depth
  - Currents on surface only

Perfect Shielded Enclosure

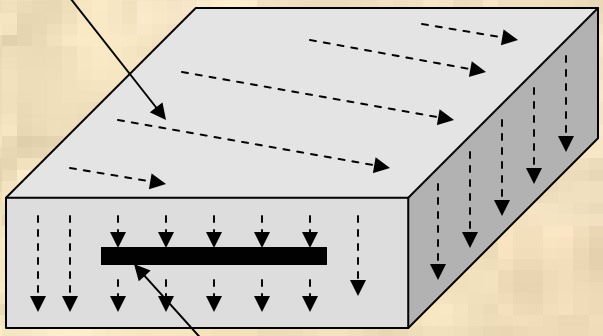
Current on inside of metal enclosure due to internal fields (from PC board, cables, etc)



Perfect metal enclosure (no apertures/holes) will have NO currents on outside of enclosure

Not-So-Perfect Shielded Enclosure

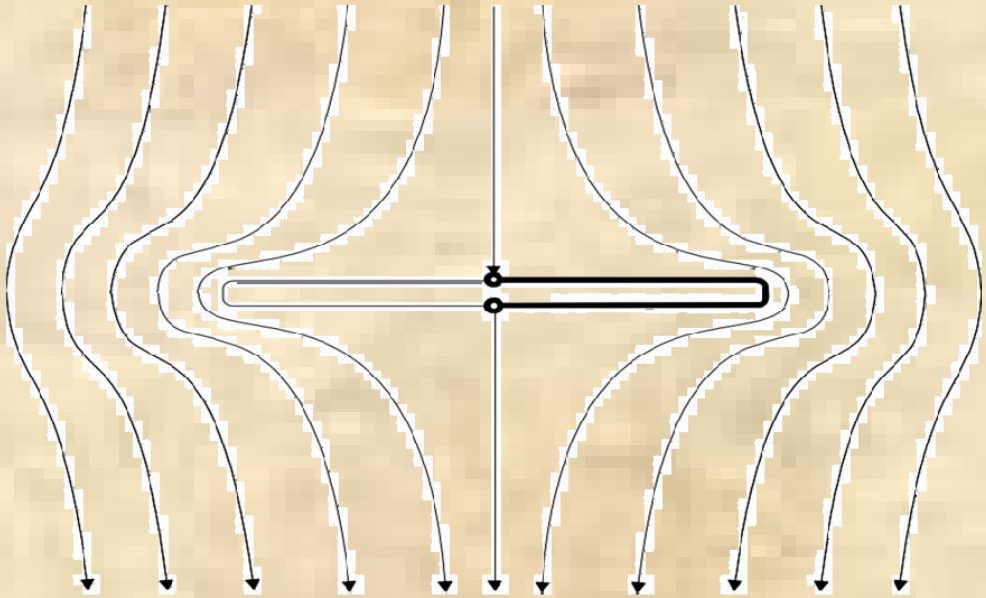
Current on inside of metal enclosure due to internal fields (from PC board, cables, etc)



Slot interrupts currents on inside of enclosure

Currents must travel around slot!

Current Path is Longer Around Aperture



-- Currents must flow in longer path

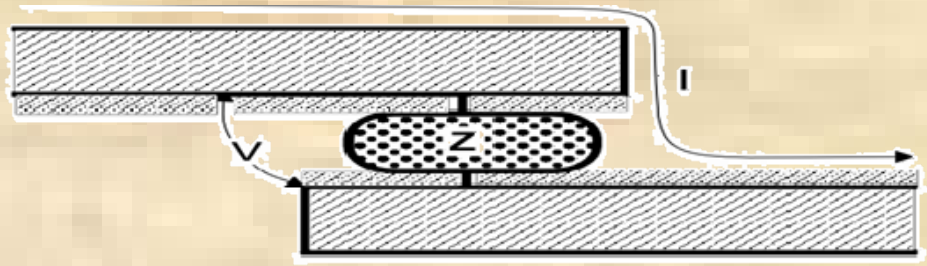
-- Inductance in this current path

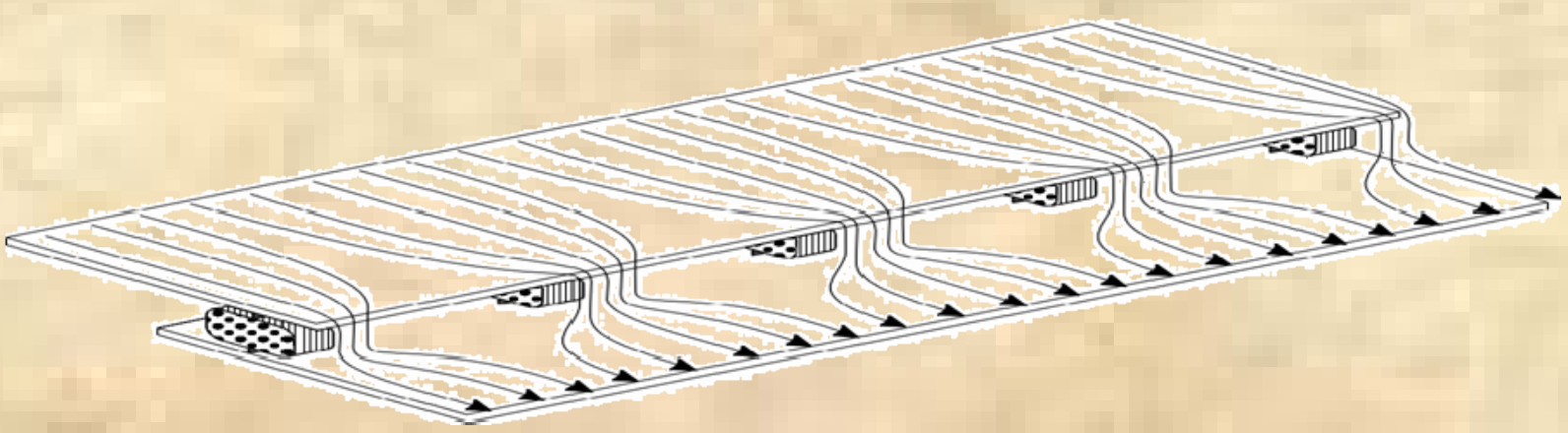
-- Current through impedance = voltage across aperture

Shield External View

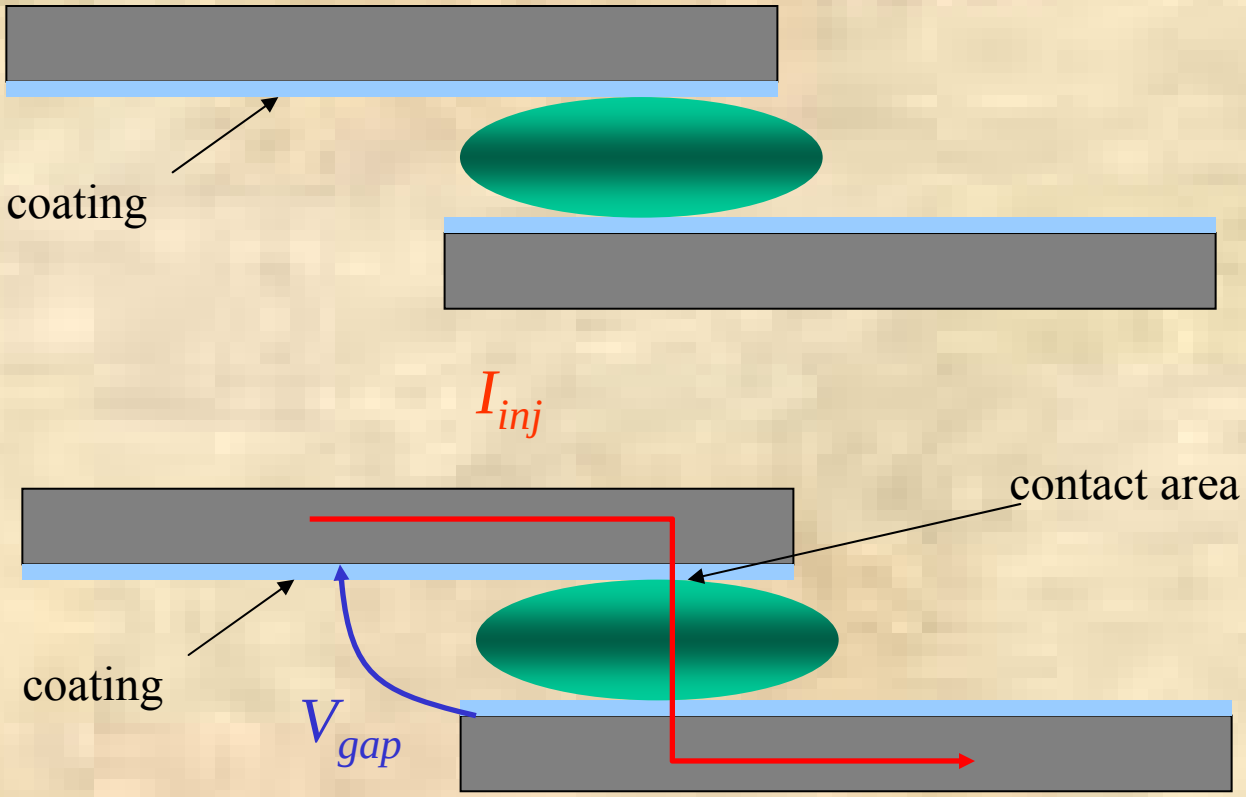
- Voltage across slot
  - Creates currents on outside of enclosure
  - Currents cause fields
- Shield ‘leakage’
  - Amount of ‘leakage’ at a given frequency is dependent on length of slot
    - Longer slots mean longer current path interruption
    - More inductance --- More impedance --- More voltage across slot

Joints with Gaskets are Three-Dimensional

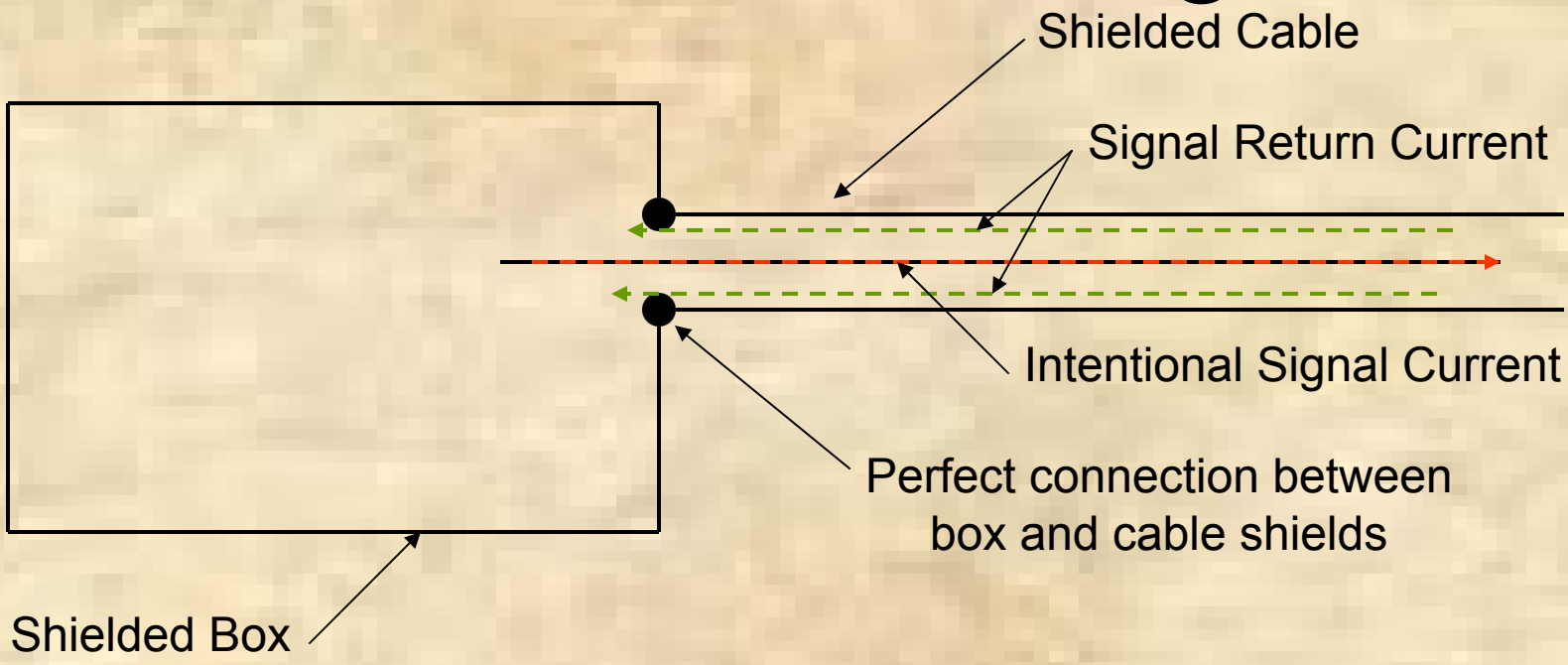




Metal-to-Metal Contact Required!

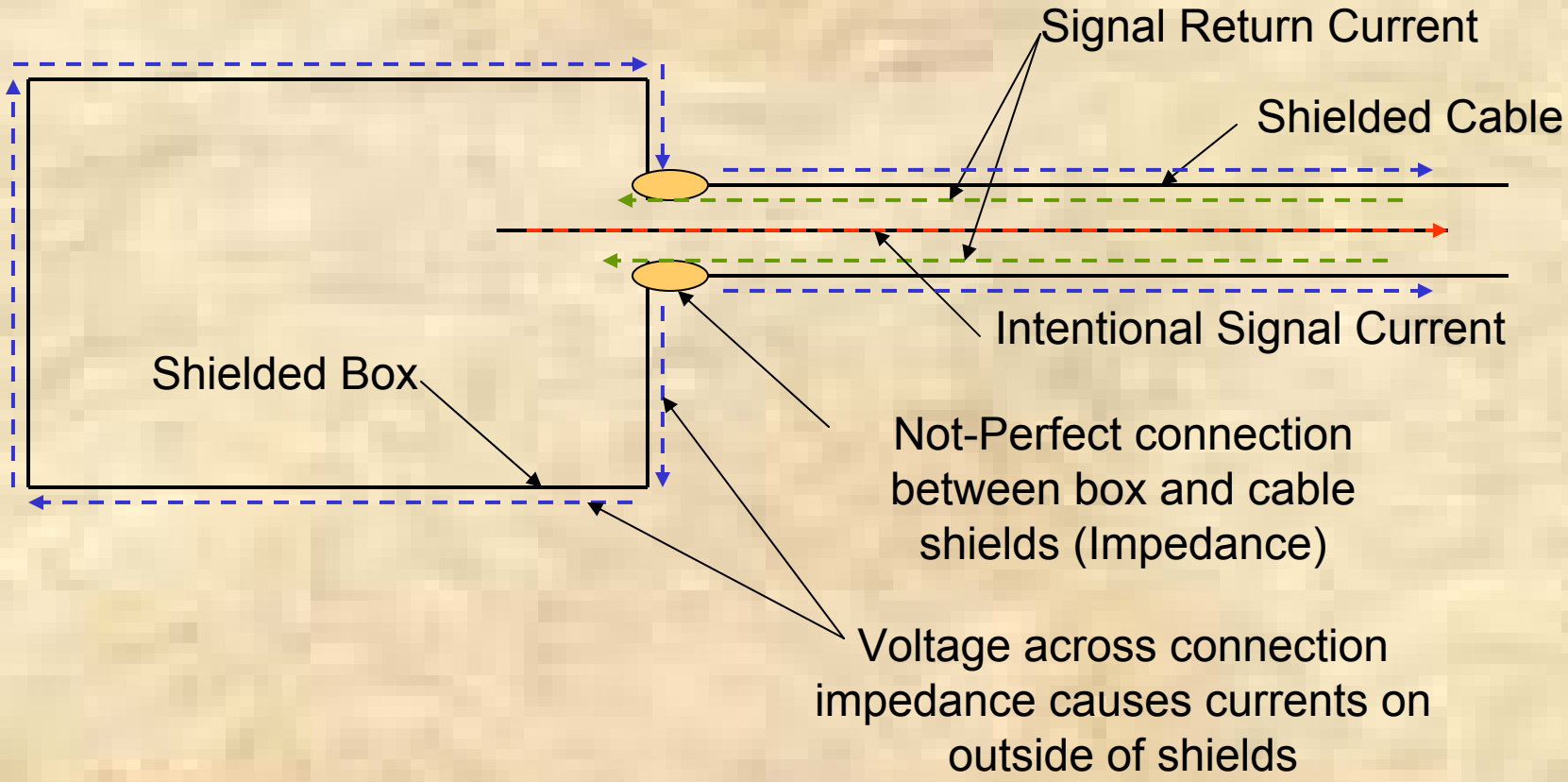


Cables and Shielding

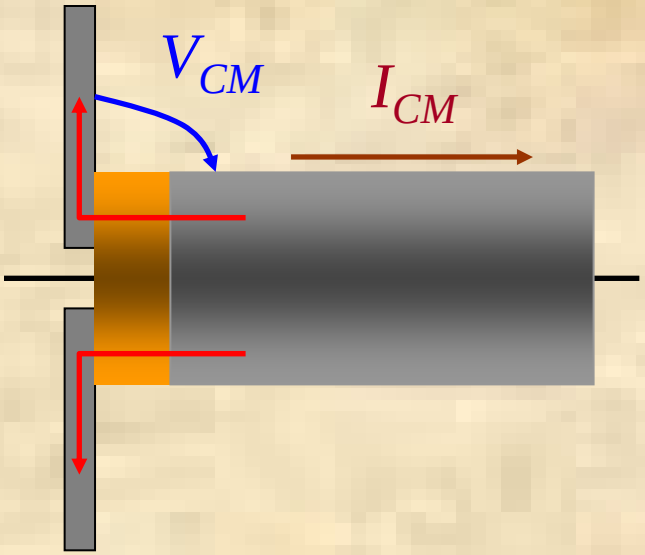


All Currents are Enclosed within Shielded Enclosure and Cable Shield

Not-so-Perfect Connection



Cable Connection to Chassis is Usually the Weak Point

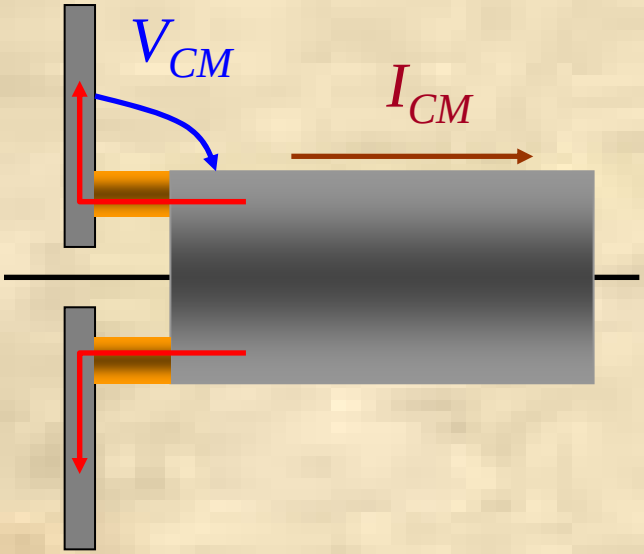


SMALL contact impedance (360°)

SMALL V_{CM}

SMALL I_{CM}

SMALL radiation



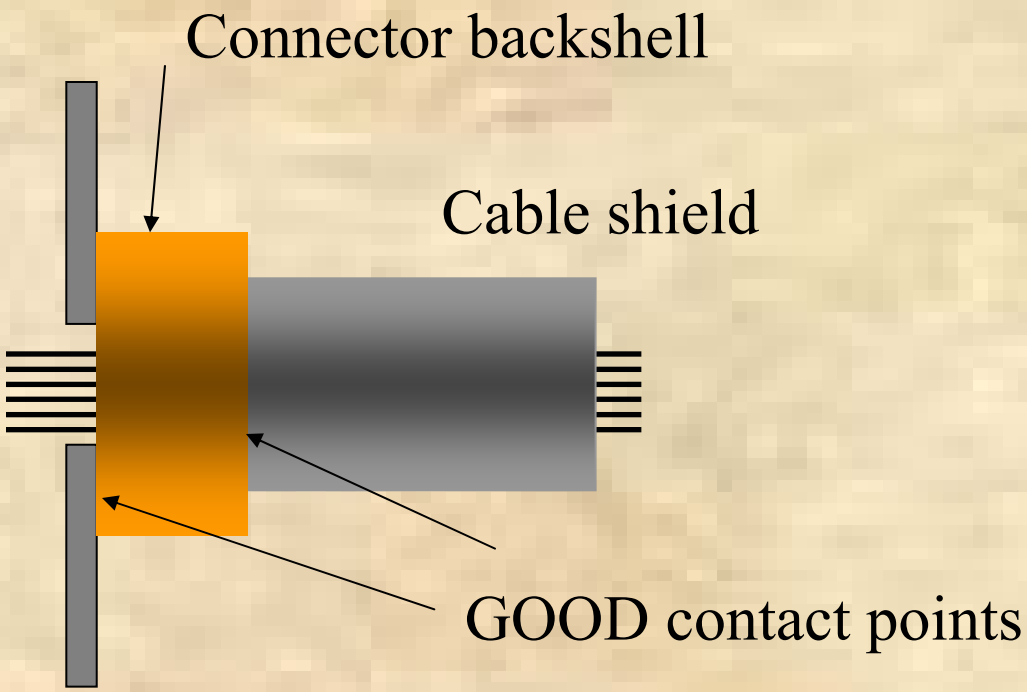
HIGH contact impedance (<360°)

HIGH V_{CM}

HIGH I_{CM}

HIGH radiation

Cables Require 360 Degree contact for Good Shielding

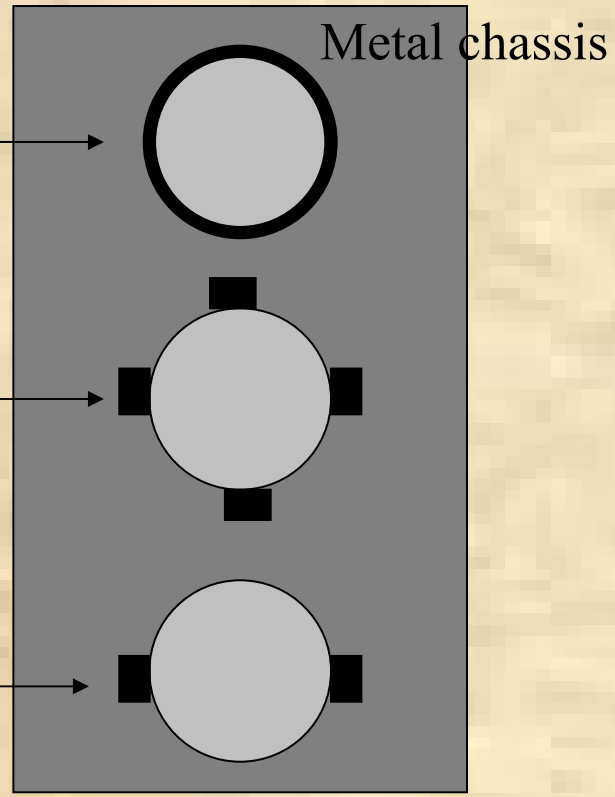


Cables

360°: good to about infinity

4 points: good to about 100 MHz

2 points: good to about 10 MHz

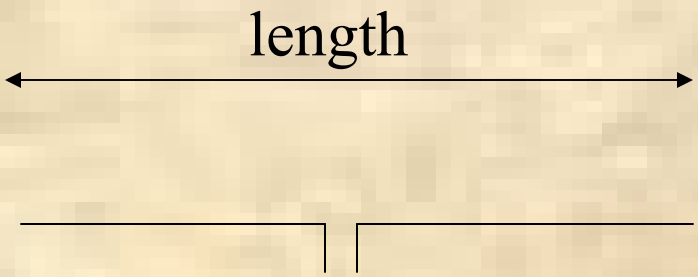


EM TIGHT

Antennas

- All metal conductors are antennas!
- Some are more efficient than others
  - especially at certain frequencies
- The same antenna can radiate or receive
  - reciprocity works!

Simple Dipole Antenna



Dipole Antenna is most efficient when it's length is one-half the wavelength

But --- it will work at ALL frequencies, just not as efficiently

Hertzian Dipole Approach

--Break Antenna into small segments

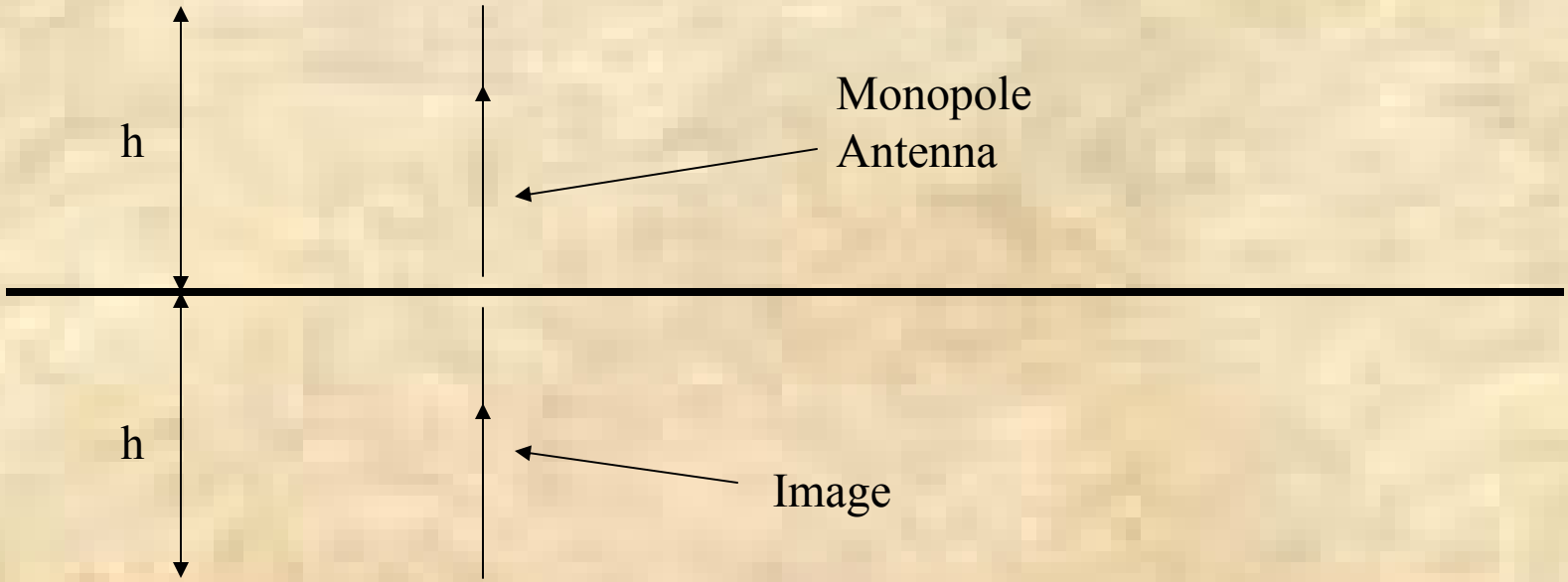
-- solve for E field for each segment individually

-- Vector sum all contributions

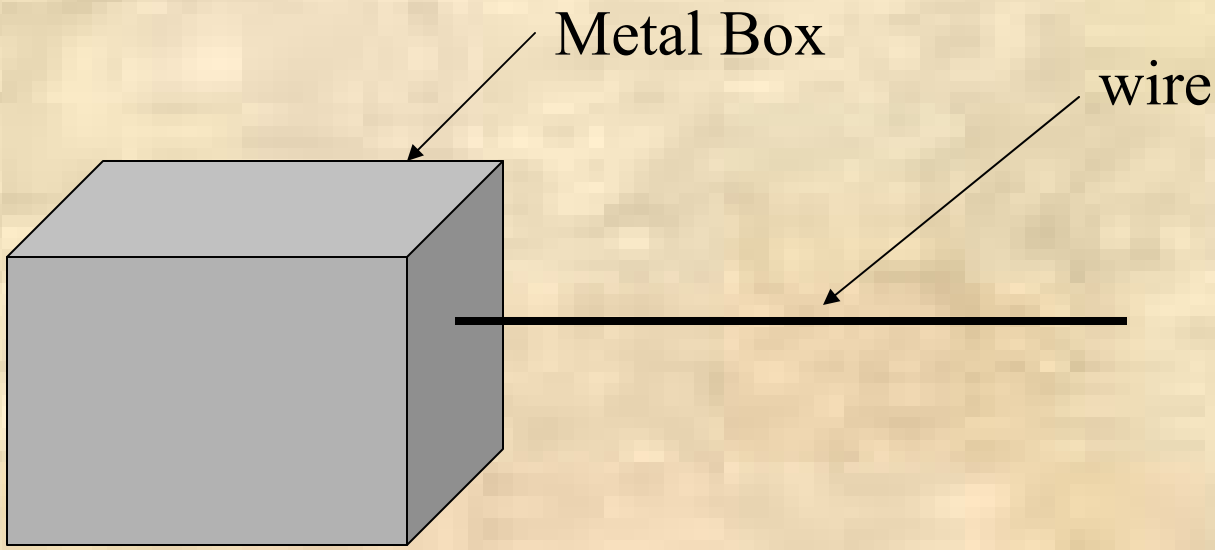
$$E_\theta = \frac{IL\sin\theta}{4\pi\varepsilon_0}\left(\frac{j\omega}{c^2 r} + \frac{1}{cr^2} + \frac{1}{j\omega r^3}\right)$$

Monopole Antenna

- Must work with a 'ground' image plane!
- Image plane must be very large (infinite)



This is not a Monopole Antenna



This is more like a lumpy, unbalanced dipole!

EMC Design Summary

- ✓Eliminate at the source
- ✓Think ahead -- Plan ahead
- ✓Intentional and Unintentional currents
- ✓What is the Frequency Spectrum of the Current on Critical Nets ?
- ✓Where does the Return Current Flow ?
- ✓No magic!

PCB EMC Design Summary

Review of Important Things

- Control the **current**
- Consider each potential emissions cause separately
- Route Critical Traces first
- Consider EMC effects *early* during board design
  - First pass boards for functionality only is usually a bad idea!

Number **ONE** Problem

- Intentional signal ***return current***

Top Contributors

- Non-optimum critical net termination
- Critical nets over splits in planes
- Critical nets routed to different layers with a change in reference planes
- Critical nets too close to I/O nets
- Un-split ground-reference planes in low speed I/O area
  - Treat I/O "ground" leads as I/O signal leads

Top Contributors (cont)

- Decoupling
  - Largest value capacitance in selected package size, spread over entire board
  - Extra capacitors near high speed ICs
  - Decouple all adjacent plane pairs
- I/O reference connected to chassis with low impedance path
- Filter all low speed I/O signal traces

Top Contributors (cont)

- Bury Critical traces on internal layers
- Keep high speed devices far from I/O area
- USB and Ethernet special cases
  - do not need planes under final I/O lines
- Provide “grounding” option for large heatsinks

Where to Go for More?

- Limited selection of EMC design books
  - Beware of some popular books!!!
  - "PCB Design for Real-World EMI Control" (***good choice***)
    - Bruce Archambeault
- EMC 'experts'
  - Experience is important
  - Again, beware ---- ask questions and understand WHY
- Cookbooks do not work! Every case is special and different